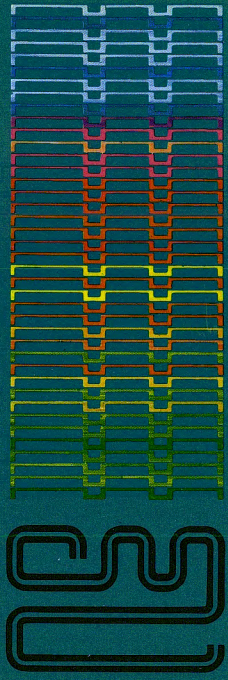


Integrated Circuits Data Book

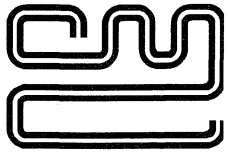
Consumer Microcircuits Limited

Edition 3

ISO 9002 Approved

Integrated Circuits Data Book

Edition 3



Consumer Microcircuits Limited

1 Wheaton Road Witham Essex CM8 3TD England
Telephone: +44 1376 513833 • Telex: 99382 CMICRO G • Telefax: +44 1376 518247

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Integrated Circuits Data Book

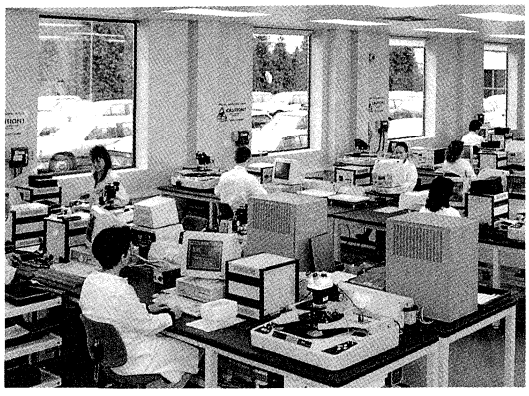
Sectional Contents

Integrated Circuits Data Book

Section 1

Product Selection

Consumer Microcircuits Limited



Consumer Microcircuits Limited (CML) is a member of the highly successful CML Microsystems Plc group of companies, and is based at Witham in England.

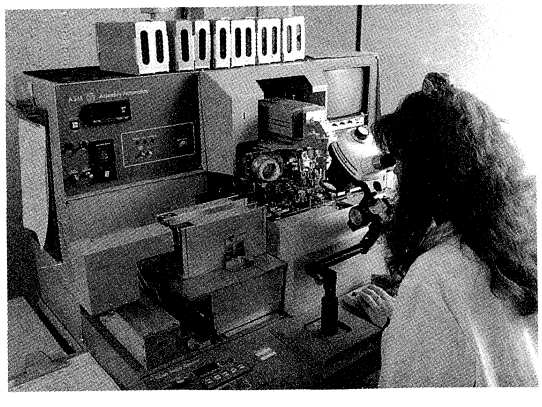
For over 20 years CML has been involved in the design and manufacture of specialized integrated circuits for Communications Markets Worldwide. CML is accredited to BS 5750 Part 2, a British Standard for quality systems, compatible with the European Community Standard EN 2900 and the International Standard ISO 9002.

Specializing in audio processing, signalling and data communication devices, the company products utilize a number of mixed analogue and digital CMOS processes. The combination of detailed system knowledge and engineering capability have resulted in products for Two-Way Mobile and Cellular radio, Telecommunications, Wireless Data-Communications, Voice Security and Military Communications.

As part of a 'total-capability' offering, CML has its own extensive modern production and packaging facilities producing both plastic and ceramic devices.
All microcircuit products are offered in surface mount or dual-in-line packages; 100 percent are tested and fully guaranteed.

The combination of 'on-site' Design, Engineering and Production allows CML to offer the highest level of customer service, quality and prompt delivery.

CML's own team of sales engineers and over 30 Distributors Worldwide ensure customers receive excellent on-going local technical and commercial support.



Consumer Microcircuits Limited and BS 5750

In November 1993 CML qualified for accreditation to BS 5750 Part 2.

BS 5750 is a British Standard for Quality Systems, compatible with the European Community Standard EN 29000 and the International Standard ISO 9002.
The section of the standard which applies to CML's operations is Part 2 and applicable to Microcircuit Production.
ISO 9001 (Production and Engineering) accreditation is expected in early 1995.

NATIONAL INSPECTION COUNCIL QUALITY ASSURANCE LIMITED

Certificate Number

2834

NATIONAL ACCREDITATION OF CERTIFICATION BODIES

This is to Certify that

CONSUMER MICROCIRCUITS LTD

is Registered to produce goods or provide services in accordance with BS 5750 : PART 2 : ISO 9002 : EN 29002 : 1987

Signed for and on behalf of NICQA Limited

Director NICQA Limited *Date: 23 NOVEMBER 1993*

CML Product Locator

To enable the widest possible use to be made of the information provided in this edition of the Data Book, this section contains comprehensive tables which illustrate the uses of CML microcircuits by both System Function and Market Application.

Each table also indicates the page upon which the relevant information may be found.

For rapid access to data the list below is a direct product/page index.

CML Products Listed in Alpha-Numeric Order:

Integrated Circuits Data Book

Section 1

Product Selection by System Function

STOP PRESS

NEW PRODUCTS Available Shortly

- **CDPD/AMPS Cellular Wireless Data - 19.2kb/s GMSK Modem and AMPS Processor**
- **CDPD - Data Modem with CDPD Data Processing**
- **Half-Duplex Low-Cost GMSK Modem**
- **Caller Line Indentification to UK Specifications**

Audio Processing Arrays

Audio Processing Arrays				Arrays of switched capacitor filters; low, high and bandpass, deviation limiters, pre-/de-emphasis and digitally controlled gain and switching functions; voice, signalling and data compatible. 5 volt devices.		
Description	**Signal Paths**	**Duplex**	**Filtering**	**Comments**	**Product**	**Page**
PMR Audio Processor	Switched Rx/Tx	Half	3kHz LP 300Hz HP 2550/3000Hz LP Pre/De-Emp	VOGAD (compressor); Carrier Detect (squelch function). Controlled two-point modulation and Rx audio outputs. Pre- and De-Emphasis. Tx and Rx audio input paths; Sub-audio and data inputs. Rx and Tx filtering and deviation limiter to international standards. Digitally controlled signal level adjustment and array functions. Serial data control.	FX506	2 - 35
PMR Audio Processor	Switched Rx/Tx	Half	LP + HP = voicepath (297Hz - 3000Hz) Pre/De-Emp	VOGAD (compressor); Inputs from external audio (voice, sub-audio, scrambling, tone and data) processes; Controlled two-point modulation and LS audio outputs. Pre- /De-Emphasis filtering and deviation limiter. Digitally controlled signal level adjustment and array functions. Access to internal signal paths. Serial data control.	FX806A	2 - 123
NMT Audio Processor	Rx Tx Signalling	Full	Voiceband (LP + HP) 4kHz BPF Pre/De-Emp	VOGAD amp; Inputs from external audio (voice, scrambling, tone and data) processes; Controlled modulation, Separate signal and audio paths, Tx, sidetone and LS audio outputs; Voice storage and DTMF compatible inputs. Pre- /De-Emphasis filtering and deviation limiter. Digitally controlled signal level adjustment and array functions. Access to internal signal paths. Serial data control.	FX816	3 - 39
TACS Audio Processor	Rx Tx Signalling	Full	Voiceband (LP + HP) 6kHz BPF Pre/De-Emp	Inputs from external audio (voice, scrambling, tone and data) processes. Controlled modulation; Tx, sidetone and LS audio outputs; Voice storage and DTMF compatible inputs. Pre- /De-Emphasis filtering and deviation limiter. Digitally controlled signal level adjustment and array functions. Access to internal signal paths. Serial data control.	FX826	3 - 51
R2000 Audio Processor	Rx Tx LF Data	Full	Voiceband (LP + HP) Pre/De-Emp LF Data	Inputs from external audio (voice, sub-audio, scrambling, tone and data) processes; Controlled modulation, sidetone and LS audio outputs; Voice storage and DTMF compatible inputs; Separate LF data path. Pre- /De-Emphasis filtering and deviation limiter. Digitally controlled signal level adjustment and array functions. Access to internal signal paths. Serial data control.	FX836	3 - 63

Tone Detectors and Generators		Audio frequency tone detectors and generators available for telephone, selcall, security and general purpose applications. Available interfacing ranges from simple to full µController control.				
Description	**Function**	**Freq. Range**	**Supply**	**Comments**	**Product**	**Page**
Tone Detector	Tone Detector	40Hz - 5kHz	10 - 15 Volts	Frequency set by external components.	FX105P	7 - 27
Unifil® Analogue Processor	Detector and Generator	50Hz - 5kHz	5 Volts	Versatile "Unifil®" device; Frequency set by components or clock input; Sine waves and Square waves.	FX406	7 - 41
Universal Call Progess Decoder	Non-Predictive Tone Decoder	300Hz - 2,150Hz	3 - 5.5 Volts	µP compatible; Serial data out (6-Bit).	FX613	6 - 3
Call Progress Tone Decoder	Predictive Tone Decoder	375Hz - 2,140Hz	3 - 5.5 Volts	µP compatible; 4-Bit (Hex) parallel data out; 13 popular 'telephone' tones.	FX623	6 - 11
Low-Voltage SPM Detector	Pulse Metering (SPM) Decoder	12kHz and 16kHz	3 - 5.5 Volts	Component-adjustable input threshold levels; Tone Follower and Cumulative Tone logic level outputs; High speechband rejection properties.	FX631	6 - 17
Dual SPM Detector	Two SPM Decoders	12kHz and 16kHz	5 Volts	Serial data or component-adjustable threshold level control; Tone Follower and Cumulative Tone logic level or high Z outputs.	FX641	6 - 25
Audio Signalling Processor	Full-Duplex Detector and Generator	Enc. 208Hz - 3kHz Dec. 313Hz - 6kHz	5 Volts	Serial "CBUS" Data Control; 2 Separate Tone generators (2/5/N-Tone and DTMF encoder); Output tone summation on-chip; Non-Predictive frequency detection.	FX803	2 - 91
Signal-To-Noise Enhancer	Signal Improvement	17Hz - 13kHz	2.5 - 5.5 Volts	Up to 8.5dB received signal-to-noise improvement; Sub-audio and audio ranges.	FX002	7 - 3
Non-Predictive Selcall Module	Intelligent Selcall Generator and Decoder	CCIR, EEA, ZVEI Tonesets	6 - 26 Volts	Complete Selcall Audio system for Mobile Radio: Simple Radio Interface; User configurable; Over-Air Reconfiguration, Stun and Release Facility; Coded Audio Alerts; All System GROUP-Call.	CM1481	2 - 161

Sub-Audio Tone Detectors and Generators		Sub-audio signalling products.				
Description	**Function**	**Freq. Range**	**Supply**	**Comments**	**Product**	**Page**
CTCSS Encoder	Tone Generator	67Hz - 250.3Hz	5 Volts	40 CTCSS tones; Frequency set by external parallel switch or link.	FX315	2 - 11
CTCSS Encoder/Decoder	Tone Detector and Generator	67Hz - 250.3Hz	3 - 5.5 Volts	Half-duplex operation; 39 (predictable) tones + Notone; µP compatible serial or parallel control interface; Separate, filtered voiceband path; Sub-audio bandstop and bandpass filters.	FX365C	2 - 17
Private Squelch Circuit	Scrambler; Tone Detector and Generator	67Hz - 250.3Hz	5 Volts	Half-duplex operation; Tone operated speech-inversion scrambler with pre- and de-emphasis; detects and generates 38 (predictable) tones + Notone; Serial or parallel data control; switched (Rx/Tx) voiceband paths.	FX375	2 - 25
Sub-Audio Signalling Processor	CTCSS + DCS Tone Detector and Generator	65Hz - 257Hz	5 Volts	Non-predictive CTCSS/DCS detector and generator; Serial "C-BUS" data control; Separate, (sub-audio bandstop) filtered voice path; adjustable Tx output level; Rx and Tx sub-audio filtering.	FX805	2 - 107
Sub-Audio Signalling Module	Intelligent CTCSS and DCS Signalling	62.5Hz - 250.3Hz	6 - 26 Volts	Generate and (non-predictive) detect 41 (CTCSS) sub-audio tones; Generate and (non-predictive) detect 104 DCS codes, with inversion; selective lock-out facility; Simple radio interface; User configurable; Voiceband filtering.	CM1482	2 - 165

Digitally Controlled Amplifier Arrays		Amplifiers whose gain can be adjusted by a microprocessor, hence removing the need for potentiometers. These amplifiers allow for adaptive adjustment of levels and audio volumes.			
Description	**Stages**	**Range**	**Comments**	**Product**	**Page**
Digitally Controlled Amplifier Array	7 + 1	±3dB (0.43dB steps) ±14dB (2.0dB steps)	Low noise, 5 volt amplifiers with serial control; Output mute function.	FX009A	7 - 9
Digitally Controlled 'Quad' Amplifier Array	3 + 1	±3dB (0.43dB steps) ±14dB (2.0dB steps)	Low noise, 5 volt amplifiers with serial control; Output mute function.	FX019	7 - 15
Digitally Controlled 'Dual' Amplifier Array	2 + 1	±48dB (2.0dB steps) component adjustable	Low noise, 5 volt amplifiers with selectable inputs and outputs under serial control; Output mute function. Low noise, 5 volt uncommitted amplifier.	FX029	7 - 21

Wireless Modems		Modem microcircuits providing a comprehensive range of data rates, modulation types and interfaces for serial and packet data applications.							
Description	**Data Rate**	**Duplex and Modulation**	**Systems and Specification**	**Carrier Detect Capability**	**Control and Data Type**	**Sync Detect**	**Supply**	**Product**	**Page**
MPT1327 FFSK Modem	1.2kb/s 1.2/2.4kb/s	Full-Duplex FFSK/MSK	MPT 1317/1327, General Purpose	Yes	Parallel Formatted	Yes SYNC/SYNT	5 Volts	FX429 FX429A	8 - 3
1200/2400/4800 Baud FFSK Modem	1.2/2.4/ 4.8kb/s	Full-Duplex FFSK/MSK	General Purpose	Yes	Serial Unformatted	No (Free Format)	5 Volts	FX469	8 - 23
FFSK Modem for Digital Selcall and Trunked Radio	1.2kb/s	Full-Duplex FFSK/MSK	PAA 1382, EBSS 1200 & General Purpose	Yes	Parallel Formatted	Yes SYNC/SYNT	5 Volts	FX529	8 - 17
Low-Voltage/ High-Speed GMSK Modem	4kb/s to 40kb/s	Full-Duplex GMSK	General Purpose	Yes (Rx Quality Report)	Serial Unformatted	No	3 - 5.5 Volts	FX589	8 - 31
FFSK Modem	1.2kb/s	Half-Duplex FFSK/MSK	PAA 1382, EBSS 1200 MPT 1327 & General Purpose	No	Serial Formatted	Yes (user selectable)	5 Volts	FX809	2 - 135
GMSK 'Packet Data' Modem	4kb/s to 19.2kb/s	Half-Duplex GMSK	Mobitex, General Purpose Packet Data	Yes (Rx Quality Report)	Parallel Formatted	Yes	5 Volts	FX909	8 - 47
4-Level FSK Modem	4.8/9.6/ 19.2kb/s	Half-Duplex 4-Level FSK	General Purpose	Yes (Rx Quality Report)	Parallel Formatted	Yes	5 Volts	FX919	8 - 81
4-Level FSK Modem for RD-LAP	9.6/19.2kb/s	Half-Duplex 4-Level FSK	RD-LAP (Modacom) (Ardis)	Yes (Rx Quality Report)	Parallel Formatted	Yes	5 Volts	FX929	8 - 111

STOP PRESS !

New Modems available for CDPD --- 19.2kb/s GMSK Modem and Half-Duplex low-cost GMSK Modem available shortly
Ask for CML Modem Product Review

Switched Capacitor Filters

Switched Capacitor Filters	A range of CML devices containing a large proportion of accessible audio filtering; Although used on specific systems, these microcircuits can be utilised by other applications having high accuracy filter requirements.

Description	Available Filtering	Filter Cutoff Frequency (Hz)	Filter Order	Supply	Comments	Product	Page
Voiceband Inverter	Audio Bandpass	273 - 2757 333 - 3370 300 - 3033	Tx Path 16th order Rx Path 32nd order	5 Volts	µP compatible; Fixed frequency inverter; choice of 3 bandwidths and inversion frequencies; Remote Private/Clear switching.	FX004	2 - 3
Duplex Frequency Inverter	2 x Lowpass 2 x Bandpass	3100 300 - 3000	10th order 14th order	3 - 5.5 Volts	2 Separate filter/inversion paths; 2 Fixed frequency inverters.	FX118	5 - 3
Audio Filter Array	Lowpass Lowpass + Highpass	3400 300 - 3400	6th order 6th order 4th order	5 Volts	Meets NMT, TACS and AMPS specs.; Uncommitted amplifier on-chip; Low group delay distortion; Enable facility.	FX306	3 - 3
NMT Filter Array	Lowpass SAT Bandpass	3400 4000 (±200Hz)	12 order 6th order	5 Volts	For NMT cellular radio; Uncommitted amplifier on-chip; Low group delay distortion; Enable facility.	FX316	3 - 9
Audio Bandpass Filter	Lowpass + Highpass	Selectable Bandwidths 882Hz to 13125Hz	6th order 4th order	5 Volts	A versatile (bandpass) filter array with pin and clock selectable frequency parameters; Uncommitted amplifier on-chip; Low group delay distortion; Enable facility.	FX326	7 - 35
R2000 Filter Array	Highpass Lowpass Data Bandpass	300 2550 148 (±50Hz)	8th order 4th order 6th order	5 Volts	For Radiocom 2000 cellular radio; Uncommitted amplifier and controllable analogue switch on-chip; Low group delay distortion; Enable facility.	FX336	3 - 15
CTCSS Encoder/Decode	Audio Highpass CTCSS	300 Selected Tone	6th order	3 - 5.5 Volts	CTCSS Encoder/Decoder with integral Rx/Tx voice path; Serial and parallel µP interface.	FX365C	2 - 17
AMPS/TACS Quad Filter Array	2 x Bandpass 2 x Lowpass	300 - 3000 3000	14th order 10th order	5 Volts	4 (2 x 2) separate filter paths; 4 separate 'input level' amps; For AMPS/TACS cellular radio systems; Path Enable facility.	FX366	3 - 21
Unifil® Analogue Processor	Custom -Notch -Bandpass -Lowpass -Highpass	Configurable Cut-offs 5kHz Max. 50Hz Min.	2nd order	5 Volts	A highly versatile audio processor to be user-configured as: Filters, Oscillators or Modems.	FX406	7 - 41

Switched Capacitor Filters		A range of CML devices containing a large proportion of accessible audio filtering. Although used on specific systems, these microcircuits can be utilised by other applications having high accuracy filter requirements.					
Description	**Available Filtering**	**Filter Cutoff Frequency**	**Filter Order**	**Supply**	**Comments**	**Product**	**Page**
Mobile Radio Audio Processor	Voiceband Audio Filters	Various (system specific)		5 Volts	A collection of filters and digitally controlled level devices forming a complete half-duplex audio system to CEPT standards; Pre and De-emphasis; High, Low and Bandpass; Selectable signal paths; Access to external audio processes available; Serial control.	FX506	2 - 35
PLMR Audio Processor	Voiceband Audio Filters			5 Volts	A collection of filters and digitally controlled level devices forming a complete half-duplex audio system which meets EIA and CEPT audio specs; Pre- and De-emphasis; High, Low and Bandpass; Selectable signal paths; Access to external audio processes available; Serial "C-BUS" control.	FX806A	2 - 123
NMT Audio Processor	Voiceband Audio Filters			5 Volts	A collection of filters and digitally controlled level devices forming a complete half-duplex audio system for use in the NMT equipment; Pre- and De-emphasis; High, Low and Bandpass; selectable signal paths; Access to external audio processes available; Serial "C-BUS" control.	FX816	3 - 39
TACS Audio Processor	Voiceband Audio Filters			5 Volts	A collection of filters and digitally controlled level devices forming a complete half-duplex audio system for use in TACS equipment; Pre- and De-emphasis; High, Low and Bandpass; selectable signal paths; Access to external audio processes available; Serial "C-BUS" control.	FX826	3 - 51
R2000 Audio Processor	Voiceband Audio Filters			5 Volts	A collection of filters and digitally controlled level devices forming a complete half-duplex audio for use in the R2000 system; Pre- and De-emphasis; High, Low and Bandpass; selectable signal paths; Access to external audio processes available; Serial "C-BUS" control.	FX836	3 - 63

Analogue-To-Digital Converters

Analogue-To-Digital Converters		Voiceband to digital conversion; 5 Volt requirement; Single-chip devices employing CVSD Codecs. Programmable and external sampling clocks; On-chip voiceband switched capacitor filters.				
Description	**Function**	**Control Interface**	**Duplex**	**Comments**	**Product**	**Page**
CVSD Codec	Encode and Decode	Input pins	Full	3 or 4-bit compand algorithm; Forced Idle facility; Multiplexing 'Enable' function.	FX609	9 - 17
'Eurocom' Delta Codec	Encode and Decode	Input pins	Full	3 or 4-bit compand algorithm; Forced Idle facility; Multiplexing 'Enable' function; Meets Eurocom D1-IA8 spec.	FX619	4 - 3
Military Delta Codec	Encode and Decode	Input pins	Full	3 or 4-bit compand algorithm; Forced Idle facility; Multiplexing 'Enable' function; Meets Mil-Std-188-113 spec.	FX629	4 - 13
VSR Codec	Encode and Decode with Voice Store/Replay	Parallel µC	Half	Selectable voiceband filtering; 'Average Signal Level' indication; Voice Store and Replay controls; 'Page Position' locator.	FX709	9 - 23
DVSR Codec	Encode and Decode with Voice and Data Store/Replay	Serial "C-BUS" µC	Full	Data store and replay; Voice store and replay; DRAM interface; 'Average Signal Level' indication; Compatible with CML DBS 800 system for mobile radio.	FX802	2 - 77
VSR Codec	Encode and Decode with Voice Store/Replay	Serial "C-BUS" µC	Half	Voice store and replay; DRAM interface; 'Average Signal Level' indication; Compatible with CML DBS 800 system for cellular radio.	FX812	3 - 27

Audio Privacy (Scrambling)			Analogue scramblers operate directly on the input audio; Digital signal devices provide privacy by the transmission of a digital 'voice' signal, however for more secure communications the digital signal can be interleaved and/or scrambled by a logic function; On-chip voicband filters as appropriate.		
Description	**Function**	**Type of Privacy**	**Comments**	**Product**	**Page**
Voiceband Inverter	Analogue Scrambling	Fixed Frequency Inversion	A half-duplex scrambler with 3 selectable audio bandwidths and inversion frequencies; High order filtering; Clear/private switching by local or remote (tone) control; Serial or parallel device control; 5 volt requirement.	FX004	2 - 3
Duplex Frequency Inverter	3 Volt Analogue Scrambling	Fixed Frequency Inversion	2 separate channels providing a full-duplex audio scrambler; Lowpass and bandpass filters; Component configurable input level adjustment; 3 volt requirement.	FX118	5 - 3
VSB Scrambler	Analogue Scrambling	Variable Split-Band Inversion	A half-duplex scrambler with up to 32 programmable split frequencies; Voice paths with voiceband filters; Serial or parallel control; Fixed or rolling-code operation; Clear/Private switching; 5 volt requirement.	FX214 FX224	9 - 3
Private Squelch Circuit	Analogue Scrambling	Fixed Frequency Inversion	Half-duplex scrambler; Tone operated speech-inversion with pre- and de-emphasis; detects and generates 38 (predictable) tones + Notone; Serial or parallel data control; switched (Rx/Tx) voiceband paths; 5 volt requirement.	FX375	2 - 25
CVSD Codec	Encode/Decode	Digital Signal	A full-duplex delta modulation codec with 3 or 4-bit compand algorithm; forced Idle facility and output Enable control; 5 volt requirement.	FX609	9 - 17
'Eurocom' Delta Codec	Encode/Decode	Digital Signal	A full-duplex delta modulation codec with 3 or 4-bit compand algorithm; forced Idle facility and output Enable control; 5 volt requirement.	FX619	4 - 3
Military Delta Codec	Encode/Decode	Digital Signal	A full-duplex delta modulation codec with 3 or 4-bit compand algorithm; forced Idle facility and output Enable control; 5 volt requirement.	FX629	4 - 13
VSR Codec	Encode/Decode with Voice Store/Replay	Digital Signal	A half-duplex delta modulation codec with 3 or 4-bit compand algorithm; forced Idle facility and output Enable control; Parallel µControlled voice store and replay facilities on chip; 'Average Signal Level' indication; 5 volt requirement.	FX709	9 - 23
DVSR Codec	Encode/Decode with Voice and Data Store/Replay	Digital Signal	A full-duplex delta modulation codec; forced Idle facility and output Enable control; Serial µControlled voice and data store and replay facilities on chip; DRAM interface.	FX802	2 - 77
VSR Codec	Encode/Decode with Voice Store/Replay	Digital Signal	A half-duplex delta modulation codec; forced Idle facility and output enable control; Serial µControlled voice store and replay facilities on chip; DRAM interface; 5 volt requirement.	FX812	3 - 27

Integrated Circuits Data Book

Section 1

Product Selection by Market Application

STOP PRESS

NEW PRODUCTS Available Shortly

- **CDPD/AMPS Cellular Wireless Data - 19.2kb/s GMSK Modem and AMPS Processor**
- **CDPD - Data Modem with CDPD Data Processing**
- **Half-Duplex Low-Cost GMSK Modem**
- **Caller Line Indentification to UK Specifications**

2-Way Mobile Radio

2-Way Mobile Radio	CML products currently promoted and employed within Mobile Radio Systems worldwide.				
Description	**Primary Function**	**Control and Supply**	**Comments**	**Product**	**Page**
Voiceband Inverter	Analogue Scrambling	Serial/Parallel 5 Volts	A half-duplex voiceband inverter controlled either locally or by a remote pilot tone; High order bandpass audio and tone filtering; Rx/Tx path switching; PTL function.	FX004	2 - 3
CTCSS Encoder	Sub-Audio Tone Generation	Parallel Pin/Link 5 Volts	A sub-audio tone encoder capable of up to 40 CTCSS frequencies (67-250.3Hz); Output enable control; sinewave output.	FX315	2 - 11
Low-Voltage CTCSS Encoder/Decoder	Sub-Audio Tone Detection and Generation	Serial/Parallel µC 3 Volts	A sub-audio tone encoder and decoder capable of up to 39 CTCSS frequencies (67-250.3Hz); CTCSS output enable control; sinewave output; Separate (remote switched) half-duplex voice (highpass - CTCSS reject) audio path; Rx tone detect indication. Meets MPT1306 and EIA-220B specs.	FX365C	2 - 17
Private Squelch Circuit	Analogue Scrambling	Serial/Parallel µC 5 Volts	A fixed frequency speech inversion scrambler with CTCSS tone operated Private/Clear switching; Half-duplex voice audio (300-3033Hz) path; Pre- and de-emphasis and bandpass filtering; 38 programmable sub-audio tones; PTL function.	FX375	2 - 25
Mobile Radio Audio Processor	Audio Processing	Serial µC 5 Volts	A complete half-duplex voiceband, data and signalling audio processor; Contains, on chip, the following processes: de-emphasis, pre-emphasis, deviation limiter, high order voiceband filters, VOGAD (compressor) and a signal detect (squelch system); all system levels set by digital control. Filters meet CEPT standards.	FX506	2 - 35
Audio Processing and Signalling Chip-Set	Voice - Sub-Audio - In-Band - Data -	Serial µC "C-BUS" 5 Volts	A complete voiceband, audio and sub-audio signalling and data chip set, available as individual functional units on a CML proprietary 3-line serial "C-BUS" control bus; FX802; FX803; FX805; FX806A; FX809;	DBS 800 Chipset	2 - 51
DVSR Codec	Delta Codec with Voice and Data Store/Replay	Serial µC "C-BUS" 5 Volts	A DBS 800 microcircuit: A full-duplex CVSD codec with on-chip voiceband filters; Speech store and replay; Data store and replay; On-chip DRAM control and timing; Input power assessement; Control commands can be buffered.	FX802	2 - 77

2-Way Mobile Radio		CML products currently promoted and employed within Mobile Radio Systems worldwide.			
Description	**Primary Function**	**Control and Supply**	**Comments**	**Product**	**Page**
Audio Signalling Processor	Audio Tone Signalling	Serial µC "C-BUS" 5 Volts	A DBS 800 microcircuit: A full-duplex inband tone encoder and decoder; Signalling systems supported include: selcall (CCIR, ZVEI, EEA and 2-tone) and DTMF encode; On-chip signal summing amplifier.	FX803	2 - 91
Sub-Audio Signalling Processor	Sub-Audio Tone Signalling	Serial µC "C-BUS" 5 Volts	A DBS 800 microcircuit: A half-duplex sub-audio microcircuit; A non-predictive CTCSS tone decoder and DCS demodulator; A CTCSS/DCS tone encoder with digital Tx level adjustment; Voiceband path with sud-audio bandstop filter.	FX805	2 - 107
Audio Processor	Audio Processing	Serial µC "C-BUS" 5 Volts	A DBS 800 microcircuit: A half-duplex audio processor with voicband filters, pre- and de-emphasis; Deviation limiting; VOGAD (compressor); Inputs from external audio (voice, sub-audio, scrambling, tone and data) processes; Digital control of path level setting; Controlled two-point modulation and LS audio outputs.	FX806A	2 - 123
FFSK Modem	1200 Baud Data Transfer	Serial µC "C-BUS" 5 Volts	A DBS 800 microcircuit: A half-duplex 1200 baud serial data FFSK/MSK modem; Checksum generation and error checking in accordance with MPT1327; Custom system SYNC operations; Uncommitted Op-Amp on chip.	FX809	2 - 135
Computer Aided Despatching Module	Radio Signalling PC Expansion Card	Standard ISA Expansion	An expansion card providing total base station control by the PC; 5/6 tone selcall encode/decode for all recognised tonesets; 2-tone encode; 1200 baud FFSK encode/decode; separate Rx/Tx tone, data and voice paths; morse 'station ID' output.	CM10	2 - 149
Non-Predictive Selcall Module	Inband Signalling	6 - 26 Volts	A compact 5- or 6-tone CCIR, EEA and ZVEI selcall module with individual address encoding, non-predictive all-tone decoding, transponding and full, all-system GROUP Call and ANI capabilities.	CM1481	2 - 161
CTCSS + DCS Signalling Module	Sub-Audio Signalling Module	6 - 26 Volts	An intelligent non-predictive CTCSS and DCS encoder/decoder module for mobile and portable radios; will encode and decode any one of 41 sub-audio tones and 104 DCS codes.	CM1482	2 - 165

Cellular Radio

Cellular Radio		CML products currently promoted and employed within analogue Cellular Radio Systems worldwide.			
Description	**Primary Function**	**Control and Supply**	**Comments**	**Product**	**Page**
Digitally Controlled Amplifier Array	Remote Adaptive Level Control	Serial Data 5 Volts	Eight low-noise amplifiers with serial control and output mute function; 7 with ±3dB range (0.43dB steps); 1 with ±14dB range (2.0dB steps).	F009A	7 - 9
Digitally Controlled 'Quad' Amplifier Array	Remote Adaptive Level Control	Serial Data 5 Volts	Four low-noise amplifiers with serial control and output mute function; 3 with ±3dB range (0.43dB steps); 1 with ±14dB range (2.0dB steps).	FX019	7 - 15
VSR Codec	Voice Storage and Replay	Serial µP 5 Volts	Compatible with FX816, FX826 and FX836 cellular audio processors; Half-duplex voice store and retreive CVSD codec; Digitises and stores voice data in external DRAM; Recovers voice data from external DRAM and replays as audio; On-chip DRAM controller; Selectable sample rates and memory size.	FX812	3 - 27
NMT System Audio Processor	Voiceband and Signalling	Serial µP 5 Volts	For NMT applications. A full-duplex speech and signalling processing array: Tx/Rx/SAT filtering and digitally controlled gain. VOGAD. Pre-/de-emphasis. Deviation limiter; VSR and data compatible; Separate SAT channel; Single modulation output.	FX816	3 - 39
AMPS/TACS System Audio Processor	Voiceband and Signalling	Serial µP 5 Volts	For AMPS and TACS applications. A full-duplex speech and signalling processing array: Tx/Rx/SAT filtering and digitally controlled gain. Pre-/de-emphasis. Deviation limiter; VSR and data compatible; Separate SAT channel; Single modulation output.	FX826	3 - 51
R2000 System Audio Processor	Voiceband and Signalling	Serial µP 5 Volts	For AMPS and TACS applications. A full-duplex speech and signalling processing array: Tx/Rx/SAT filtering and digitally controlled gain. Pre-/de-emphasis. Deviation limiter; VSR and data compatible; Separate SAT channel; Single modulation output.	FX836	3 - 63

Wireless Data Comms	Modem microcircuits providing a comprehensive range of data rates, modulation types and interfaces for serial and packet data applications.								
Description	**Data Rate**	**Duplex and Modulation**	**Systems and Specification**	**Carrier Detect Capability**	**Control and Data Type**	**Sync Detect**	**Supply**	**Product**	**Page**
MPT1327 FFSK Modem	1.2kb/s 1.2/2.4kb/s	Full-Duplex FFSK/MSK	MPT 1317/1327, General Purpose	Yes	Parallel Formatted	Yes SYNC/SYNT	5 Volts	FX429 FX429A	8 - 3
1200/2400/4800 Baud FFSK Modem	1.2/2.4/ 4.8kb/s	Full-Duplex FFSK/MSK	General Purpose	Yes	Serial Unformatted	No (Free Format)	5 Volts	FX469	8 - 23
FFSK Modem for Digital Selcall and Trunked Radio	1.2kb/s	Full-Duplex FFSK/MSK	PAA 1382, EBSS 1200 & General Purpose	Yes	Parallel Formatted	Yes SYNC/SYNT	5 Volts	FX529	8 - 17
Low-Voltage/ High-Speed GMSK Modem	4kb/s to 40kb/s	Full-Duplex GMSK	General Purpose	Yes (Rx Quality Report)	Serial Unformatted	No	3 - 5.5 Volts	FX589	8 - 31
FFSK Modem	1.2kb/s	Half-Duplex FFSK/MSK	PAA 1382, EBSS 1200 MPT 1327 & General Purpose	No	Serial Formatted	Yes (user selectable)	5 Volts	FX809	2 - 135
GMSK 'Packet Data' Modem	4kb/s to 19.2kb/s	Half-Duplex GMSK	Mobitex, General Purpose Packet Data	Yes (Rx Quality Report)	Parallel Formatted	Yes	5 Volts	FX909	8 - 47
4-Level FSK Modem	4.8/9.6/ 19.2kb/s	Half-Duplex 4-Level FSK	General Purpose	Yes (Rx Quality Report)	Parallel Formatted	Yes	5 Volts	FX919	8 - 81
4-Level FSK Modem for RD-LAP	9.6/19.2kb/s	Half-Duplex 4-Level FSK	RD-LAP (Modacom) (Ardis)	Yes (Rx Quality Report)	Parallel Formatted	Yes	5 Volts	FX929	8 - 111

STOP PRESS !

New Modems available for CDPD --- 19.2kb/s GMSK Modem and Half-Duplex low-cost GMSK Modem available shortly
Ask for CML Modem Product Review

Military Comms		Versatile delta modulation codecs to meet specific military specifications.			
Description	**Primary Function**	**Control and Supply**	**Comments**	**Product**	**Page**
'Eurocom' Delta Codec	Analogue to Digital and Digital to Analogue Conversion	Input Pin 5 Volts	To meet Eurocom D1-IA8. A full-duplex CVSD codec; On-chip voiceband input and output filters; Programmable sampling clocks; 3- or 4-bit compand algorithm; Forced Idle facility; Chip Enable function.	FX619	4 - 3
'Military' Delta Modulation Codec	Analogue to Digital and Digital to Analogue Conversion	Input Pin 5 Volts	To meet Mil-Std-188-113. A full-duplex CVDSD codec; On-chip voiceband input and output filters; Programmable sampling clocks; 3- or 4-bit compand algorithm; Forced Idle facility; Chip Enable function.	FX629	4 - 13

Cordless Telephones		Low-power duplex scrambling device for analogue cordless telephone systems.			
Description	**Primary Function**	**Control and Supply**	**Comments**	**Product**	**Page**
Duplex Frequency Inverter	Voiceband Scrambling	Input Pin 3 Volts	Two separate voiceband frequency inversion channels each with input and output voiceband filtering and fixed frequency balanced modulator; Component adjustable input op-amp;	FX118	5 - 3

Telecoms		A range of call charge, call progress and voice and signal handling products for telecoms applications.			
Description	**Primary Function**	**Control and Supply**	**Comments**	**Product**	**Page**
Universal Call Progress Decoder	Audio Tone Decoder	Serial µP Output 3 Volts	A wide-band 'N-tone' non-predictive 'call progress' tone decoder; Range 300Hz to 2,150Hz; Analogue in / 6-bit serial data out; Speech discrimination capability; Chip select facility; used to detect call progress,'dial', 'busy' and Fax/modem tones.	FX613	6 - 3
Call Progress Decoder	Custom Audio Tone Decoder	Parallel µP Output 3 Volts	A wide-band predictive 'call progress' tone decoder; 13 popular 'telephone progress' tones in the range 300Hz to 2,150Hz; Analogue in / 4-bit parallel data out; Speech discrimination capability; Chip select facility; used to detect call progress,'dial', 'busy' and Fax/modem tones.	FX623	6 - 11
Low-Voltage SPM Detector	12KHz and 16kHz Tone Detector	Serial Logic Output 3 Volts	12kHz and 16kHz system selectable; Component adjustable input level thresholds; Tone Follower and Cumulative Tone logic level outputs; High speechband rejection properties; used to detect telephone call charge metering pulses.	FX631	6 - 17
Dual SPM Detector	Two 12KHz and 16kHz Tone Detectors	Serial µP 5 Volts	Two detectors on a single chip; 12kHz and 16kHz system selectable Serial data or component-adjustable threshold level control; Tone Follower and Cumulative Tone logic level or high Z outputs; ideal for 2-line/card PABX applications.	FX641	6 - 25

STOP PRESS !
Caller Line Identification to UK Specifications available shortly

Voice Security and Voice Coding

Voice Security / Voice Coding		Analogue scramblers operate directly on the input audio; Digital signal devices provide privacy by the transmission of a digital 'voice' signal provided by a voice codec, however for a more secure communication the digital signal can be interleaved and/or scrambled by a logic function.			
Description	**Primary Function**	**Control and Supply**	**Comments**	**Product**	**Page**
Duplex Frequency Inverter	Analogue Scrambling	Input Pin 3 - 5.5 Volts	Two separate voiceband frequency inversion channels each with input and output voiceband filtering and fixed frequency balanced modulator; Component adjustable input op-amp.	FX118	5 - 3
VSB Scrambler	Analogue Scrambling	Serial or Parallel 5 Volts	VSB = Variable Split-Band. A half-duplex scrambler with up to 32 programmable split frequencies; Voice paths with voiceband filters; Serial or parallel control; Fixed or rolling-code operation; Clear/Private switching.	FX214 FX224	9 - 3
CVSD Codec	Analogue to Digital and Digital to Analogue Conversion	Input Pin 5 Volts	A full-duplex CVSD codec; On-chip voiceband input and output filters; Programmable sampling clocks; 3- or 4-bit compand algorithm; Forced Idle facility; Chip Enable function.	FX609	9 - 17
VSR Codec	Encode/Decode with Voice Store/Replay	Parallel 5 Volts	A half-duplex delta modulation codec with 3 or 4-bit compand algorithm; forced Idle facility and output Enable control; Parallel µControlled voice store and replay facilities on chip; 'Average Signal Level' indication.	FX709	9 - 23

General Purpose Applications		Products which have many and varied uses in all aspects of the electronics industry.			
Description	**Primary Function**	**Control and Supply**	**Comments**	**Product**	**Page**
Signal-to-Noise Enhancer	Audio Band Signal Improvement	Logic Output 2.5 - 5.5 Volts	Extracts single periodic signals from high random noise environments; Up to 8.5dB signal-to-noise improvement; Input range: 17Hz to 13kHz; Analogue in / logic out.	FX002	7 - 3
Digitally Controlled Amp Array	Eight Digitally Controlled Gain Blocks	Serial 5 Volts	7 'amplifiers' with a ±3dB range in 0.43dB steps; 1 'amplifier' with a ±14dB range in 2dB steps; Output mute function.	FX009A	7 - 9
Digitally Controlled Quad Amp Array	Four Digitally Controlled Gain Blocks	Serial 5 Volts	3 'amplifiers' with a ±3dB range in 0.43dB steps; 1 'amplifier' with a ±14dB range in 2dB steps; Output mute function.	FX019	7 - 15
Dual Digitally Controlled Amp	Two Digitally Controlled Gain Blocks	Serial 5 Volts	2 'amplifiers' with a ±48dB range in 2dB steps; Each with selectable inputs and outputs; 1 separate component-adjustable 'amplifier 'stage; Mute function.	FX029	7 - 21
Tone Detector	Audio Frequency Detector	10 - 15 Volts	Range 40Hz to 5kHz;Tone frequencies and bandwidths are set by external components.	FX105P	7 - 27
Audio Bandpass Filter	Programmable Bandpass Filter	Parallel Pin 5 Volts	Pin and clock selectable frequency parameters (bandwidths from 882Hz to 13125Hz); Uncommitted amplifier on-chip; Low group delay distortion; Enable facility.	FX326	7 - 35
Analogue Processor	Frequency Detector and Generator	Pin/Component 5 Volts	Versatile "Unifil®" device; Frequency set by components or clock input; Configurable to lowpass, highpass, bandpass, bandstop and notch filters, FSK and PSK modems, Sine/Square generators; tracking filters and oscillators.	FX406	7 - 41
VSR Codec	Encode/Decode with Voice Store/Replay	Parallel 5 Volts	A half-duplex delta modulation codec with 3 or 4-bit compand algorithm; forced Idle facility and output Enable control; Parallel µControlled voice store and replay facilities on chip; 'Average Signal Level' indication.	FX709	9 - 23

Other CML Products

Other CML Product Items		Products that are in production but not detailed in this publication. Please contact Consumer Microcircuits Limited or your local distributor (Section 12) for further information.					
Product	**Description**	**Market Application**	**Comments**	**Product**	**Description**	**Market Application**	**Comments**
FX003	Selcall Decoder	PMR	FX803 is a similar replacement	**FX365**	CTCSS Encoder/Decoder	PMR	FX365C is a similar replacement
FX009	Digitally Controlled Amp Array	General Purpose	FX009A is a similar replacement	**FX419**	FFSK Modem	Datacoms	FX469 is a similar replacement
FX102	Selcall Decoder	PMR	FX002 is a similar replacement	**FX439**	FFSK Modem	Datacoms	FX469 is a similar replacement
FX203	Selcall Tone Codec	PMR	FX803 is a similar replacement	**FX503**	Selcall Encoder	PMR	FX803 is a similar replacement
FX304	C-Net Audio Processor	Cellular	FX108 is a similar replacement	**FX601**	Tone Operated Switch	General Purpose	
FX309	CVSD Codec	Datacoms	FX609 is a similar replacement	**FX611**	12kHz/16kHz SPM Detector	Telecoms	FX631 is a similar replacement
FX335	CTCSS Encoder/Decoder	PMR	FX365C is a similar replacement	**FX621**	Low-Power SPM Detector	Telecoms	FX631 is a similar replacement
FX346	AMPS/TACS/ NMT Audio Processor	Cellular	FX816 is a similar replacement				

CML Publications

Details of CML products and their applications are provided by the following publications:

Product Information Publications
The Data Sheet; individual multi-page documents containing technical information, specifications and explanations to enable the product user to embody and operate a particular device within its final application. Each publication eventually forms part of the CML Integrated Circuits Data Book at its next due publication date. The technical status of these documents is governed by CML Data Classification (see below).

Integrated Circuits Shortform Catalogue
A short descriptive list of all current CML products and their suggested applications.

Product Review
A promotional document providing brief information on a specific group of products.

Integrated Circuits Data Book
This document; a complete collation of all current data sheets and applications. This document, when published, will supersede individual data sheets.

CML Data Classification

The product data published in both Product Information Publications (data sheets) and the Integrated Circuits Data Book is classified technically as described in the table below.
The data classification "printed identifier" can be found immediately below the individual publication number printed on the front page of each data sheet.

Data Status	Printed Identifier	Explanation
Advance	"Advance"	Data relevant to a product that is still in its development stages. Function, operation and operating parameters have not been proven.
Provisional	"Provisional Issue"	Specified limits described are based upon currently incomplete batch testing and product evaluation and may change. Device operation and function will not change.
Full	No printed identifier	Specification limits are guaranteed and will not change except through officially accepted change procedures.

CML Microcircuit Package Information

Package Suffixes

CML package styles are currently identified with the following suffixes: J, LG, LH, LS and P.
To make this system more explanatory, new identifier suffixes are being introduced to all NEW CML products.
For an undetermined period both current and new identifiers will be used in publications where relevant. The table below explains the old and new nomenclature:

Package Information	PLCC - Plastic Leaded Chip Carrier. TQFP - Thin Quad Plastic Flatpack. SOIC - Small Outline Integrated Circuit. PDIP - Plastic Dual In Line.						
Number of Pins	**Material**	**Package Type**	**Package Style**	**Lead Style**	**Current Product Suffix**	**New Product Suffix**	**Page**
24	Plastic	PLCC	Quad	Gull	LG	L1	10.6
24	Plastic	PLCC	Quad	Hook	LS	L2	10.5
28	Plastic	PLCC	Quad	Hook	LH	L3	10.5
48	Plastic	TQFP	Quad	Gull		L4	10.5
28	Ceramic	CLCC	Quad	Hook	M1		10.7
28	Plastic	SOIC	DIL	Gull	DW	D1	10.3
24	Plastic	SOIC	DIL	Gull	DW	D2	10.3
20	Plastic	SOIC	DIL	Gull	DW	D3	10.3
16	Plastic	SOIC	DIL	Gull	DW	D4	10.3
14	Plastic	PDIP	DIL	Thro' Hole	P	P2	10.6
16	Plastic	PDIP	DIL	Thro' Hole	P	P3	10.6
24	Plastic	PDIP	DIL	Thro' Hole	P	P4	10.6
14	Ceramic	Cerdip	DIL	Thro' Hole	J	J1	10.5
16	Ceramic	Cerdip	DIL	Thro' Hole	J	J2	10.4
22	Ceramic	Cerdip	DIL	Thro' Hole	J	J3	10.4
24	Ceramic	Cerdip	DIL	Thro' Hole	J	J4	10.4
28	Ceramic	Cerdip	DIL	Thro' Hole	J	J5	10.4

CML microcircuit package mechanical diagrams with dimensions are now available in Section 10 of this Data Book; basic form illustrations of the relevant packages are provided on the back page of each individual data sheet.

Integrated Circuits Data Book

Section 2

Two-Way Mobile Radio

CML Semiconductor Products

PRODUCT INFORMATION

FX004

Voice Band Inverter

Publication D/004/4 July 1994

Features/Applications

- Fixed Frequency Inversion
- CTCSS Compatible
- Choice of Three Audio Bandwidths and Inversion Frequencies
- μP Compatible Interface
- Automatic Private/Clear Switching
- Private Mobile Radio
- Community Repeaters
- Interconnect Systems
- Cordless Telephones
- Telephony

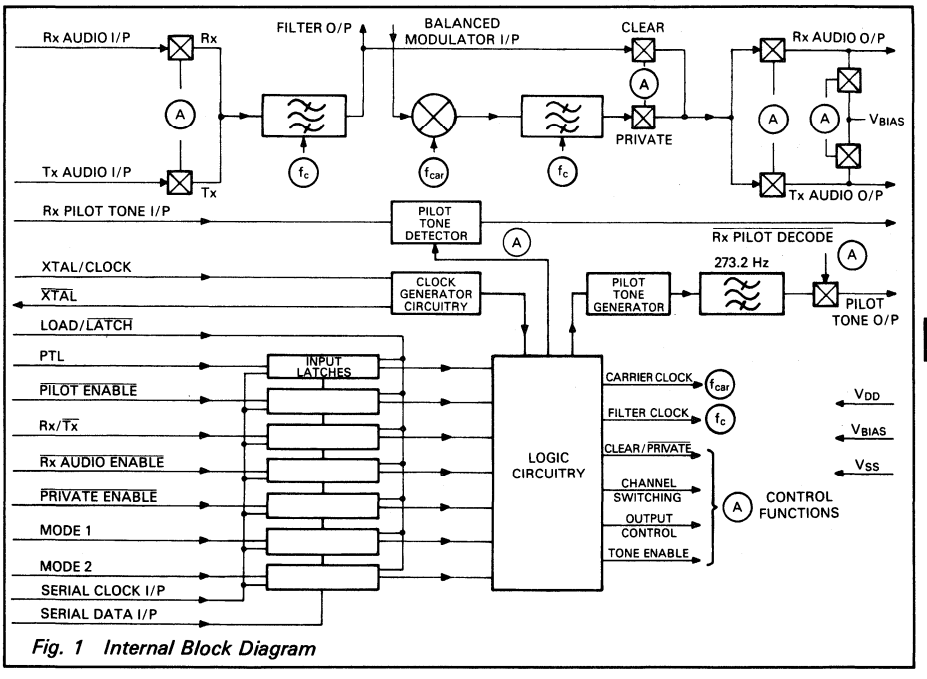


Fig. 1 Internal Block Diagram

FX004

Brief Description

The FX004 is designed to protect speech privacy in Private Mobile Radio and other common channel radio systems. It uses "FIXED FREQUENCY INVERSION" techniques which exchange the low and high frequencies of the transmitted voiceband signal to render the message unintelligible to eavesdropping.

Sharp cut-off in the internal voiceband filters permits operation with CTCSS and similar sub-audio signalling schemes and ensures the high quality of the recovered audio. The device incorporates a programmable clock divider which controls the carrier frequency and filter cut-off frequencies, thus permitting the selection of one of three scrambling codes and transmission bandwidths. A pilot tone generator and detector are used to operate the automatic clear/private facility in mixed equipment systems. Control of the Rx/$\overline{\text{Tx}}$, PTL and privacy functions is by pin selection or use of serial/parallel microprocessor interfaces.

The FX004 operates from a single 5V supply and uses a 1MHz crystal oscillator to ensure correct pitch of the recovered speech. Signal coupling and supply decoupling are the only external components needed and a choice of DIL or SMD packages is available.

Pin Number FX004 J and LG	Function
1	**Filter Output:** This is the audio bandpass filtered signal and is coupled externally to the Balanced Modulator Input pin via capacitor C_6. See Figure 2.
2	**Load/$\overline{\text{Latch}}$:** This pin is used for controlling input latches in both parallel and serial loading modes. In parallel, a logic '1' makes the latches transparent and the following inputs operate directly: PTL, Pilot Enable, Rx/Tx, Rx Audio Enable Private Enable, Mode 1 and Mode 2. When a logic '0', the data present is latched in. During serial loading Load/Latch should be kept low until data is completely loaded then the pin strobed 0 - 1 - 0, latching the new data in. Internal 1 MΩ pullup. See Figure 4.
3	**PTL:** A logic '1' level at this input enables the Audio Output in Rx mode when Rx Audio Enable is at a logic '1'. This feature enables channel checking without intercepting a private conversation. Internal 1MΩ pullup.
4	**$\overline{\text{Pilot Enable}}$:** A logic '0' at this input enables the 273.2Hz pilot tone at the Tx Pilot Tone Output when in Tx mode. Internal 1 MΩ pullup.
5	**Rx/$\overline{\text{Tx}}$:** This input selects the receive or transmit operating mode. Logic '1' is Rx, logic '0' is Tx. Internal 1 MΩ pullup.
6	**$\overline{\text{Rx Audio Enable}}$:** A logic '0' at this input enables the Rx audio path in Rx mode. May be connected to a CTCSS decoder. Internal 1 MΩ pullup.
7	**$\overline{\text{Private Enable}}$:** This input controls the input action of the balanced modulator by switching the carrier clock (refer to Table 1). When audio signals are inverted the signal path gain is adjusted automatically to compensate for upper sideband loss. Internal 1 MΩ pullup. For an 'auto-clear' function this input should be connected to the Rx Pilot Decode pin via external integrating components R_2 and C_9. See Figure 2.
8	**Mode 1:** These two inputs control the audio band frequency, carrier frequency and loading control mode. Internal 1 MΩ pullups. See Table 2.
9	**Mode 2:**
10	**Rx Pilot Tone Input:** This pin is the input to the Rx pilot tone decoder. Signals should be ac coupled. See Figure 2. The tone decoder is disabled in the Tx mode.
11	**Rx Audio Input:** This is the audio input pin in Rx mode. Signals should be ac coupled. See Figure 2.

Pin Number FX004 J and LG	Function
12	**V_{SS}:** Negative supply (GND).
13	**Tx Audio Input:** This is the audio input pin in Tx mode (mic). Signals should be ac coupled. See Figure 2.
14	**Rx Audio Output:** This is the audio output in Rx mode, internally biased at $V_{DD}/2$ in Tx mode.
15	**Tx Audio Output:** This is the audio output in Tx mode, internally biased at $V_{DD}/2$ when Rx mode is selected.
16	**Tx Pilot Tone Output:** This pin outputs the 273.2Hz pilot tone and would normally be summed with the Tx Audio Output to modulate the transmitter. When not enabled or in Rx this output is open circuit (high-impedance).
17	**$\overline{\text{Rx Pilot Decode}}$:** This pin is the output of the pilot tone detector, it outputs a logic '0' when a valid 273.2Hz tone is input. Has high impedance load to V_{DD} for wired 'OR' connection to other pins. For an 'Auto-Clear' function this input should be connected to the Private Enable pin via external integrating components R_2 and C_9, see Figure 2.
18	**V_{BIAS}:** This is the bias pin and is set internally to $V_{DD}/2$. It should be externally decoupled using a capacitor of 1.0µF (minimum) to V_{SS}. See Figure 2.
19	**Serial Data Input:** Data present at this input is clocked into the input register by the '0 - 1' clock transition of the Serial Clock Input. See Figure 4. Internal 1MΩ pullup.
20	**Serial Clock Input:** The timing clock pulses for serial loading are input here. Internal 1MΩ pullup.
21	**$\overline{\text{Xtal}}$:** Output of the clock oscillator inverter.
22	**Xtal/Clock:** This is the input of the clock oscillator inverter. 1MHz Xtal input or externally derived clock can be injected into this input.
23	**V_{DD}:** Positive supply. A single +5V power supply is required.
24	**Balanced Modulator Input:** This pin should be connected to the Filter Output pin via capacitor C_6, see Figure 2. It is internally biased at $V_{DD}/2$.

External Conditions

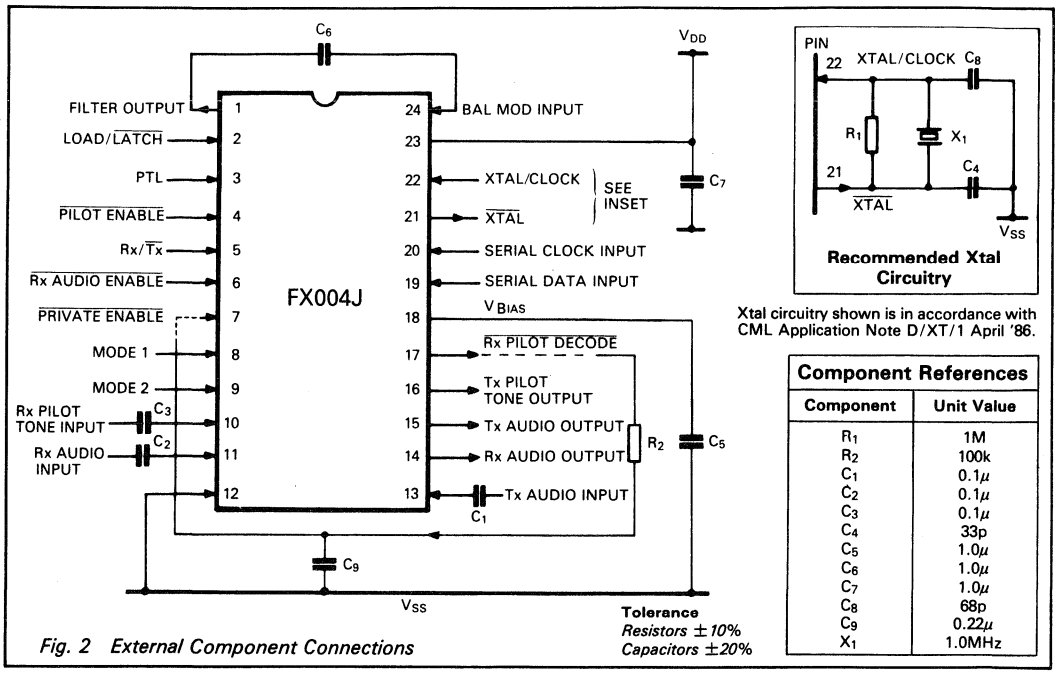


Fig. 2 External Component Connections

Xtal circuitry shown is in accordance with CML Application Note D/XT/1 April '86.

Component References

Component	Unit Value
R_1	1M
R_2	100k
C_1	0.1μ
C_2	0.1μ
C_3	0.1μ
C_4	33p
C_5	1.0μ
C_6	1.0μ
C_7	1.0μ
C_8	68p
C_9	0.22μ
X_1	1.0MHz

Private Enable (Auto-Clear)

To minimise the effect of noise and signal strength fluctuations on the 'Auto-Clear' function, the use of external integrating components between the Rx Pilot Decode output and the Private Enable input is required. Components R_2 and C_9, having a time constant of 20ms are recommended, as shown in figure 2.

Audio Quality

If it is necessary to install the FX004 Voice Band Inverter before the transmitter's existing pre-emphasis stage, an additional pre-emphasis stage before the FX004 followed by a de-emphasis stage after the FX004 will enhance the audio quality. At the receiver the FX004 should be installed between the demodulator and existing de-emphasis stage.

Input and Output Pin Conditions

Rx/$\overline{Tx}$	PTL	Private Enable	Pilot Enable	Rx Audio Enable	Assumed Rx I/P	Tx I/P	Rx O/P	Tx O/P	Tx Pilot O/P
1	0	X	X	1	X	X	$V_{DD}/2$	$V_{DD}/2$	O/C
1	1	X	X	1	Signal	X	Non Inverted	$V_{DD}/2$	O/C
1	X	0	X	0	Frequency Inverted	X	Clear (Passband Invert)	$V_{DD}/2$	O/C
1	X	1	X	0	Clear	X	Clear	$V_{DD}/2$	O/C
0	X	1	1	X	X	Signal	$V_{DD}/2$	Clear (Passband Non-Invert)	O/C
0	X	1	0	X	X	Signal	$V_{DD}/2$	Clear (Passband Non-Invert)	Tone
0	X	0	0	X	X	Signal	$V_{DD}/2$	Inverted (Passband Invert)	Tone
0	X	0	1	X	X	Signal	$V_{DD}/2$	Inverted (Passband Invert)	O/C

Table 1 Control Truth Table (X = don't care)

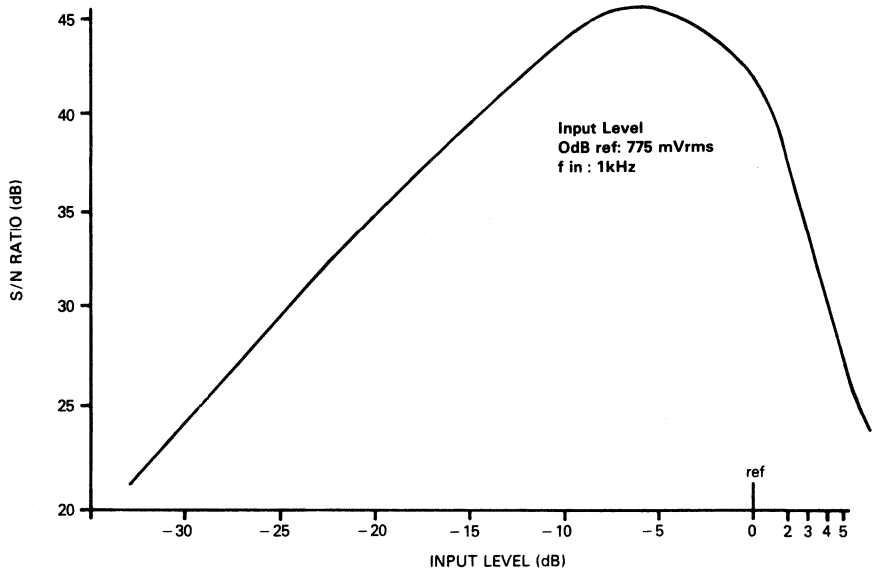
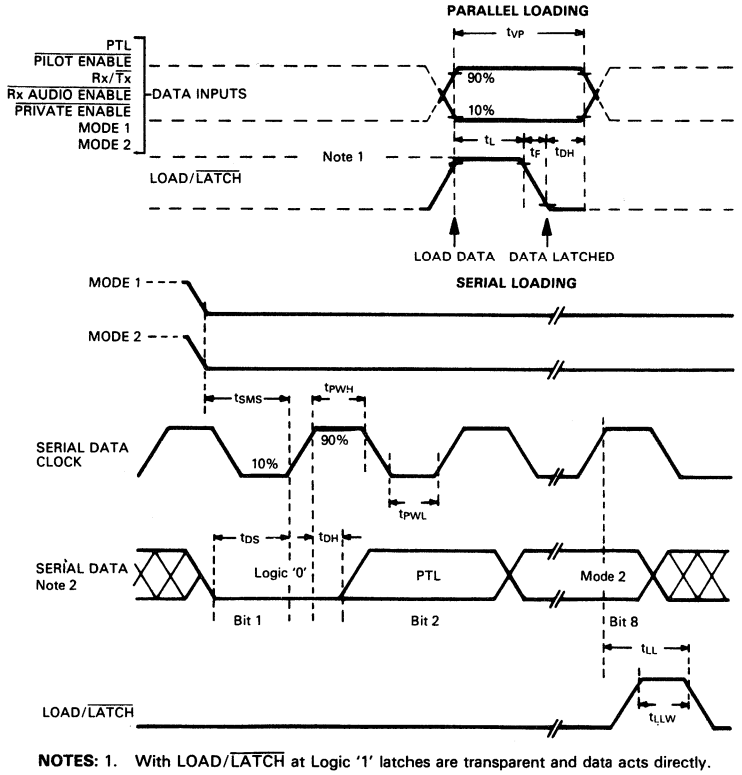


Fig. 3 Typical S/N Ratio Vs Input Level



Timing

t_{VP}	200ns Min.
t_L	150ns Min.
t_F	50ns Max.
t_{DH}	50ns Min.
t_{SMS}	250ns Min.
t_{DS}	150ns Min.
t_{PWH}	250ns Min.
t_{PWL}	250ns Min.
t_{LL}	250ns Min.
t_{LLW}	150ns Min.

NOTES: 1. With LOAD/$\overline{\text{LATCH}}$ at Logic '1' latches are transparent and data acts directly.

2. Serial Data Loading Sequence: – Logic '0' – PTL – $\overline{\text{PILOT ENABLE}}$ – Rx/$\overline{\text{Tx}}$ – $\overline{\text{Rx AUDIO ENABLE}}$ – $\overline{\text{PRIVATE ENABLE}}$ – MODE 1 – MODE 2.

Fig. 4 Loading Timing Diagrams

Audio Frequency Bands

Band Usage

Any Audio Band may be selected for clear or private functions, but "intended" use would be:

1. **Band A** Rx/$\overline{Tx}$ Private (333 – 3370Hz)
   Band B Rx/$\overline{Tx}$ Clear (300 – 3033Hz)
   Compatible with 'Auto Clear' pilot tone, CTCSS and PMR bandwidths.

2. **Band A** Rx/$\overline{Tx}$ Private/Clear (333 – 3370Hz)
   This is similar to (1) except that clear audio does not comply with mandatory PMR bandwidths.

3. **Band B** Rx/$\overline{Tx}$ Private/Clear (300 – 3033Hz)
   This complies with mandatory PMR bandwidths at all times but its use in "Auto -Clear" Mode (with Pilot Tone) is not recommended because the Pilot Tone is not filtered out at the receiver. This is suitable for fixed mode Private or manual Private/Clear operation.

4. **Band C** Rx/$\overline{Tx}$ Private/Clear (273 – 2757Hz) Required for time-compressed applications where loss of recovered "Private" voice bandwidth is avoided. The Pilot Tone could be used in the time-compressed mode if injected after compression.

Table 2 Loading Mode/Audio Band Control

Parallel Loading Mode						Serial Loading Mode		
Mode 1 I/P	Mode 2 I/P	Audio Band-Freq. (Hz)	Carrier Freq. (Hz)	Divisor ($f_{clk}/_X$)	Control Mode	Serial Data In Bit 7	Bit 8	Audio Band
0	1	C 273 – 2757	3030	X = 330	Parallel	0	1	C
1	0	A 333 – 3370	3703	X = 270	Parallel	1	0	A
1	1	B 300 – 3033	3333	X = 300	Parallel	1	1	B
0	0	—	—	—	Serial	0	0	B

Audio Bands

The audio band/modulation frequency relationships with their division ratios are shown in Table 2 and are produced with a Xtal/clock frequency (f_{clk}) of 1MHz. The modulation frequency and band limits will alter proportionally with Xtal frequency.

Table 3 Bandwidths

Audio Band	Stopband @≥–42dB. F max	Passband		Attenuation at Carrier Frequency		Stopband @≥–42dB. F min.
A	278Hz	333Hz	3370Hz	3703Hz	20dB	4036Hz
B	250Hz	300Hz	3033Hz	3333Hz	20dB	3633Hz
C	227Hz	273Hz	2757Hz	3030Hz	20dB	3302Hz

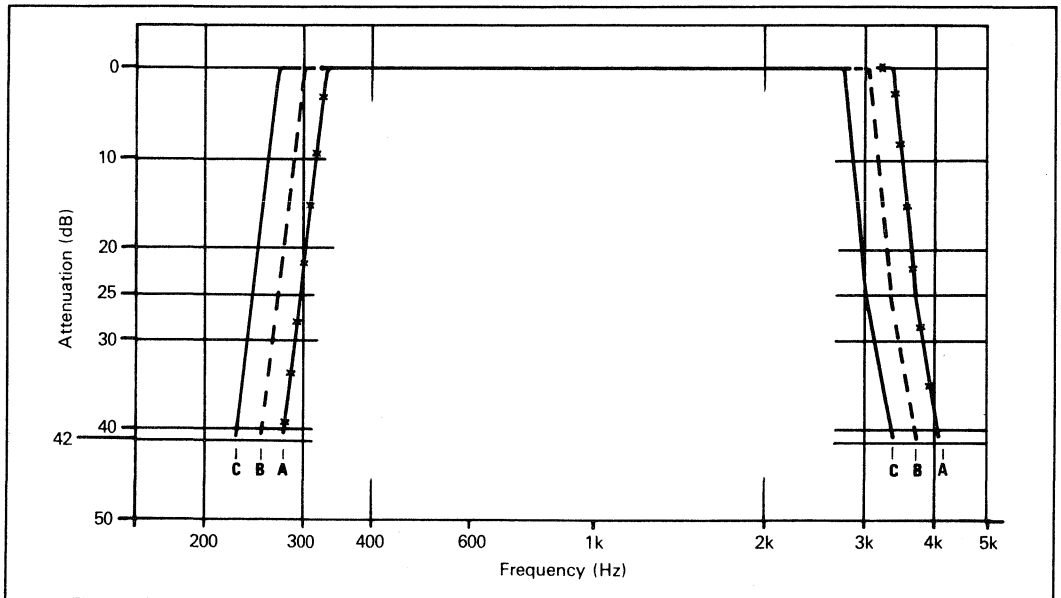


Fig. 5 Typical Audio Bandpass Filter Responses (1 Filter)

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (supply pins)		±30mA
(other pins)		±20mA
Total device dissipation @ 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX004J**	−30°C to +85°C (Cerdip)
	FX004LG	−30°C to +70°C (Plastic)
Storage temperature range:	**FX004J**	−55°C to +125°C (Cerdip)
	FX004LG	−40°C to +85°C (Plastic)

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:

V_{DD} = +5V, T_{amb} = 25°C, Xtal/Clock (f_{clk}) = 1MHz, 0dB ref: 775mVrms.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current		–	8.0	–	mA
Audio Input Impedance		–	500	–	kΩ
Audio Output Impedance		–	500	–	Ω
Logic Input Impedance		–	1	–	MΩ
Logic Output Impedance					
(Rx Pilot Decode) To V_{DD}		–	100	–	kΩ
To V_{SS}		–	500	–	Ω
Input Logic '1'	1	3.5	–	–	V
Input Logic '0'	1	–	–	1.5	V
Output Logic '1'	1	4	–	–	V
Output Logic '0'	1	–	–	1	V
Dynamic Values:	1				
Audio Input Levels Rx/Tx	8	–	−8	–	dB
Audio Output Levels Rx/Tx		–	−8	–	dB
Audio Bandpass Filter (in clear)					
Passband Frequencies Band A	2	333	–	3370	Hz
Passband Frequencies Band B	2	300	–	3033	Hz
Passband Frequencies Band C	2	273	–	2757	Hz
Passband Gain	5	–	0	–	dB
Passband Ripple	5	–	±1	–	dB
Output Noise Level	3	–	−50	–	dB
Insertion Loss		–	0	–	dB
Total Harmonic Distortion	9	–	2	5	%
Pilot Tone Detector					
Sensitivity		–	13	–	mVrms
Response Time	6	–	50	–	ms
Talk off and Falsing	4				
Pilot Tone Output					
Tone Output Level		−2	0	+2	dB
Distortion		–	–	5	%
Tone Frequency	7	–	273.2	–	Hz
Parallel/Serial Inputs (Fig. 4)					
Parallel Data Valid Time (t_{VP})		200	–	–	ns
Parallel Load Time (t_L)		150	–	–	ns
Pulse Fall Time (t_F)		–	–	50	ns
Data Hold Time (t_{DH})		50	–	–	ns
Serial Mode Set Up Time (t_{SMS})	–	250	–	–	ns
Data Set Up Time (t_{DS})		150	–	–	ns
Clock 'High' Pulse Width (t_{PWH})		250	–	–	ns
Clock 'Low' Pulse Width (t_{PWL})		250	–	–	ns
Load/Latch Set Up Time (t_{LL})		250	–	–	ns
Load/Latch Pulse Width (t_{LLW})		150	–	–	ns

Notes:

1. *Characteristics specified at 5V V_{DD}.*
2. *Bandpass limits at −1dB of mean passband level.*
3. *Measured at the Rx audio output in Private with Rx audio input A.C short circuit.*
4. *Talk off:—for 30mV pilot tone (273Hz), 5kHz white noise at −3dB on tone, 1 drop out per minute is expected. Typically 5ms/drop out.*
   Falsing:—for 380mVrms (not clipping) 5kHz white noise 25 falses per minute are expected. 10ms/false. Measured without integration components.
5. *All bandpass filters display similar performances. See figure 5.*
6. *Tested with composite signal of 300 mVrms 1kHz tone, Pilot tone 30mVrms in white noise of 5kHz at 75mVrms.*
7. *In Tx only.*
8. *See figure 3 with respect to signal to noise ratio.*
9. *For −3dB, 1kHz input.*

Package Outlines

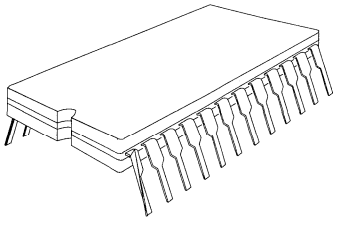
The FX004 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX004 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX004J 24-pin cerdip DIL (J4)

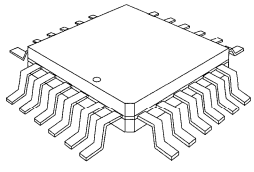
NOT TO SCALE



Max. Body Length 32.03mm
Max. Body Width 14.81mm

FX004LG 24-pin quad plastic encapsulated bent and cropped (L1)

NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

Ordering Information

FX004J 24-pin cerdip DIL (J4)

FX004LG 24-pin encapsulated bent and cropped (L1)

CML Semiconductor Products

PRODUCT INFORMATION

FX315

CTCSS Encoder

Publication D/315/5 July 1994

Features/Applications

- 40 CTCSS Frequencies
- Field Programmable Tone Encoder
- Xtal Frequency Stability
- Low Distortion Sinewave Output
- Low Power 5 volt CMOS
- Surface Mount or DIL Package Style

Applications

- CTCSS Encode Applications
- Repeater Access Control
- Mobile or Hand Held Radio Squelch Control
- Low Frequency Tone Generation

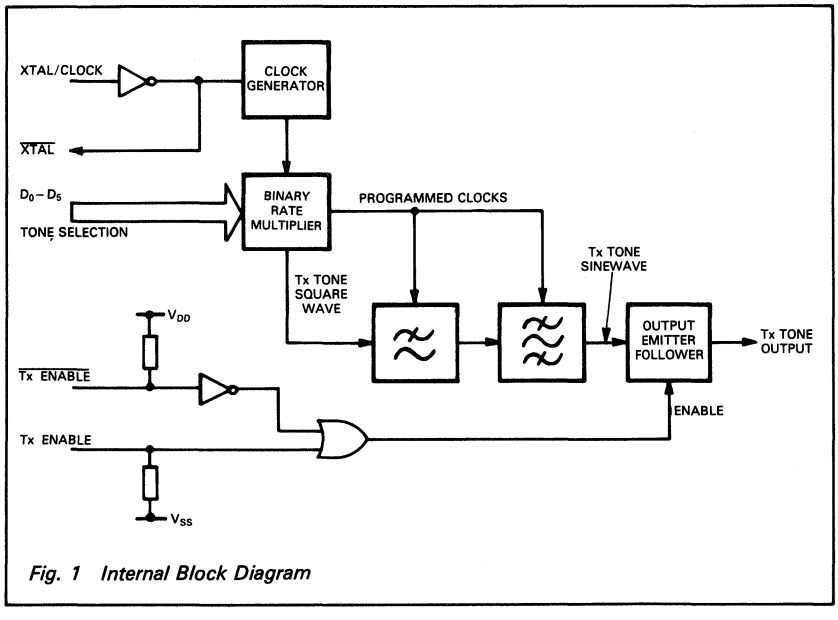


Fig. 1 Internal Block Diagram

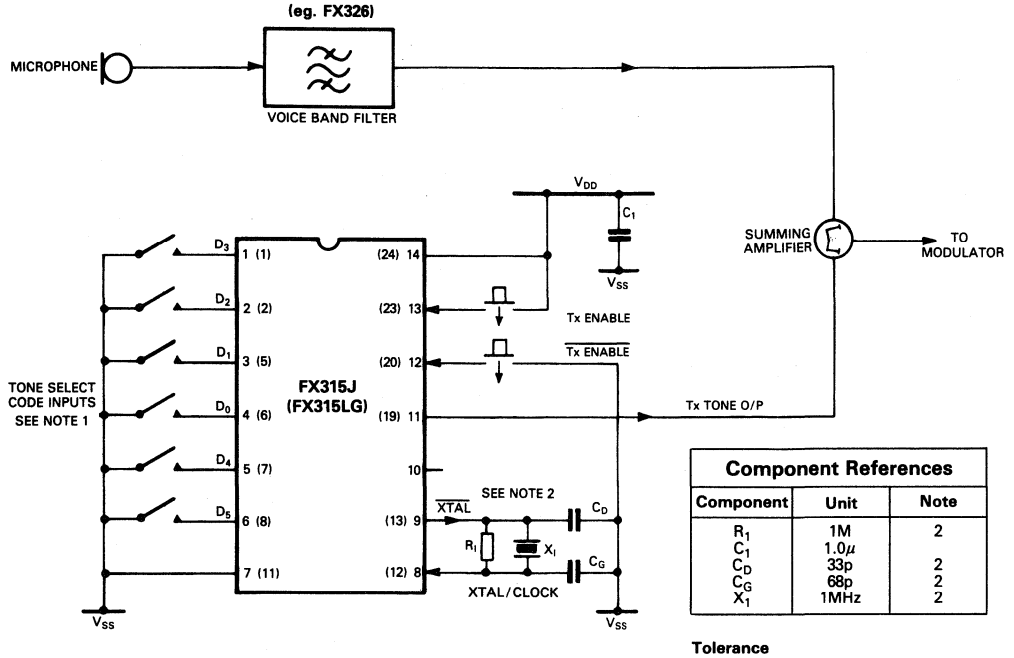
FX315

Brief Description

The FX315 is a monolithic CMOS integrated circuit tone encoder for sub-audio tone squelch systems. The tone frequencies are derived from an input reference frequency and an on-chip inverter is provided to drive an external crystal circuit.

Tone selection is by a logic code at the $D_0 - D_5$ programming inputs and two control inputs allow either a logic '1' or logic '0' to enable the device. A low distortion sinewave is generated at the Tx Tone Output when the FX315 is activated. The emitter follower output stage can source 1mW directly into a 600 Ohm load.

Pin Number		Function
DIL FX315J	Quad FX315LG	
1	1	D_3
2	2	D_2
3	5	D_1 — **Data Inputs:** The logic combination at these inputs defines the CTCSS tone that the FX315 will encode (see Table 1). The input is not latched and can be changed at any time. A logic '1' will be programmed if the input is open circuit, allowing the use of SPST switches. Internal 1MΩ pull-up to V_{DD} per pin.
4	6	D_0
5	7	D_4
6	8	D_5
7	11	V_{SS}: Negative Supply.
8	12	**Xtal/Clock:** 1MHz Xtal input or externally derived clock can be injected here. Input to the on-chip inverting oscillator, at no time should supply voltage be applied without the input clock signal.
9	13	**$\overline{\text{XTAL}}$:** 1MHz Xtal output. Inverting output of the on-chip inverting oscillator. When used as a Xtal oscillator, track lengths and loading on the two oscillator pins should be minimised.
10		**Internally wired.** Leave open circuit.
11	19	**Tx TONE OUTPUT:** The output of a low impedance emitter follower tone output stage. The tone is generated about a d.c. level of $V_{DD}/2$. The pin is high impedance when not enabled.
12	20	**$\overline{\text{Tx ENABLE}}$:** A logic '0' input at this pin will force the device into tone encoding. Internal 1MΩ pull-up to V_{DD}.
13	23	**Tx ENABLE:** A logic '1' input at this pin will force the device into tone encoding. Internal 1MΩ pull-down to V_{SS}.
14	24	V_{DD}: Positive 5 volt supply.
	3.4.9.10 14.15.16. 17.18.21 22	Not connected.



Component References		
Component	**Unit**	**Note**
R_1	1M	2
C_1	1.0μ	
C_D	33p	2
C_G	68p	2
X_1	1MHz	2

Tolerance
Resistors ±10%
Capacitors ±20%

Fig. 2 External Components and Application

Notes:

1. The FX315 'Tone Select' code inputs, left open circuit will be programmed with Logic '1's by the internal 1MΩ pull-up resistors.
This enables the use of simple devices when coding. Wire links can be fitted for permanent code, SPST switches will allow code changes in the field. Using preformed coded 7-pin inserts will enable the user to communicate in predetermined groups.

2. X_1 is a parallel resonant crystal. A reference frequency of 1 MHz± 0.19% is required to maintain a tone accuracy within ±0.5%.
Crystal circuitry shown in Figure 2 is in accordance with CML Application Note D/XT/1 April 1986. Where two or more circuits are required to use a single oscillator (eg. repeater applications), the signal at $\overline{XTAL}$ can be used to drive one additional Xtal/Clock input. Any further circuits can be driven from the buffered $\overline{XTAL}$ output of the second device.

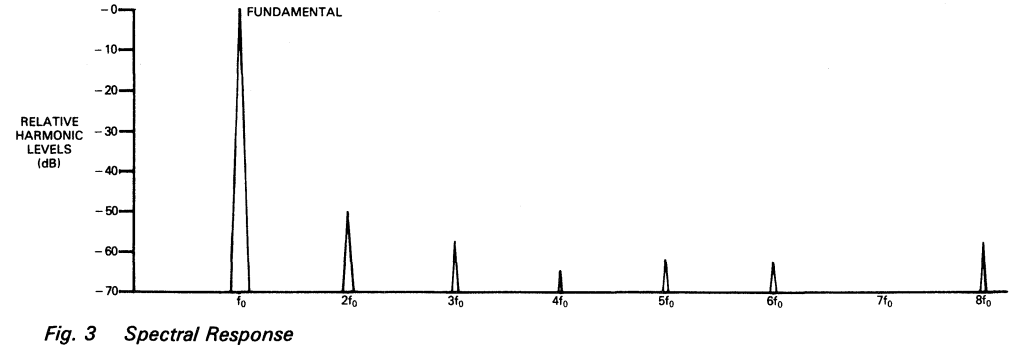


Fig. 3 Spectral Response

Nominal Freq. (Hz)	FX315 Freq. f_0 (Hz)	Δf_0 (%)	Programmable Inputs D_0 D_1 D_2 D_3 D_4 D_5	Nominal Freq. (Hz)	FX315 Freq. f_0 (Hz)	Δf_0 (%)	Programmable Inputs D_0 D_1 D_2 D_3 D_4 D_5
67.0	67.06	+0.10	1 1 1 1 1 1	131.8	131.67	-0.10	1 0 0 1 0 0
69.3	69.37	+0.10	1 0 0 1 1 1	136.5	136.69	+0.14	0 0 0 1 1 0
71.9	71.84	-0.08	1 1 1 1 1 0	141.3	141.48	+0.13	0 0 0 1 0 0
74.4	74.33	-0.10	0 1 1 1 1 1	146.2	145.96	-0.16	1 1 1 0 1 0
77.0	76.99	-0.02	1 1 1 1 0 0	151.4	151.45	+0.03	1 1 1 0 0 0
79.7	79.65	-0.06	1 0 1 1 1 1	156.7	156.59	-0.07	0 1 1 0 1 0
82.5	82.50	0.0	0 1 1 1 1 0	162.2	162.10	-0.06	0 1 1 0 0 0
85.4	85.34	-0.07	0 0 1 1 1 1	167.9	168.01	+0.07	1 0 1 0 1 0
88.5	88.62	+0.14	0 1 1 1 0 0	173.8	173.43	-0.21	1 0 1 0 0 0
91.5	91.38	-0.13	1 1 0 1 1 1	179.9	180.21	+0.17	0 0 1 0 1 0
94.8	94.88	+0.08	1 0 1 1 1 0	186.2	186.46	+0.14	0 0 1 0 0 0
97.4	97.46	+0.06	0 1 0 1 1 1	192.8	193.16	+0.19	1 1 0 0 1 0
100.0	99.87	-0.13	1 0 1 1 0 0	203.5	202.88	-0.31	1 1 0 0 0 0
103.5	103.39	-0.11	0 0 1 1 1 0	206.5	206.78	+0.14	0 0 0 1 1 1
107.2	107.17	-0.03	0 0 1 1 0 0	210.7	210.84	+0.07	0 1 0 0 1 0
110.9	110.85	-0.04	1 1 0 1 1 0	218.1	217.96	-0.07	0 1 0 0 0 0
114.8	114.80	0.0	1 1 0 1 0 0	225.7	225.58	-0.05	1 0 0 0 1 0
118.8	118.60	-0.17	0 1 0 1 1 0	233.6	233.75	+0.07	1 0 0 0 0 0
123.0	123.12	+0.10	0 1 0 1 0 0	241.8	242.54	+0.31	0 0 0 0 1 0
127.3	127.50	+0.16	1 0 0 1 1 0	250.3	250.06	+0.10	0 0 0 0 0 0
Test	4032	0.0	1 1 0 0 1 1				

Table 1 Code Programming *Logic "1" = V_{DD}* *Logic "0" = V_{SS}* *Xtal Frequency (X_1) = 1.0MHz*

General Notes

The FX315 is dedicated to continuous tone controlled squelch systems (CTCSS) in radio applications. It can however, be used wherever encoding of low frequency tones is required such as intercoms, door entry systems or industrial applications.

The performance of a CTCSS system can be degraded if speech frequencies in the signalling spectrum are not removed prior to transmission. This can be achieved by filtering the microphone signals to attenuate frequencies below 250Hz. Figure 2 illustrates adding the Tx Tone Output to the filtered microphone signals prior to modulation.

The FX315 requires a clock of 1MHz which is internally converted to logic level square waves. Consideration should therefore be given to possible interference problems with RF or IF circuitry caused by 1MHz or its harmonics (Fig. 3). A decoupling capacitor (C_1) should be used to smooth the supply rails. This will reduce the level of superimposed noise on the supply caused by internal switching transients (particularly at 1MHz and f_0).

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3 to (V_{DD} + 0.3V)
Output sink/source current (supply pins)		±30mA
(other pins)		±20mA
Total device dissipation @ 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX315J**	−30°C to +85°C (Ceramic)
	FX315LG	−30°C to +70°C (Plastic)
Storage temperature range:	**FX315J**	−55°C to +125°C (Ceramic)
	FX315LG	−40°C to +85°C (Plastic)

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:

V_{DD} = 5V, T_{amb} = 25°C, ϕ = 1MHz . R_L = 600Ω, C_L = 15pF.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (Enabled)		—	1.5	—	mA
Logic Input Impedance		—	500	—	kΩ
Xtal Input Impedance		—	10	—	MΩ
Inputs Logic '1'	1	3.5	—	—	V
Inputs Logic '0'	1	—	—	1.5	V
Dynamic Values:					
Tone Output Level		−3	0	—	dBm
Tone Accuracy (f_0 error)		—	—	±0.31	%f_0
Total Harmonic Distortion	2	—	2	5	%
Tone Output Load Current		—	—	5	mA
Tone Output Rise Time (t_R)		—	1	—	ms
Tone Level Variations		—	0.1	—	dB
Output Harmonic Attenuation		−49	—	—	dB

Notes: *1. Relate to all inputs.*

2. T.H.D. measurements taken in the 0 − 6kHz bandwidth.

3. Output Loading: Large capacitive loads could cause the output pins of this device to oscillate. If capacitive loads in excess of 200 pF are unavoidable a resistor of typically <100Ω put in series with the load should minimise this effect.

Package Outlines

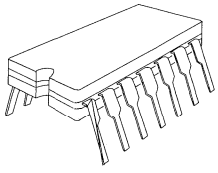
The FX315 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX315 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX315J 14-pin cerdip DIL (J1)

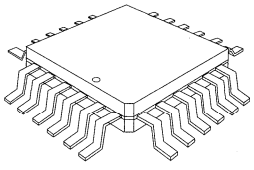
NOT TO SCALE



Max. Body Length 19.45mm
Max. Body Width 6.38mm

FX315LG 24-pin quad plastic encapsulated bent and cropped (L1)

NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

Ordering Information

FX315J 14-pin cerdip DIL (J1)

FX315LG 24-pin encapsulated bent and cropped (L1)

CML Semiconductor Products

PRODUCT INFORMATION

FX365C Low-Voltage CTCSS Encoder/ Decoder

Publication D/365C/2 July 1994

Features

- **Low-Voltage (3-Volt) Supply**
- **39 Programmable Sub-Audio Tones + NOTONE**
- **Meets MPT1306 and EIA - 220 B**
- **High Voiceband/CTCSS Isolation**
- **Separate Sub-Audio and Rx/Tx Audio Paths and Filtering**

Applications

- **Mobile Radio Systems**
- **Community Base Stations**
- **"Sports Radio" (Japan)**
- **Sub-Audio Signalling and Selective Calling**
- **Status and Alarm Systems**
- **Amateur Radio**

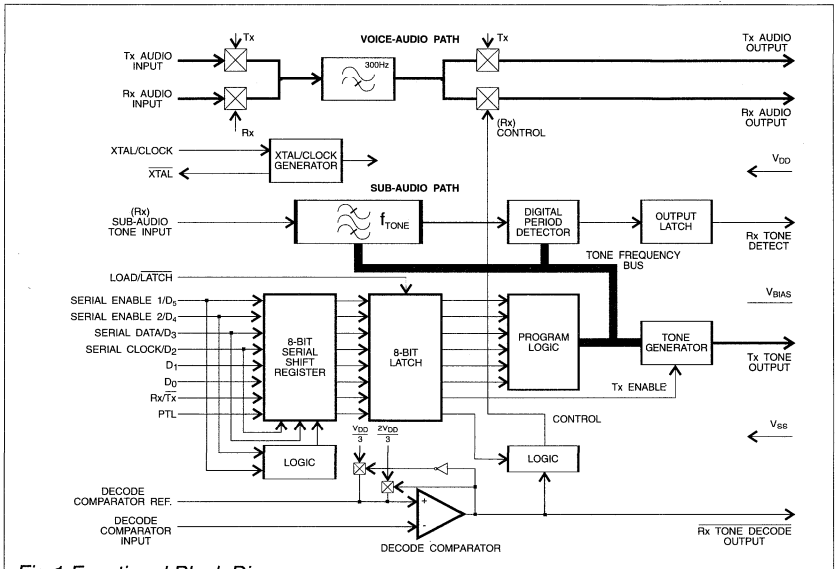


Fig.1 Functional Block Diagram

FX365C

Brief Description

The FX365C is a 3-volt, half-duplex predictive Continuous Tone Controlled Squelch System (CTCSS) encoder/decoder microcircuit. The FX365C has integral voice-band filtering for prefiltering of Tx audio and the rejection of the CTCSS tone in receive.

Under µProcessor control, the FX365C will encode and decode any one of 39 sub-audio frequencies (+NOTONE) in the range 67.0Hz to 250.3Hz. Tone frequencies and all functional commands can be loaded to the device in either pin-selectable 8-bit parallel or serial format.

A separate, Rx/Tx voice-audio path is available with a highpass (sub-audio reject) filter automatically placed in the relevant Rx or Tx voice line.

The Rx sub-audio (CTCSS) path contains a (selected tone frequency) bandpass filter and period detector providing a logic level output (Rx Tone Detect) to indicate a successful decode operation.

Rx "Press to Listen" (PTL) and Tx "Squelch-Tail Elimination" functions are available in both command loading modes. The squelch-tail elimination function will provide (Tx tone) phase-reversal to minimise the annoying audio outputs that occur at the receiver on completion of a transmission.

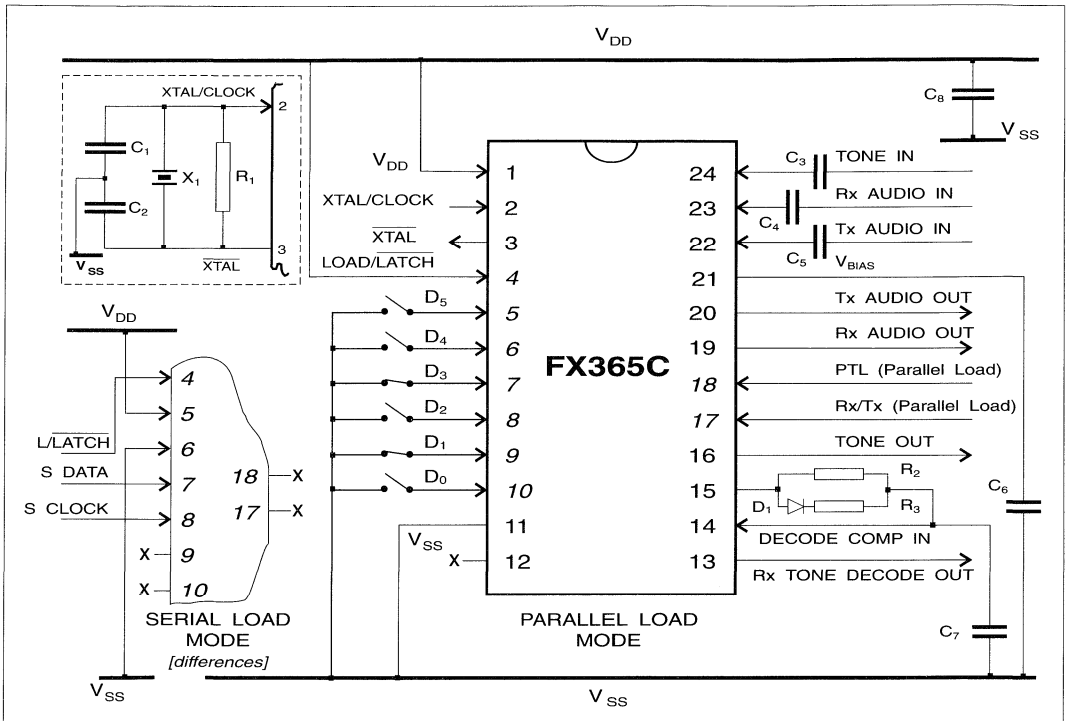
Tone frequencies and filter accuracies are maintained by an on-chip 1.0MHz clock oscillator employing an external crystal or clock pulse input.

The FX365C, which exhibits high audio and sub-audio performance with low falsing, is available in 24-pin DIL and small outline SMD packages.

Pin Number	Function
FX365C	DW and J package styles.
1	**V_{DD}:** Positive supply rail. A single stable supply is required; levels and voltages within the FX365C are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor located close to the pin.
2	**Xtal/Clock:** Input to the on-chip inverter; used with a 1.0MHz Xtal or external clock source.
3	**$\overline{\text{Xtal}}$:** Output of the on-chip clock oscillator inverter.
4	**Load/$\overline{\text{Latch}}$:** Controls 8 on-chip latches and is used to latch Rx/Tx, PTL, D_0 - D_5. This pin is internally pulled to V_{DD}. A logic '1' applied to this input places the 8 latches into a 'transparent' mode. A logic '0' applied to this input places the 8 latches into the 'latched' mode. In parallel mode data is loaded and latched by a logic '1' to '0' transition (see Figure 4a). In serial mode data is loaded and latched by a '0' to '1' to '0' strobe pulse on this pin (see Figure 4b).
5	**D_5/Serial Enable 1:** Data input D_5 (Parallel Mode); Serial Enable 1 (Serial Mode). A logic 'l' applied to this input, together with a logic '0' applied to D_4/Serial Enable 2, will put the device into 'Serial Mode' (see Figure 4b). This pin is internally pulled to V_{DD}.
6	**D_4/Serial Enable 2:** Data input D_4 (Parallel Mode); Serial Enable 2 (Serial Mode). A logic '0' applied to this input, together with a logic '1' applied to D_5/Serial Enable 1, will place the device into 'Serial Mode' (see Figure 4b). This pin internally pulled to V_{DD}.
7	**D_3/Serial Data:** Data input D_3 (Parallel Mode); Serial Data Input (Serial Mode). In Serial Mode this pin becomes the serial data input for D_5 - D_0, Rx/Tx, PTL (see Figure 4b). D_5 is clocked-in first and PTL last. This pin internally pulled to V_{DD}.
8	**D_2/Serial Clock:** Data input D_2 (Parallel Mode); Serial Clock Input (Serial Mode). In Serial Mode this pin becomes the Serial Clock input. Data is clocked on the positive-going edge (see Figure 4b). This pin is internally pulled to V_{DD}.
9	**D_1:** Data input D_1 (Parallel Mode); Not Used (Serial Mode). This pin is internally pulled to V_{DD}.
10	**D_0:** Data input D_0 (Parallel Mode); Not Used (Serial Mode). This pin is internally pulled to V_{DD}.
11	**V_{SS}:** Negative supply (GND).
12	**Decode Comparator Ref.** (I/P): Internally biased to $V_{DD}/3$ or $2V_{DD}/3$ via 1.0MΩ resistors depending on the logical state of the Tone Decode Output pin, this input provides the decode comparator reference voltage; switching of bias voltages provides hysteresis to reduce 'chatter' under marginal conditions. Tone Decode Output = logic '1' will place this input to $2V_{DD}/3$ bias, a logic '0' will bias this input to $V_{DD}/3$.

Pin Number	Function
FX365C	DW and J package styles.
13	**$\overline{\text{Rx Tone Decoder}}$** (O/P): The gated output of the on-chip Decode Comparator. This output is used to gate the Rx Audio path. A logic '0' output on this pin indicates a successful decode and indicates that the 'Decode Comparator Input' pin is more positive than the 'Decode Comparator Ref' input (see Table 1).
14	**Decode Comparator Input:** The inverting input of the Decode Comparator. This pin is to be connected to the Rx Tone Detect pin via external integrating components as shown in Figure 2.
15	**Rx Tone Detect** (O/P): In the Rx mode this output will go to a logic '1' during a successful decode (Table 1). This pin is to be connected to the Decode Comparator Input via the external integrating circuitry as shown in Figure 2.
16	**Tx Tone Output:** A low-impedance emitter-follower source, under the control of the Rx/Tx pin, of the CTCSS sinewave. This output, when not transmitting a sub-audio tone, may be set to a V_{DD}/(2-0.7)V bias or open-circuit as described in Table 1.
17	**Rx/$\overline{\text{Tx}}$:** This input (Parallel Mode) selects Rx or Tx modes (see Figure 2). Logic '1' = Rx; logic '0' = Tx. In Serial Mode this (Rx or Tx) function is serially loaded via pin 7 (Serial Data) and this pin not used. This pin is internally pulled to V_{DD} via a 1MΩ resistor (Rx operaion).
18	**PTL:** A dual-function input. In the parallel load mode, Rx operation: A logic '1' provides a "Press To Listen" function by overriding the tone-squelch and enabling the audio path. In the parallel load mode, Tx operation: A logic '1' provides a "Squelch Tail Elimination" function by reversing the phase of the transmitting sub-audio tone; the phase reversal function should be applied by a suitable timing circuit. In the serial load mode (Rx and Tx) these functions are loaded via the serial data word at pin 7.
19	**Rx Audio Output:** The high-pass filtered 'Received Audio' output. This pin outputs audio when Rx Tone Decode = '0', or PTL = '1' or 'Notone' is programmed (Table 2). In Tx Mode this pin is biased to V_{DD}/2.
20	**Tx Audio Output:** The high-pass filtered 'Transmit Audio' output. In Tx mode this pin outputs audio present at the Tx Audio Input by opening the Tx audio path. In Rx mode this pin is biased to V_{DD}/2.
21	**V_{BIAS}:** The output of the on-chip analogue bias circuitry. Held internally at V_{DD}/2, this pin should be externally decoupled to V_{SS}.
22	**Tx Audio Input:** The Tx Audio Input pin. Tx voice-band audio may be prefiitered, using the Voice Audio Path, thus helping to avoid talk-off due to the intermodulation of speech frequencies with the transmitted CTCSS tone. The Tx Audio Path may also be used to pre-filter speech when employing 'scramblers' which could introduce noise into the low frequency band. This pin is internally biased to V_{DD}/2.
23	**Rx Audio Input:** The input to the Voice Audio high-pass filter in the Rx Mode. This pin is internally biased to V_{DD}/2.
24	**Tone Input:** The input to the CTCSS tone detector and is internally biased to V_{DD}/2.

Application Information



External Components

Component	Value	Tolerance	Component	Value	Tolerance
R_1	1.0MΩ	±10%	C_4	0.1µF	±20%
R_2	820kΩ	±10%	C_5	0.1µF	±20%
R_3	330kΩ	±10%	C_6	1.0µF	±20%
			C_7	0.1µF	±20%
C_1	68.0pF	±20%	C_8	1.0µF	±20%
C_2	33pF	±20%	D_1	small signal type	
C_3	0.1µF	±20%	X_1	1.0MHz	

Fig.2 Recommended External Components

Input Pin Condition				*Output Pin Condition*		*Result and/or Function*					
D_0 to D_5	Rx/$\overline{Tx}$	PTL	Decode Comp. Input	Rx Tone Detect	$\overline{\text{Rx Tone Decode}}$	Tone Tx Enabled	Tx Tone Phase Reversed	Tx Audio Path Enabled	Tone Decoder Enabled	Rx Audio Path Enabled	Notes
TONE	0	0	x	0	1	YES	NO	YES	NO	NO (BIAS)	1A
TONE	0	1	x	0	1	YES	YES	YES	NO	NO (BIAS)	1B
NOTONE	0	x	x	0	1	NO (BIAS)	x	YES	NO	NO (BIAS)	2
TONE	1	0	0	0	1	NO(o/c)	x	NO	YES	YES	3A
TONE	1	1	0	0	1	NO (o/c)	x	NO	YES	YES	3B
TONE	1	x	1	1	0	NO (o/c)	x	NO	YES	YES	4
NOTONE	1	x	x	x	0	NO (o/c)	x	NO	YES	YES	5

NOTES

1A Normal tone transmit condition.
1B Tone Tx with phase reversed.
2 NOTONE programmed in Tx mode; tone transmit output set to $V_{DD}/2$ -(0.7v). Tx audio path enabled.
3A Normal decode standby.
3B Normal decode standby with PTL used to enable audio.
4 Normal 'decode of correct CTCSS tone' condition; PTL has no effect.
5 NOTONE programmed in Rx mode; tone transmit output (o/c). Rx audio path enabled.

Table 1 Combinations of Input/Output Conditions *x = don't care*

Application Information .....

Nominal Freq (Hz)	FX365C Freq. (Hz)	Δfo %	D_0	D_1	D_2	D_3	D_4	D_5
67.0	67.05	+0.7	1	1	1	1	1	1
69.3	69.32	+0.03	1	0	0	1	1	1
71.9	71.90	0.0	1	1	1	1	1	0
74.4	74.35	-0.07	0	1	1	1	1	1
77.0	76.96	-0.05	1	1	1	1	0	0
79.7	79.77	+0.09	1	0	1	1	1	1
82.5	82.59	+0.10	0	1	1	1	1	0
85.4	85.38	-0.02	0	0	1	1	1	1
88.5	88.61	+0.13	0	1	1	1	0	0
91.5	91.58	+0.09	1	1	0	1	1	1
94.8	94.76	-0.04	1	0	1	1	1	0
97.4	97.29	-0.11	0	1	0	1	1	1
100.0	99.96	-0.04	1	0	1	1	0	0
103.5	103.43	-0.07	0	0	1	1	1	0
107.2	107.15	-0.05	0	0	1	1	0	0
110.9	110.77	-0.12	1	1	0	1	1	0
114.8	114.64	-0.14	1	1	0	1	0	0
118.8	118.80	0.0	0	1	0	1	1	0
123.0	122.80	-0.17	0	1	0	1	0	0
127.3	127.08	-0.17	1	0	0	1	1	0
131.8	131.67	-0.10	1	0	0	1	0	0
136.5	136.61	+0.08	0	0	0	1	1	0
141.3	141.32	+0.02	0	0	0	1	0	0
146.2	146.37	+0.12	1	1	1	0	1	0
151.4	151.09	-0.20	1	1	1	0	0	0
156.7	156.88	+0.11	0	1	1	0	1	0
162.2	162.31	+0.07	0	1	1	0	0	0
167.9	168.14	+0.14	1	0	1	0	1	0
173.8	173.48	-0.19	1	0	1	0	0	0
179.9	180.15	+0.14	0	0	1	0	1	0
186.2	186.29	+0.05	0	0	1	0	0	0
192.8	192.86	+0.03	1	1	0	0	1	0
203.5	203.65	+0.07	1	1	0	0	0	0
210.7	210.17	-0.25	0	1	0	0	1	0
218.1	218.58	+0.22	0	1	0	0	0	0
225.7	226.12	+0.18	1	0	0	0	1	0
233.6	234.19	+0.25	1	0	0	0	0	0
241.8	241.08	-0.30	0	0	0	0	1	0
250.3	250.28	-0.01	0	0	0	0	0	0
NOTONE	NOTONE		0	0	0	0	1	1
Serial Input Mode			x	x	Clock	Data	0	1

Table 2 Tone Programming Information

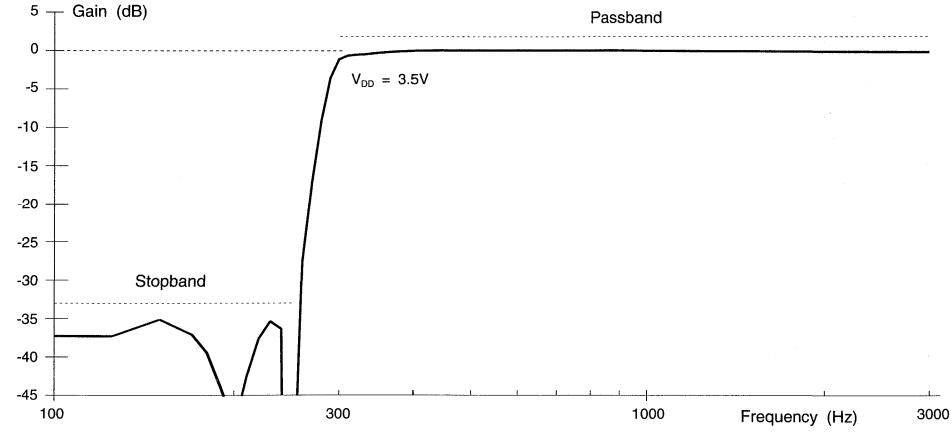


Fig.3 Voiceband Filter Response

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX365C J**	-40°C to +85°C (cerdip)
	FX365C DW	-40°C to +85°C (plastic)
Storage temperature range:	**FX365C J**	-55°C to +125°C (cerdip)
	FX365C DW	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:
V_{DD} = 3.3V. T_{AMB} = 25°C. Xtal/Clock f_0 = 1.0MHz. Signal 0dB ref: = 180mVrms.
Composite Signal = 1.0kHz Audio Tone at 0dB, Noise at –12.0dB (gaussian white noise, band-limited to 6.0kHz), Programmed CTCSS Tone at -20dB.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Characteristics					
Supply Voltage (V_{DD})		3.0	3.3	5.5	V
Supply Current					
(Tx)		-	1.5	-	mA
(Rx)		-	1.5	-	mA
Sub-Audio Tone Input Impedance		-	1.0	-	MΩ
Tx Tone Output Impedance		-	4.0	-	kΩ
Voice-Audio Input Impedance		-	1.0	-	MΩ
Voice-Audio Output Impedance		-	1.0	-	kΩ
Digital Input Impedance	1	-	1.0	-	MΩ
Input Logic '1'	1	70.0	-	-	%V_{DD}
Input Logic '0'	1	-	-	30.0	%V_{DD}
Output Logic '1', source = 0.1mA	2	80.0	-	-	%V_{DD}
Output Logic '0', sink = 0.1 mA	2	-	-	20.0	%V_{DD}
Dynamic Characteristics					
Tone Decoder					
Decode Input Signal Level	3	-20.0	-	-	dB
Decode Response Time	3, 6	-	-	250	ms
De-Response Time	3, 6	-	-	250	ms
Decode Selectivity	3	±0.5	-	±3.0	%f_0
Tone Encoder					
Tx Tone Output Level		-	6[illegible]	-	mVrms
Tx Tone Frequency Accuracy (f_0 error)		-0.3	-	+0.3	%f_0
Risetime to 90% (nominal output)					
f_0 > 100Hz	4	-	55.0	-	ms
f_0 < 100Hz	4	-	70.0	-	ms
Tone Output Load Current		-	-	5.0	mA
Total Harmonic Distortion		-	2.0	5.0	%
Output Level Variation Between Tones		-	0.1	-	dB
Spurious Emissions		-	-	-48.0	dB
Voice-Audio Filter and Path					
Passband Frequencies		300		3000	Hz
Passband Gain					
at 1.0kHz		-	0	-	dB
w.r.t. 1.0kHz		-2.0	-	0.5	dB
Total Harmonic Distortion	5	-	2.0	5.0	%
Stopband Frequencies		-	-	250	Hz
Stopband Attenuation		33.0	36.0	-	dB
Output Noise Level (Input a.c. Short Cct)	7	-	-54.0	-48.0	dB
Bandpass Ripple (300Hz –3000Hz)	5	-1.0	-	+1.0	dB
SINAD	8	36.0	40.0	-	dB
Audio Switch Isolation	5	-	60.0	-	dB

Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
Serial/Parallel Inputs					
Parallel Set-Up Time (t_{SP})		400	-	-	ns
Load/Latch Pulse Width (t_L)		400	-	-	ns
Serial Clock Pulse Width (t_C)		400	-	-	ns
Serial Set-Up Time (t_{SS})		400	-	-	ns
Serial Enable Time (t_1)		400	-	-	ns
Serial Load/Latch Set-Up Time (t_2)		400	-	-	ns
Serial Clock Frequency		-	1.0	-	MHz

Notes

1. Refers to Rx/Tx, PTL, Decode Comparator Input, D_0, D_1, D_2, D_3, D_4, D_5 inputs.
2. All logic outputs.
3. Composite Signal test condition.
4. Any programme tone and RL = 600Ω. CL = 15pF. Includes response to a phase-reversal instruction.
5. 1kHz reference = 0dB.
6. f_O > 100Hz, (for 100Hz >f_O >67Hz: t = (100/f_O Hz) x 250ms).
7. Measured in a 30kHz bandwidth.
8. For an input level of 180mVrms at 1.0kHz, in a 30kHz measurement bandwidth.

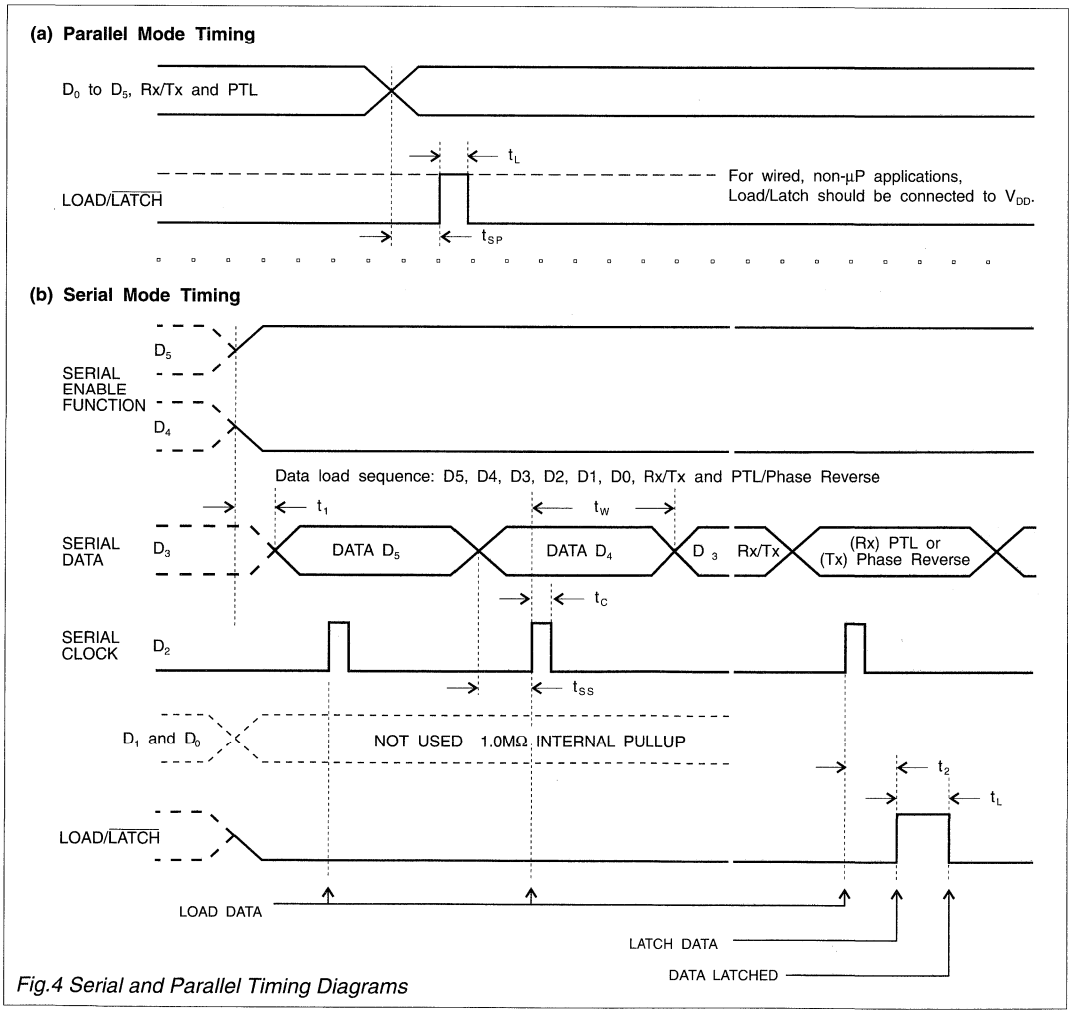


Fig.4 Serial and Parallel Timing Diagrams

Package Outlines

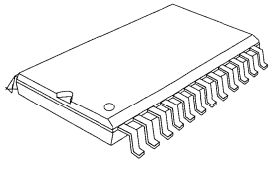
The FX365C is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX365C is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX365C DW 24-pin plastic S.O.I.C (D2)

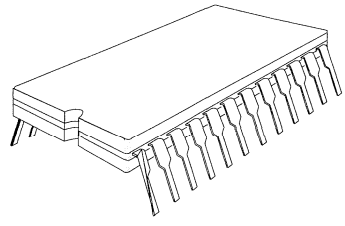
NOT TO SCALE



Max. Body Length 15.70mm
Max. Body Width 7.65mm

FX365C J 24-pin cerdip DIL (J4)

NOT TO SCALE



Max. Body Length 32.03mm
Max. Body Width 14.81mm

Ordering Information

FX365C DW 24-pin plastic S.O.I.C. (D2)

FX365C J 24-pin cerdip DIL (J4)

CML Semiconductor Products

PRODUCT INFORMATION

FX375

Private Squelch Circuit

Publication D/375/4 July 1994

Features/Applications

- Tone Operated Private/Clear Switching
- CTCSS Tone Encode/Decode
- Separate Rx/Tx Speech Paths
- Fixed Frequency Speech Inversion
- µP Compatible Interface with Serial or Parallel Control Loading
- On-Chip Pre- and De-Emphasis Filtering in the Tx Path
- 38 Programmable Tones + 'NoTone' Facility
- Audio Path Filtering (300Hz – 3033Hz)
- Low Power 5V CMOS

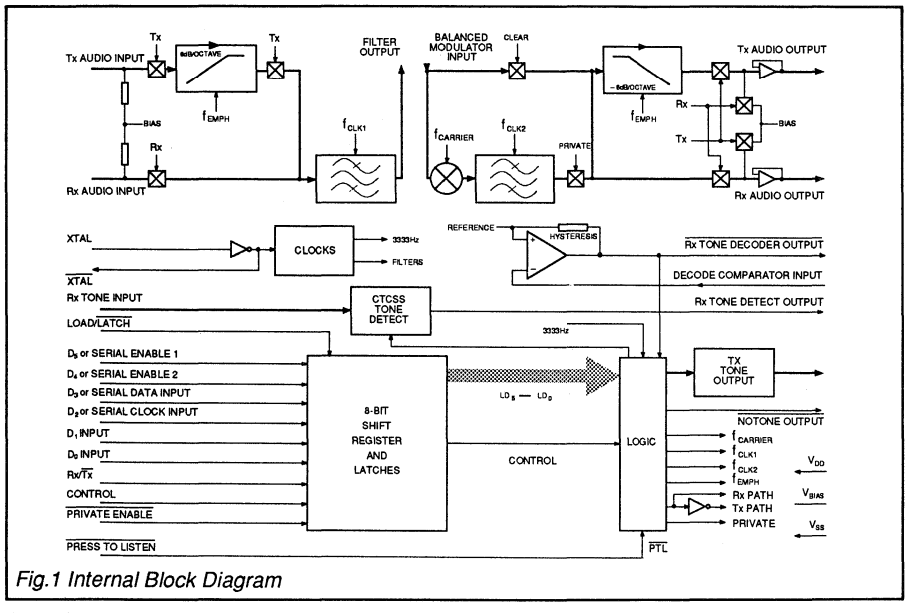


Fig.1 Internal Block Diagram

FX375

Brief Description

The FX375 is a Low-Power CMOS LSI microcircuit designed for Tone Operated Voice Privacy in communication systems.

This half-duplex device consists of a Fixed Frequency Voice Band Inverter interfaced with a Continuous Tone Controlled Squelch System (CTCSS) Encoder/ Decoder, whose allocated tone is used for voice privacy and audio squelch operation.

Frequency Inversion is achieved by modulating the input audio with a fixed carrier frequency to exchange the high and low frequencies of the voice band, making the resulting audio output unintelligible to receivers not equipped with a compatible system.

The on-chip CTCSS Dencoder is capable of encoding and decoding any one of 38 sub-audio tones in the range 67.0Hz to 250.3Hz, these Xtal derived tones are selected by a 6-bit binary word that can be loaded to the device in either a serial or parallel format.

The Privacy function is exclusive only to units using the same tone set, other intercepted signals remain "as transmitted."

A 'Press to Listen' facility allows monitoring of the channel prior to transmitting.

This device has separate, switched Rx and Tx voice, and tone audio paths. Voice paths use switched capacitor bandpass filters for the attenuation of sub-audio tones and unwanted modulation products.

6dB/octave pre- and de-emphasis filtering in the Tx path maintains natural sounding audio from this device when embodied in communication transceivers.

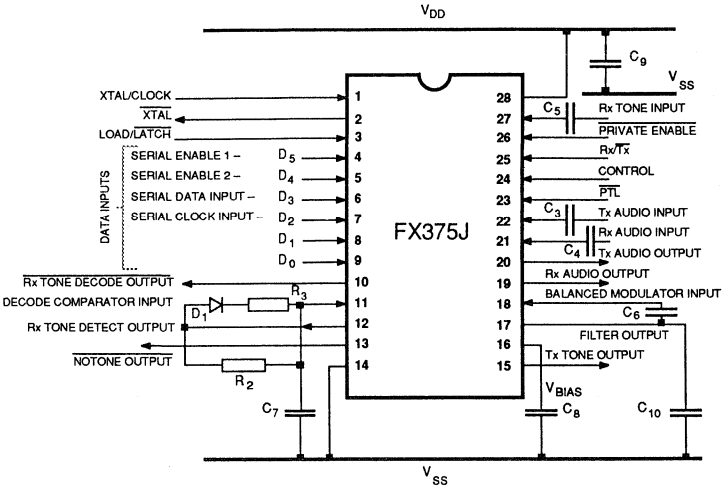
The FX375, which is available in DIL and SMT packages, can be simply controlled by switches, or interfaced to a µProcessor.

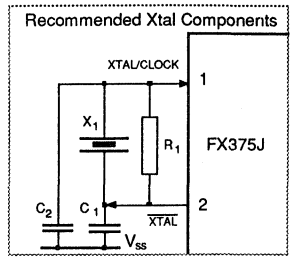
External requirements are a single 5-volt supply, an external 4.0MHz Xtal or clock input and signal coupling components.

Pin Number		Function
FX375J	FX375LG FX375LS	
1	2	**Xtal/Clock:** The input to the clock oscillator inverter. An external 4MHz Xtal or clock input is to be applied at this pin. See Figure 2.
2	3	**$\overline{\text{Xtal}}$:** The 4MHz output of the clock oscillator inverter. See Figure 2.
3	4	**Load/$\overline{\text{Latch}}$:** This input regulates the operation of the eight input latches : D_0, D_1, D_2, D_3, D_4, D_5, Rx/Tx and Private Enable for both parallel and serial input load modes. Rx/Tx and Private Enable inputs can be used independently in either mode by the use of Load/Latch and Control inputs configured as shown in Table 3, the data format ($D_0 - D_5$), remains as set. This input has an internal 1MΩ pullup resistor.
4	–	**D_5 – (Serial Enable 1) :** The Rx/$\overline{\text{Tx}}$ tone programming and function inputs. Programmed as shown in Table 2 these inputs will select the CTCSS tone frequency and parallel or serial loading function. Notone, when set in receive, enables the Rx Audio Output and forces the Rx Tone Decode Output to a logic '0,' in transmit the Tx Tone Output is held at V_{BIAS} (Notone). These inputs each have an internal 1MΩ pullup resistor. If FX375LG or LS package styles are used Pin 5 (Serial Enable 2) should be externally connected to V_{SS}.
5	5	**D_4 – (Serial Enable 2) :**
6	6	**D_3 – (Serial Data Input) :**
7	7	**D_2 – (Serial Clock Input) :**
8	–	**D_1**
9	–	**D_0**
10	8	**$\overline{\text{Rx Tone Decode Output}}$:** The output of the decode comparator. In Rx a logic '0' indicates 'CTCSS tone decoded' above the internal reference level, or Notone programmed. This action internally enables the Rx audio path and Frequency Inversion function (when applicable) as shown in Table 1. In Tx this output is a logic '1'.
11	9	**Decode Comparator Input :** A logic '1' at this pin, in Rx, is compared internally with a fixed reference level, a more positive input value will produce a logic '0' at the Rx Tone Decode Output. This input should be externally connected to the Rx Tone Detect Output via external integrator components C_7, R_2, R_3, D_1 (see Figure 2).
12	10	**Rx Tone Detect Output :** This output, in Rx, goes to a logic '1' when a valid, programmed CTCSS tone is received at the Rx Tone Input. This input should be externally connected to the Decode Comparator Input via external integrator components C_7, R_2, R_3, D_1 (see Figure 2).
13	–	**$\overline{\text{Notone Output}}$:** Outputs a logic '0' when a " Notone" CTCSS code has been programmed . It can be used to operate squelch circuitry under receive "Notone" conditions.
14	11	**V_{SS} :** Negative supply rail (GND). The FX375LG and LS package styles are configured as a serial-data loading device, Parallel Programing Inputs D_0, D_1 and D_5, and the NOTONE Output pin functions are not available.

Pin Number		Function
FX375J	FX375LG FX375LS	
15	12	**Tx Tone Output :** This is the buffered, programmed CTCSS tone sinewave output in Tx. During Rx and Notone operation this output is held at V_{BIAS}. See note "g," page 7 with reference to capacitive load limits of this output.
16	13	**V_{BIAS} :** This bias pin is set internally to $V_{DD}/2$. It must be externally decoupled using a capacitor, C_8, of 1.0µF (minimum) to V_{SS}, see Figure 2.
17	14	**Filter Output :** The Input Audio Bandpass Filter output, this pin must be connected to the Balanced Modulator Input via a capacitor, C_6, and decoupled to V_{SS} by C_{10}, see Figure 2.
18	15	**Balanced Modulator Input :** The input to the Balanced Modulator, this pin must be connected to the Filter Output via a capacitor, C_6, see Figure 2.
19	16	**Rx Audio Output :** Outputs the received audio from a buffered output stage and is held at V_{BIAS} when in Tx.
20	17	**Tx Audio Output :** The output of the audio path in the Tx mode and is held at V_{BIAS} when in Rx.
21	18	**Rx Audio Input :** The Audio input pin for the Rx mode. Input signals should be a.c. coupled via an external capacitor, C_4, see Figure 2.
22	19	**Tx Audio Input :** This is the voice input pin for the Tx mode. Signals should be a.c. coupled via an external capacitor, C_3, see Figure 2.
23	20	**$\overline{\text{PTL}}$:** The "Press To Listen" function input, in the receive mode a logic '0' enables the Rx Audio Output directly, overriding tone squelch but not intercepting a private conversation. In the transmit mode a logic '0' reverses the phase of the Tx Tone Output for "squelch tail" reduction (see Table 1), this function, in Tx, should be accurately applied by a timing circuit to ensure correct system operation.
24	21	**Control :** This input, with Load/$\overline{\text{Latch}}$, selects the operational mode of Rx/$\overline{\text{Tx}}$ and Private Enable functions, see Table 3.
25	22	**Rx/$\overline{\text{Tx}}$:** Selects the receive or transmit mode (Rx = '1', Tx = '0') and can be loaded by serial or parallel means, as described in Table 3.
26	23	**$\overline{\text{Private Enable}}$:** This input selects either Private or Clear modes (Clear = '1', Private ='0'), and can be loaded by serial or parallel means, as described in Table 3. In Rx this input could be taken from the Rx Tone Decode Output. This input has an internal 1MΩ pullup resistor.
27	24	**Rx Tone Input :** The received tone input to the on-chip CTCSS decoder and should be a.c. coupled via capacitor C_5, see Figure 2.
28	1	**V_{DD} :** Positive supply rail. A single +5V power supply is required.

Operational Information





Component	Unit Value
R_1	1M
R_2	820k
R_3	330k
C_1	33p
C_2	33p
C_3	0.1µ
C_4	0.1µ
C_5	0.1µ
C_6	1.0µ
C_7	0.1µ
C_8	1.0µ
C_9	1.0µ
C_{10}	1.0n
D_1	Small Signal
X_1	4MHz

Component Tolerances
Resistors ± 10%
Capacitors ± 20%

Fig.2 External Component Connections

Operational Truth Table – Table 1 (below) illustrates the output paths and logic functions of the FX375 Private Squelch Circuit in both Receive and Transmit modes.

Receive Operation – (Rx/$\overline{Tx}$ = '1')
In the Rx mode Tx Tone and Tx Audio paths are held at bias.

D_0 – D_5	$\overline{\text{Notone}}$	$\overline{\text{Private Enable}}$	$\overline{\text{PTL}}$	Rx Tone Detect	$\overline{\text{Rx Tone Decode}}$	Receive Signal Path State	Receive Signal Path Condition
Tone	1	0	1	0	1	bias	X
Tone	1	0	0	0	1	open	Not Inverted
Tone	1	0	X	1	0	open	Inverted
Notone	0	0	X	X	0	open	Not Inverted
Tone	1	1	1	0	1	bias	X
Tone	1	1	0	0	1	open	Not Inverted
Tone	1	1	X	1	0	open	Not Inverted
Notone	0	1	X	X	0	open	Not Inverted

Transmit Operation – (Rx/$\overline{Tx}$ ='0')
In the Tx mode the Rx audio path is held at bias and the Rx Tone Detect output at logic '0.'

D_0 – D_5	$\overline{\text{Notone}}$	$\overline{\text{Private Enable}}$	$\overline{\text{PTL}}$	Transmitted Tone State	Transmitted Tone Phase	Transmit Signal Path State	Transmit Signal Path Condition
Tone	1	0	1	active	0°	open	Inverted
Tone	1	0	0	active	180°	open	Inverted
Notone	0	0	X	bias	X	open	Not Inverted
Tone	1	1	1	active	0°	open	Not Inverted
Tone	1	1	0	active	180°	open	Not Inverted
Notone	0	1	X	bias	X	open	Not Inverted

Notes

1. The pre- and de-emphasis circuits remain in the Transmit path during Clear and Private operation.
2. Power remains applied to the CTCSS tone decoder at all times.
3. Carrier Frequency = 3333Hz during Private operation (Tx or Rx).
4. During Clear operation the carrier frequency is turned off to reduce spurious emissions.
5. Under Rx-Notone conditions the Notone output can be used to operate squelch circuitry.
6. The functions in this table are applicable when the device is connected as recommended in Figure 2.

Table 1 Functions and Outputs

Operational Information

The logical inputs ($D_0 - D_5$) are used to programme the FX375 tone frequency (Rx/$\overline{Tx}$) as shown in Table 2 (below). Loading of data is carried out in either serial or parallel formats.

Nominal Frequency (Hz)	FX375 Frequency (Hz)	Δfo (%)	Tone Data Programme Inputs					
			D_0	D_1	D_2	D_3	D_4	D_5
67.0	67.05	+ 0.07	1	1	1	1	1	1
71.9	71.9	0	1	1	1	1	1	0
74.4	74.35	- 0.07	0	1	1	1	1	1
77.0	76.96	- 0.05	1	1	1	1	0	0
79.7	79.77	+ 0.09	1	0	1	1	1	1
82.5	82.59	+ 0.1	0	1	1	1	1	0
85.4	85.38	- 0.02	0	0	1	1	1	1
88.5	88.61	+ 0.13	0	1	1	1	0	0
91.5	91.58	+ 0.09	1	1	0	1	1	1
94.8	94.76	- 0.04	1	0	1	1	1	0
97.4	97.29	- 0.11	0	1	0	1	1	1
100.0	99.96	- 0.04	1	0	1	1	0	0
103.5	103.43	- 0.07	0	0	1	1	1	0
107.2	107.15	- 0.05	0	0	1	1	0	0
110.9	110.77	- 0.12	1	1	0	1	1	0
114.8	114.64	- 0.14	1	1	0	1	0	0
118.8	118.8	0	0	1	0	1	1	0
123.0	122.8	- 0.17	0	1	0	1	0	0
127.3	127.08	- 0.17	1	0	0	1	1	0
131.8	131.67	- 0.1	1	0	0	1	0	0
136.5	136.61	+ 0.08	0	0	0	1	1	0
141.3	141.32	+ 0.02	0	0	0	1	0	0
146.2	146.37	+ 0.12	1	1	1	0	1	0
151.4	151.09	- 0.2	1	1	1	0	0	0
156.7	156.88	+ 0.11	0	1	1	0	1	0
162.2	162.31	+ 0.07	0	1	1	0	0	0
167.9	168.14	+ 0.14	1	0	1	0	1	0
173.8	173.48	- 0.19	1	0	1	0	0	0
179.9	180.15	+ 0.14	0	0	1	0	1	0
186.2	186.29	+ 0.05	0	0	1	0	0	0
192.8	192.86	+ 0.03	1	1	0	0	1	0
203.5	203.65	+ 0.07	1	1	0	0	0	0
210.7	210.17	- 0.25	0	1	0	0	1	0
218.1	218.58	+ 0.22	0	1	0	0	0	0
225.7	226.12	+ 0.18	1	0	0	0	1	0
233.6	234.19	+ 0.25	1	0	0	0	0	0
241.8	241.08	- 0.30	0	0	0	0	1	0
250.3	250.28	- 0.01	0	0	0	0	0	0
Serial Input Mode			X	X	Clk	Data	0	1
Notone			0	0	0	0	1	1

Table 2 Tone Programming

Load/$\overline{Latch}$ and Control Functions – The Load/$\overline{Latch}$ function regulates the loading of the FX375 tone frequency ($D_0 - D_5$, Table 2) in either the serial or parallel modes. The Control input enables the flexible use of the Rx/$\overline{Tx}$ and $\overline{Private\ Enable}$ functions, its use is illustrated in Table 3.

Load Configuration	Load/$\overline{Latch}$ *Logic*	*and*	Control *Logic*	Loading mode of :- $D_0 - D_5$	Loading mode of :- Rx/Tx, Private Enable
Parallel	1		0	Transparent	Transparent
Parallel	0		0	Latched	Latched
Parallel	1		1	Transparent	Transparent
Parallel	0		1	Latched	Transparent
Serial	0		1	Load data in	Transparent
Serial	0 – 1 – 0		0	Latch data in	Latched

Notes

Glossary – Transparent — Data at the device inputs acts directly.
Latched — In this position data and/or functions are latched in.

'0 – 1 – 0' is a strobe pulse as shown in figures 3 and 4 (Timing).

Table 3 Load/$\overline{Latch}$ and Control Functions

Timing Information... Control instructions are input to the FX375 by serial (figure 3) or parallel (figure 4) means, using Data Inputs and Load/$\overline{\text{Latch}}$ as shown in the diagrams below.

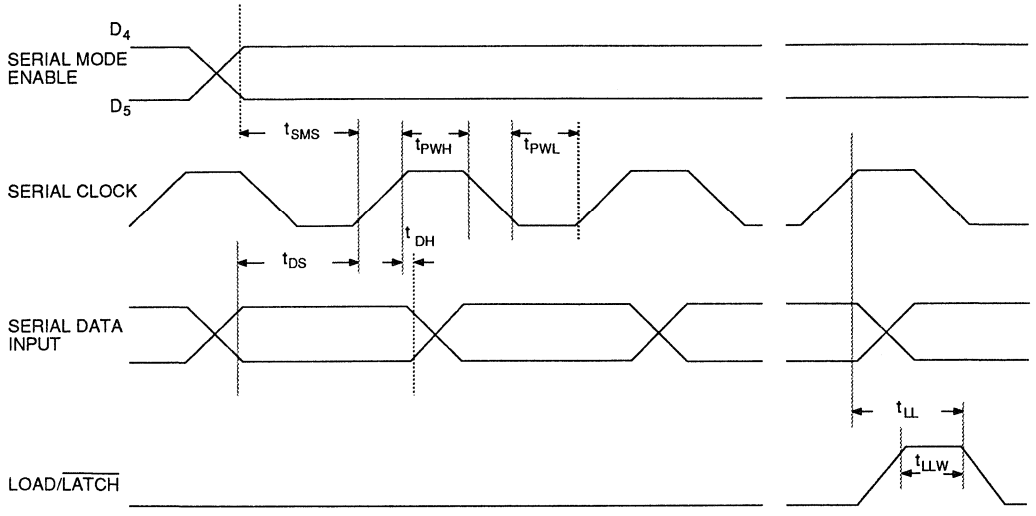


Fig.3 Serial Load Timing

		Min.	Typ.	Max.	Unit
Serial	Figure 3				
Serial Mode Enable Set Up Time – (t_{SMS})		250	–	–	ns
Clock 'High' Pulse Width – (t_{pWH})		250	–	–	ns
Clock 'Low' Pulse Width – (t_{pWL})		250	–	–	ns
Data Set Up Time – (t_{DS})		150	–	–	ns
Data Hold Time – (t_{DH})		50	–	–	ns
Load/$\overline{\text{Latch}}$ Set Up Time – (t_{LL})		250	–	–	ns
Load/$\overline{\text{Latch}}$ Pulse Width – (t_{LLW})		150	–	–	ns
Parallel	Figure 4				
Data Valid Time – (t_{VP})		200	–	–	ns
Load Time – (t_L)		150	–	–	ns
Fall Time – (t_F)		–	–	50	ns
Data Hold Time – (t_H)		50	–	–	ns

Serial Loading Sequence : With Load/$\overline{\text{Latch}}$ at logic '0' serial data is loaded in the sequence :- **D_5, D_4, D_3, D_2, D_1, D_0, Rx/$\overline{\text{Tx}}$, $\overline{\text{Private Enable}}$.** When these 8 bits have been clocked in on the rising clock edge, data is latched by strobing the Load/$\overline{\text{Latch}}$ input – " 0 – 1 – 0 " (Figure 3).

Table 4 Timing

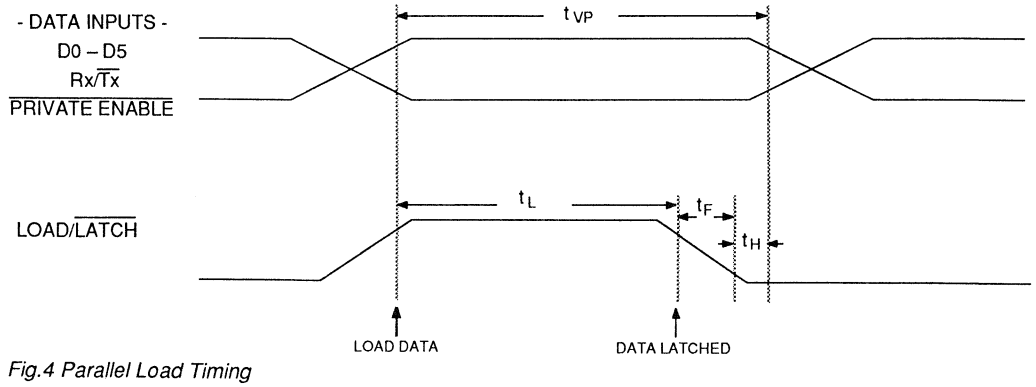


Fig.4 Parallel Load Timing

Private Squelch Circuit... Application Notes

The FX375 Private Squelch Circuit utilizes Audio Frequency Inversion and Continuous Tone Controlled Squelch System (CTCSS) techniques to provide secure voice communication on a common radio channel.

Clear/Private Switching is controlled by the logic state of the Private Enable input. Table 1 shows that, in the receive condition the signal path will only be inverted when the programmed CTCSS tone is received. Although other logic actions will enable the receive path, privacy of the conversation is maintained at all times.

Pre- and De-emphasis (6dB/octave) filters are included on-chip in the transmit path, so that the use of this device will produce natural sounding audio (clear or private modes) when installed in modern radio communication transceivers, with or without existing audio processing circuitry. The recommended layout is shown in block form below.

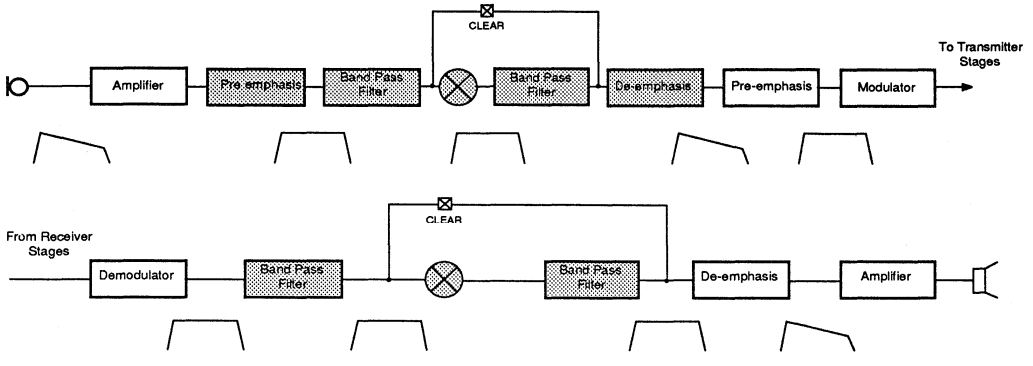


Fig.5 The Private Squelch Circuit Installed within a Typical Audio Stage

Figure 5 shows the recommended positioning of the FX375 (shaded areas) when installed within the audio stages of a typical transceiver system. The accompanying waveform diagrams indicate the relative "voice band amplitudes" at each stage of the receive or transmit process.

Installation Recommendations – Care should be taken on the design and layout of the printed circuit board taking into consideration the points noted below.

(a) All external components (as recommended in Figure 2) should be kept close to the package.

(b) Tracks should be kept short, particularly the Audio and V_{BIAS} inputs.

(c) Xtal/clock and digital tracks should be kept well away from analogue inputs and outputs.

(d) Inputs and outputs should be screened wherever possible.

(e) A "ground plane" connected to V_{SS} will assist in eliminating external pick-up on input and output pins.

(f) It is recommended that the power supply rails have less than 1mV rms of noise allowed.

(g) Tx Tone Output loading – Large capacitive loads could cause this pin to oscillate. If capacitive loads in excess of 100pF are unavoidable, a resistor of 1kΩ or greater put in series with the load should minimise this effect.

Specification

Electrical Characteristics

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		- 0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		- 0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX375J**	- 30°C to + 85°C (ceramic)
	FX375LG/LS	- 30°C to + 70°C (plastic)
Storage temperature range:	**FX375J**	- 55°C to + 125°C (ceramic)
	FX375LG/LS	- 40°C to + 85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:
V_{DD} = 5.0V, T_{AMB} = 25°C, Xtal/Clock f_0 = 4.0 MHz, Audio level 0dB ref: = 300mV rms.
Composite input signal = 0dB, 1kHz tone in –12dB (6kHz band limited) gaussian white noise with a –20dB CTCSS tone.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current :					
Rx /Tx (Operating)		–	8.0	–	mA
Rx standby (No Decode)		–	2.8	–	mA
Rx only (Decoding)		–	5.0	–	mA
Analogue Input Impedance		–	0.5	–	MΩ
Analogue Output Impedance		–	0.5	–	kΩ
Tone Input Impedance		–	1.0	–	MΩ
Digital Input Impedance		–	1.0	–	MΩ
Input Logic '1'		3.5	–	–	V
Input Logic '0'		–	–	1.5	V
Output Logic '1' (I = 0.1mA)		4.0	–	–	V
Output Logic '0' (I = 0.1mA)		–	–	1.0	V
Dynamic Values					
Maximum Input Level		–	+ 10.5	–	dB
Decoder					
Tone Input Signal Level	1,4	- 20	–	–	dB
Response Time	1,4,6	–	–	250	ms
De-response Time	1,4,6	–	–	250	ms
Selectivity	4	± 0.5	–	± 3.0	%f_o
Encoder					
Tone Output Level (relative 775mVrms)		- 3.0	0	+ 3.0	dB
Tone Frequency Accuracy		- 0.3	–	+ 0.3	%f_o
Tone Harmonic Distortion		–	2.0	5.0	%
Tone Output Load Current	2	–	–	5.0	mA
Output Level Variation between Tones		–	0.1	–	dB
Rise Time (to 90% nominal level)					
(f_o >100Hz)	5	–	15	–	ms
(f_o <100Hz)	5	–	45	–	ms

Specification

Frequency Characteristics

Characteristics	See Note	Min.	Typ.	Max.	Unit
Rx Clear					
Total Harmonic Distortion	3	–	2	5	%
Output Noise Level	7	–	- 43	–	dB
Passband Gain (300Hz – 3033Hz)		–	0	–	dB
Passband Ripple (300Hz – 3033Hz)	3	–	–	3	dB
Audio Stopband Attenuation					
($f$in > 3333Hz)		–	20	–	dB
($f$in > 3633Hz)		–	45	–	dB
($f$in < 250Hz)		–	42	–	dB
Rx Invert					
Carrier Frequency		–	3333	–	Hz
Total Harmonic Distortion	3,8	–	4	10	%
Baseband Breakthrough		–	- 40	–	dB
Carrier Breakthrough		–	- 40	–	dB
Output Noise Level	7	–	- 37	–	dB
Passband Ripple (300Hz – 3033Hz)	8	–	–	5	dB
Audio Stopband Attenuation					
($f$in > 3333Hz)		–	50	–	dB
($f$in > 3633Hz)		–	60	–	dB
($f$in < 250Hz)		–	60	–	dB
Tx Clear					
Total Harmonic Distortion	3	–	3	5	%
Output Noise Level	7	–	- 43	–	dB
Passband Gain (300Hz – 3033Hz)	3	–	0	–	dB
Passband Ripple (300Hz – 3033Hz)	3	–	–	4	dB
Audio Stopband Attenuation					
($f$in > 3333Hz)		–	20	–	dB
($f$in > 3633Hz)		–	45	–	dB
($f$in < 250Hz)		–	42	–	dB
Pre- and De-emphasis		–	–	6	dB/octave
Tx Invert					
Carrier Frequency		–	3333	–	Hz
Total Harmonic Distortion	3,8	–	4	10	%
Baseband Breakthrough		–	- 40	–	dB
Carrier Breakthrough		–	- 40	–	dB
Output Noise Level	7	–	- 37	–	dB
Passband Ripple (300Hz – 3033Hz)	3,8	–	–	5	dB
Audio Stopband Attenuation					
($f$in > 3333Hz)	8	–	50	–	dB
($f$in > 3633Hz)	8	–	60	–	dB
($f$in < 250Hz)	8	–	60	–	dB
Pre- and De-emphasis		–	–	6	dB/octave

Notes

1. These values are obtained using the external integrator components as detailed in Figure 2.
2. An Emitter Follower output.
3. With an input signal of 1kHz @ 0dB.
4. Under Composite Signal test conditions.
5. Any programmed tone with RL = 600, CL = 15pF. Including any response to a phase reversal instruction.
6. fo > 100Hz, (for 100Hz > fo > 67Hz : t = [100/fo (Hz)] x 250ms).
7. Input a.c. short circuit, audio path enabled, measured in a 30kHz bandwidth.
8. Due to frequency inversion, this figures reflects the difference from the expected ideal response.

Package Outlines

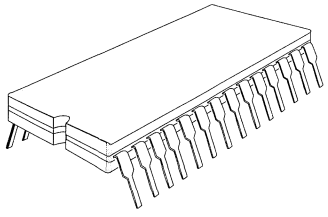
The FX375 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX375 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX375J 28-pin cerdip DIL (J5)

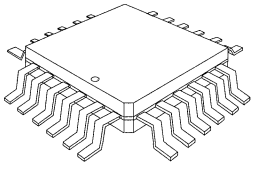
NOT TO SCALE



Max. Body Length 37.05mm
Max. Body Width 13.36mm

FX375LG 24-pin quad plastic encapsulated bent and cropped (L1)

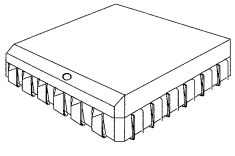
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX375LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX375J	28-pin cerdip DIL	(J5)
FX375LG	24-pin encapsulated bent and cropped	(L1)
FX375LS	24-lead plastic leaded chip carrier	(L2)

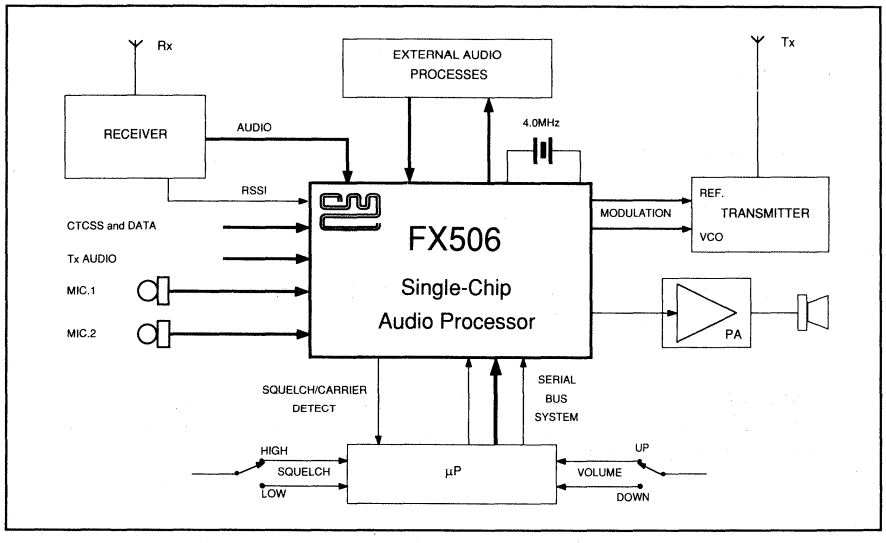
CML Semiconductor Products
PRODUCT INFORMATION

FX506 Mobile Radio Audio Processor

Publication D/506/3 July 1994
Provisional Issue

Features/Applications

- **Full Rx and Tx Filtering to CEPT Standards**
- **Digital Control of Volume, Noise Squelch and R.S.S.I.**
- **Tx VOGAD Circuitry**
- **Serial μP Control of ALL Chip Functions**
- **Deviation Limiter**
- **Military/Marine and Mobile Radio Applications**
- **FM/AM/SSB Applications**
- **16-kbit Data and Voice Scrambler Compatible**
- **Low-Power 5-Volt CMOS Process**



FX506

Brief Description

The FX506 is a μProcessor-controlled, single-chip device containing ALL the circuit elements necessary to perform the audio functions of a mobile (or portable) radio system.

On-chip signal paths include: speech-band/pre-emphasis filters, variable gain/attenuation stages, voice-compression and deviation limiter circuitry.

Each function in the signal path can be addressed or by-passed — *providing "real-time," dynamic control* — by the μProcessor. This half-duplex device comprises two separate audio signal paths.

The Pre-Process Path performs filtering and level adjustment on audio (Rx or Tx) for use in auxiliary systems such as "Frequency Inversion Scrambling," "Sub-Audio" tone or "In-Band" data signalling. This path is output at the "Pre-Process Audio Output" pin. If no external processes are being used this output should be connected to the "Pre-process Audio Input" pin.

The Post-Process Path can adjust and prepare the input audio for output to the chosen transmitter driver or loudspeaker amplifier.

Suitably software configured, the FX506, which can operate on voice, direct-digital or tone-data and sub-audio frequencies, is compatible with FM, AM and SSB type transceivers. Digital gain elements are provided on-chip for dynamic control and balance of signal-path levels during manufacturing, test and operation.

System Squelch, a separate path, is sourced from either the incoming signal or Received Signal Strength Indication (R.S.S.I.) from the radio circuitry.

The FX506, a low-power 5-volt CMOS device, is available in 24-pin/lead plastic DIL and SMD packages.

Pin Number Function

DIL FX506P	Quad FX506LG FX506LS	
1		**$\overline{\text{Xtal}}$:** The output of the 4.0MHz on-chip clock oscillator.
2		**Xtal/Clock:** The input to the on-chip 4.0MHz clock oscillator inverter. All oscillator components are included on-chip. A 4.0MHz Xtal or externally derived clock should be connected here. See Figure 2.
3		**V_{DD}:** Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the Audio Processor are dependent upon this supply.
4		**Post Process Audio Input:** The analogue input to the Post-Process Path from external audio operations. Inputs to this pin should be a.c. coupled via a capacitor C_7. See Figures 2 and 4.
5		**Pre-Process Audio Output:** The analogue output to external audio operations. See Figure 4.
6		**Rx Audio Input:** The input from the radio receiver demodulator. This input, which requires to be a.c. coupled via capacitor C_6, is selected by serial data. Audio at this input will be available for use as a signal-squelch noise source. See Figures 2 and 4.
7		**V_{BIAS}:** The output of the on-chip analogue bias circuitry, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} via capacitor C_1. See Figure 2.
8		**CTCSS/Data Input:** To allow the introduction of sub-audio tones or data to the VCO drives. By manipulation of bits 17, 18 and 19 this input can be "mixed" into the signal path or added as a burst in between speech segments.
9		**Tx Audio Input:** The pre-process transmit audio input. This input can be driven from an external source or from the FX506 Mic. input circuitry. See Figures 2, 3 and 4.
10		**Mic. Output:** The output of the microphone multiplexer, selected by serial input data. If additional gain is required for the pre-process input, an external amplifier as shown in Figure 3 is recommended.
11		**Mic.1 Input:** These separate microphone audio inputs are individually selected by the serial input data. See Figures 2, 3 and 4.
12		**Mic.2 Input:**
13		**V_{SS}:** Negative supply rail (GND).

Pin Number DIL FX506P	Pin Number Quad FX506LG FX506LS	Function
	14	**Compression Capacitor:** External components connected to this pin provide the required compression time-constant. See Figure 2.
	15	**Audio Output (Rx):** The received audio output from the Post-Process path. This output is data selected and when powersaved is held at V_{BIAS}.
	16	**VCO Ref. Drive (Tx) Output:** The output to drive the modulation reference oscillator. This output is data selected and when powersaved is held at V_{BIAS}. To prevent any d.c. level at this output causing incorrect frequency selection it is recommended that a.c. coupling components as shown in Figure 2 are employed. For modulation down to near d.c., these components should be by-passed.
	17	**VCO Drive (Tx) Output:** The output to drive the modulation VCO. This output is data selected and when powersaved is held at V_{BIAS}.
	18	**R.S.S.I.:** The input to the Squelch Selection circuitry from the radio's Received Signal Strength Indicator output. A data selected input.
	19	**Noise Input:** The noise level can be applied to this pin. This would be the Noise Output integrated by external components, as indicated in Figure 2, or an externally produced noise level.
	20	**Noise Output:** The output of the on-chip "squelch noise rectifier." This output is a half-wave rectified d.c. level that can be applied to the Noise Input via external integrating components. This output could also be used by an external signal detector circuit. This output level is at V_{BIAS} for no input. See Figures 2, 3 and 4.
	21	**Squelch Drive:** A TTL compatible output. The inputs to the comparator are: the logically selected threshold level from the Digital-to-Analogue converter and the selected noise input. A logic "0" signifies that the noise threshold has been exceeded.
	22	**Serial Clock:** The externally produced serial data loading clock input. See Figure 5. This input has an internal 1MΩ pullup resistor.
	23	**Serial Data:** The controlling, 47-bit serial data input. With $\overline{\text{Chip Select}}$ maintained at a logic "0" the serial data is entered at this pin, loaded bit 46 first, bit 0 last. Detailed information on the allocation and function of serial data bits (0 to 46) is given in tabular form on later pages. Data load timing should be carried out as described in Figure 5. This input has an internal 1MΩ pullup resistor.
	24	**$\overline{\text{Chip Select}}$:** The data loading control function. During serial loading this input should be operated as shown in Figure 5. New data is latched on the rising edge of this waveform. This input has an internal 1MΩ pullup resistor.

External Components and Interfacing

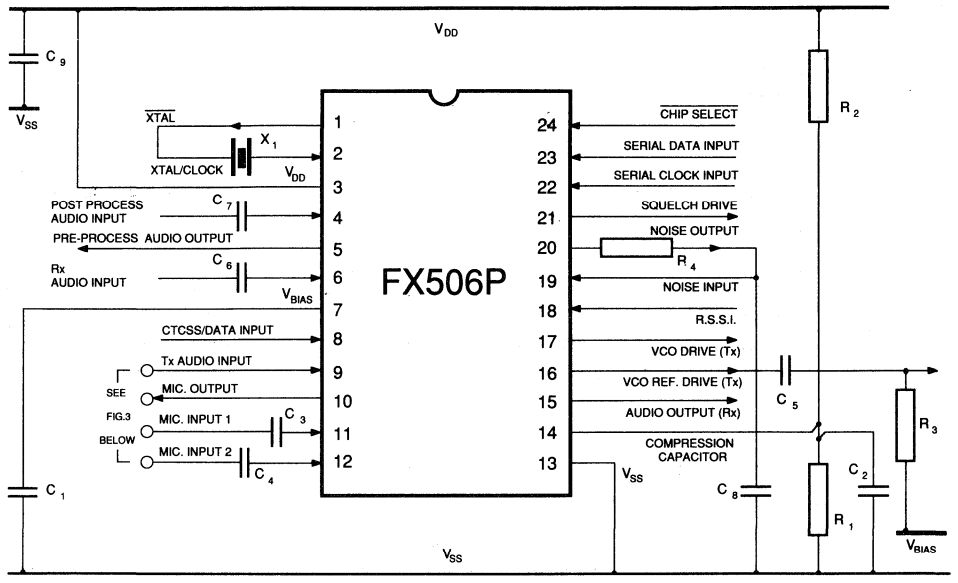


Fig.2 Recommended External Components

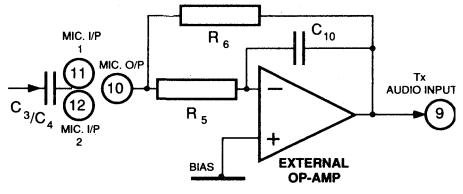


Fig.3 Typical 2nd Order Pre-emphasis Input Circuit

Notes

For dual Tx inputs using both Mic.1 and Mic.2 inputs without pre-emphasis, capacitors C_3 and C_4 will be required at the inputs as shown in Figure 2.

If pre-emphasis is required, the external circuit shown in Figure 3 is recommended.

The Op-Amp selected for this application should be of a "low noise wide-bandwidth" type i.e. with at least 60dB of gain at 6kHz.

In addition to the components shown in Figure 2, it is recommended that the power and V_{BIAS} lines to the external Op-Amp are decoupled to V_{SS} *physically close to the amplifier*, by a 1.0µF capacitor.

Circuit References

Component	Value	Tolerance						
R_1	100kΩ	±10%	C_1	1.0µF	±20%	C_7	0.1µF	±20%
R_2	390kΩ	±10%	C_2	6.8µF	±20%	C_8	0.1µF	±20%
R_3	100kΩ	±1%	C_3	1.0nF	±1%	C_9	1.0µF	±20%
R_4	10kΩ	±10%	C_4	1.0nF	±1%	C_{10}	12.0pF	±1%
R_5	18.0kΩ	±1%	C_5	15nF	±1%			
R_6	2.7MΩ	±1%	C_6	0.1µF	±20%	X_1	4.0MHz	

Layout Recommendations

Audio microcircuit performance will be affected by external noise.

All external components should be kept as close to the device as possible.

Tracks to the device should be kept short, particularly the Audio and V_{BIAS} inputs.

A "ground-plane" connected to V_{SS} will help to eliminate external pick-up.

Ensure that all inputs (analogue and d.c.) are free from noise.

Xtal/clock and digital tracks should be kept well away from analogue circuitry. Analogue inputs and outputs should be screened wherever possible with high-level outputs isolated from very low-level inputs.

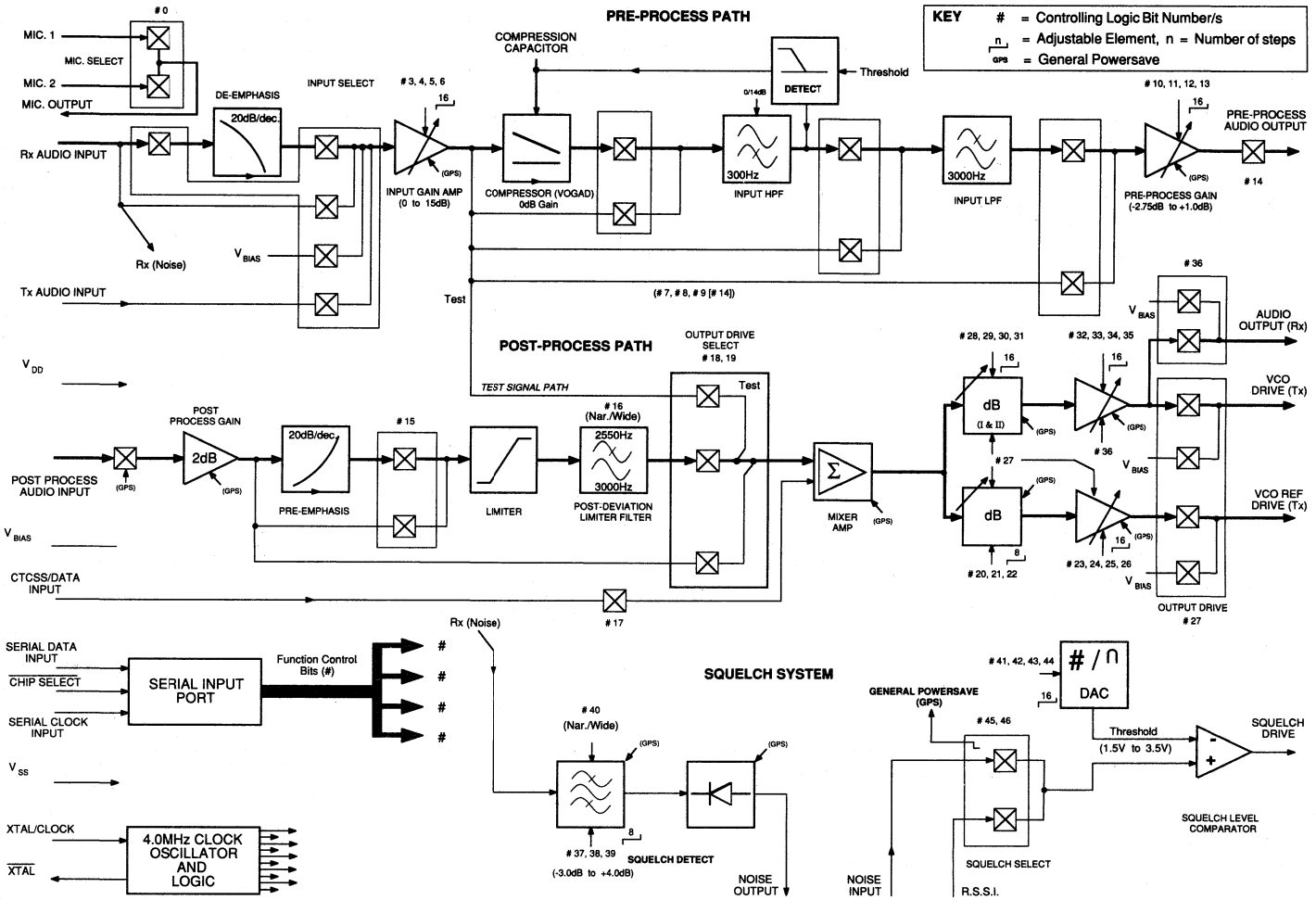


Fig.4 PMR Audio Processor – Facilities

Control bits	Function	Notes
(LSB) loaded last		
0	**Mic. Select**	A multiplexed "microphone" input allowing the use of differing type and level voice inputs.
0	– Microphone Input 1	
1	– Microphone Input 2	
1 2	**Input Select**	Transmit or receive audio sources are selected, inserting the appropriate path gain for the chosen input. The input path can be set to bias whilst allowing receiver noise monitoring.
0 0	– Rx Input De-emphasis Bypass; HPF to 0dB	
0 1	– Rx Input De-emphasis Select; HPF to 0dB	
1 0	– Tx Input Powersave De-emphasis; HPF to 14dB	
1 1	– Path Input to V_{BIAS}; Powersave De-emphasis	
3 4 5 6	**Input Gain Amplifier**	A gain element intended to adjust the drive level to the compressor, catering for differing signal sources and microphone sensitivities.
0 0 0 0	– Gain Set 0.0dB	
1 0 0 0	1.0dB	
0 1 0 0	2.0dB	
1 1 0 0	3.0dB	
0 0 1 0	4.0dB	
1 0 1 0	5.0dB	
0 1 1 0	6.0dB	
1 1 1 0	7.0dB	
0 0 0 1	8.0dB	
1 0 0 1	9.0dB	
0 1 0 1	10.0dB	
1 1 0 1	11.0dB	
0 0 1 1	12.0dB	
1 0 1 1	13.0dB	
0 1 1 1	14.0dB	
1 1 1 1	15.0dB	

7 8 9 14	***Compressor***	***HPF***	***LPF***	***Pre-Process Output***
1 1 1 ***1***	Enabled	Enabled	Enabled	Enabled
0 1 1 ***1***	Powersaved	Enabled	Enabled	Enabled
X 0 1 ***1***	Powersaved	Powersaved	Enabled	Enabled
X X 0 ***1***	Powersaved	Powersaved	Powersaved	Enabled
X X X ***0***	Powersaved	Powersaved	Powersaved	Powersaved

The Pre-Process Path LPF should be selected whilst CEPT 'Response to the Tx to Mod. frequencies exceeding 3kHz' tests are carried out.

10 11 12 13	**Pre-Process Gain**	An in-line output drive stage providing adjustable gain or attenuation to compensate for level tolerances in the external audio processes and peripherals. The output of this amplifier stage is available for further voice (audio) processing such as "Frequency Inversion Voice Scrambling."
0 0 0 0	– Gain Set -2.75dB	
1 0 0 0	-2.50dB	
0 1 0 0	-2.25dB	
1 1 0 0	-2.00dB	
0 0 1 0	-1.75dB	
1 0 1 0	-1.50dB	
0 1 1 0	-1.25dB	
1 1 1 0	-1.00dB	
0 0 0 1	-0.75dB	
1 0 0 1	-0.50dB	
0 1 0 1	-0.25dB	
1 1 0 1	0dB	
0 0 1 1	0.25dB	
1 0 1 1	0.50dB	
0 1 1 1	0.75dB	
1 1 1 1	1.00dB	
14	**Pre-Process Output**	Bit 14 is the Enable/Powersave function for the Pre-Process output stages. See *Bits 7 8 9 14 .....*
0	– Disable Pre-Process Output Output at V_{BIAS}	
1	– Enable Pre-Process Audio Output	*Reference ..... Figure 4*

Control bits	Element	Notes
	Post-Process Gain	A fixed 2.0dB gain stage.
15	**Pre-emphasis**	A selectable pre-emphasis stage set around 1.0kHz, with a characteristic of 6dB per octave. It is available for use when transmitting data signals such as FFSK. See Table below for Powersave information.
	Deviation Limiter	A pre-set amplitude limiting stage for deviation control.
	and	
16	**Post-Deviation Limiter Filter**	This lowpass filter which is selected with the Deviation Limiter, is adjustable to Narrow (2550Hz) and Wide (3000Hz) bandwidths, allowing for different channel-spacing requirements.
0	– Narrow filter bandwidth, cut-off = 2550Hz.	
1	– Wide filter bandwidth, cut-off = 3000Hz.	
17	**CTCSS/Data Input**	
0	– Disable Input path to Mixer system	
1	– Enable Input path to Mixer system	

15	*18*	*19*	*Pre-Emphasis*	*Limiter and Post-Dev LPF*	*Drive Selected*
X	0	0	Powersaved	Powersaved	Test Path
0	1	0	Powersaved	Enabled	Post-ProcessPath
1	1	0	Enabled	Enabled	Post-Process Path
X	1	1	Powersaved	Powersaved	Post-Process Bypass
X	0	1	Powersaved	Powersaved	Bias

20	*21*	*22*	**VCO Reference Drive Attenuator**	
			– Gain Set	
0	0	0		-28dB
1	0	0		-24dB
0	1	0		-20dB
1	1	0		-16dB
0	0	1		-12dB
1	0	1		-8.0dB
0	1	1		-4.0dB
1	1	1		0.0dB

The in-line control attenuator for the VCO reference channel drive output.

23	*24*	*25*	*26*	**VCO Reference Drive Amplifier**	
				– Gain Set	
0	0	0	0		-2.75dB
1	0	0	0		-2.50dB
0	1	0	0		-2.25dB
1	1	0	0		-2.00dB
0	0	1	0		-1.75dB
1	0	1	0		-1.50dB
0	1	1	0		-1.25dB
1	1	1	0		-1.00dB
0	0	0	1		-0.75dB
1	0	0	1		-0.50dB
0	1	0	1		-0.25dB
1	1	0	1		0dB
0	0	1	1		0.25dB
1	0	1	1		0.50dB
0	1	1	1		0.75dB
1	1	1	1		1.00dB

The in-line control amplifier/attenuator for the VCO reference channel drive output.

27	**Output Drive Control**	Used in conjunction with Bit 36 to control output functions.

Reference ..... Figure 4

Control bits	Element	Notes
28 29 30	**VCO Drive Attenuator I**	
0 0 0	– Gain Set -22.4dB	An in-line control attenuator for the VCO Tx channel drive output.
1 0 0	-19.2dB	
0 1 0	-16.0dB	
1 1 0	-12.8dB	This channel is also selected as Audio Output (Rx) under the control of bit 36. This attenuator can be used in a volume control application.
0 0 1	-9.6dB	
1 0 1	-6.4dB	
0 1 1	-3.2dB	
1 1 1	0dB	
31	**VCO Drive Attenuator II**	An in-line control attenuator for the VCO Tx channel drive output. As an example, when bits 28 to 31 are set to "0," the gain set is -48.0dB (-22.4 + -25.6).
0	– Gain Set -25.6dB	
1	0dB	
32 33 34 35	**VCO Drive Amplifier**	The in-line control amplifier/attenuator for the VCO Tx channel drive output. This channel is also selected as Audio Output (Rx) under the control of bit 36. This amplifier can be used in a volume control application.
0 0 0 0	– Gain Set -2.75dB	
1 0 0 0	-2.50dB	
0 1 0 0	-2.25dB	
1 1 0 0	-2.00dB	
0 0 1 0	-1.75dB	
1 0 1 0	-1.50dB	
0 1 1 0	-1.25dB	
1 1 1 0	-1.00dB	
0 0 0 1	-0.75dB	
1 0 0 1	-0.50dB	
0 1 0 1	-0.25dB	
1 1 0 1	0dB	
0 0 1 1	0.25dB	
1 0 1 1	0.50dB	
0 1 1 1	0.75dB	
1 1 1 1	1.00dB	

27 36	***VCO Drive (Tx) Output***	***VCO Ref (Tx) Output***	***Audio Output (Rx)***
0 0	Bias	Bias	Bias
0 1	Bias	Bias	Enabled
1 0	Enabled	Enabled	Bias
1 1	Enabled	Enabled	Enabled

The Drive and Ref. paths are powersaved by Bits 45 and 46 in the "Total Powersave" or "Listening Powersave" conditions. When making internal changes it is recommended that these outputs are disconnected *(placed in a bias condition)* from the relevant output (load) circuitry.

37 38 39	**Squelch Filter (Gain)**	The squelch function is set by bits 45 & 46 (Squelch Source Selection). The centre frequency gain of this element is 35dB, data selected gain variations (-3.0dB to 4.0dB) are around this value.
0 0 0	– Gain Set -3.0dB	
1 0 0	-2.0dB	
0 1 0	-1.0dB	
1 1 0	0dB	
0 0 1	1.0dB	
1 0 1	2.0dB	
0 1 1	3.0dB	
1 1 1	4.0dB	
40	**Squelch Filter** (Narrow/Wide)	For use in wide or narrow channel systems. The squelch function is set by bits 45 & 46 (Squelch Source Selection).
0	– Narrow ($fc \approx 18kHz \pm 6.5kHz$).	
1	– Wide ($fc \approx 25kHz \pm 8.5kHz$).	

Reference ..... Figure 4

Control bits				Element		Notes
41	*42*	*43*	*44*	**Squelch Threshold Voltage**		The fine squelch adjustment level from the Digital-to-Analogue converter. These threshold levels are used as a comparison with the selected input noise voltage (bits 45 and 46). Variation in V_{DD} will produce variation in threshold levels.
0	0	0	0	3.500V d.c.	70.0% V_{DD}	
1	0	0	0	3.366	67.3%	
0	1	0	0	3.233	64.6%	
1	1	0	0	3.100	62.0%	
0	0	1	0	2.966	59.3%	
1	0	1	0	2.833	56.6%	
0	1	1	0	2.700	54.0%	
1	1	1	0	2.566	51.3%	
0	0	0	1	2.433	48.6%	
1	0	0	1	2.300	46.0%	
0	1	0	1	2.166	43.3%	
1	1	0	1	2.033	40.6%	
0	0	1	1	1.900	38.0%	
1	0	1	1	1.766	35.3%	
0	1	1	1	1.633	32.6%	
1	1	1	1	1.500	30.0%	
	45	*46*		**Squelch Source Selector**		As well as selecting the input to the Noise Comparator, these two bits produce additional General Powersave (GPS) functions which control those elements not having individual serial control.
	0	0		A "Total Powersave" condition		**Powersaved:** Input Gain Amp – Post Process (2dB) Gain Amp – Mixer Amp – Noise BPF – Noise Rectifier – Squelch Comparator
	1	0		Noise Input selected to Comparator		
	0	1		R.S.S.I. input selected to Comparator		
	1	1		Powersave but LISTENING condition R.S.S.I. input selected to Comparator		**Powersaved:** Input Gain Amp – Post Process (2dB) Gain Amp – Mixer Amp – Noise BPF – Noise Rectifier

Rx Noise Path

Any high-frequency noise (18kHz/25kHz) present at the Rx Audio Input will also be available at the Noise Output pin via the squelch filter and noise rectifier (when enabled) for use as a squelch detection level. This means that the FX506 can be set to "LISTEN" with the majority of circuit elements powersaved until an R.S.S.I. level is detected and produces a "Squelch Drive output."

Test Signal Path

This path, when selected, can be used as a direct path, via the Output Drive Selector (bits 18 and 19), to dynamically set and balance the VCO drive and reference output levels.

Reference ..... Figure 4

Serial Control Bits – Loading and Timing Information

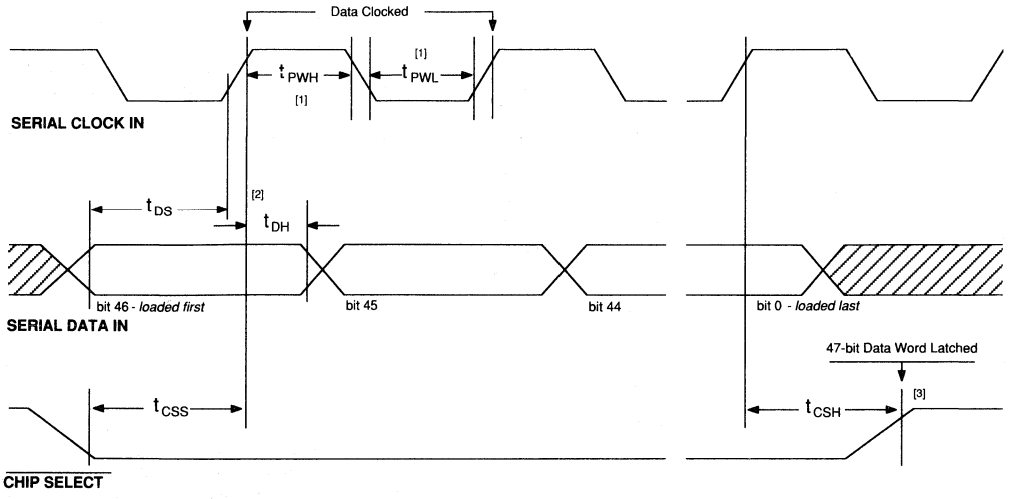


Fig.5 Data Load Timing Diagram

Data Loading

Serial Data bits, whose functions are described on the previous pages, are loaded to the FX506 using the timing format illustrated on this page. All 47 bits must be loaded. Data is loaded bit 46 first, bit 0 last.

Function			Min.	Typ.	Max.	Unit
Serial Clock	[1]					
'High' Pulse Width		t_{PWH}	600	–	–	ns
'Low' Pulse Width		t_{PWL}	600	–	–	ns
Serial Data	[2]					
Data Set-Up Time		t_{DS}	360	–	–	ns
Data Hold Time		t_{DH}	120	–	–	ns
$\overline{\text{Chip Select}}$	[3]					
Select Set-Up Time		t_{CSS}	600	–	–	ns
Select Hold Time		t_{CSH}	600	–	–	ns

[1] The Serial Clock pulses do not have to be symmetrical, as shown above, but pulse lengths must conform to the "minimum" time specification.

[2] Individual data bits (logic "1" or "0") are loaded to the device on the rising edge of the input Serial *Data* Clock pulse. The data hold period (t_{DH}) is to ensure that the data level is steady when it is sampled.

[3] The full 47-bit data word is latched into the device on the rising edge of the $\overline{\text{Chip Select}}$ waveform, at this time the loaded data is acted upon and the circuit configuration/settings will change.

System Response Characteristics

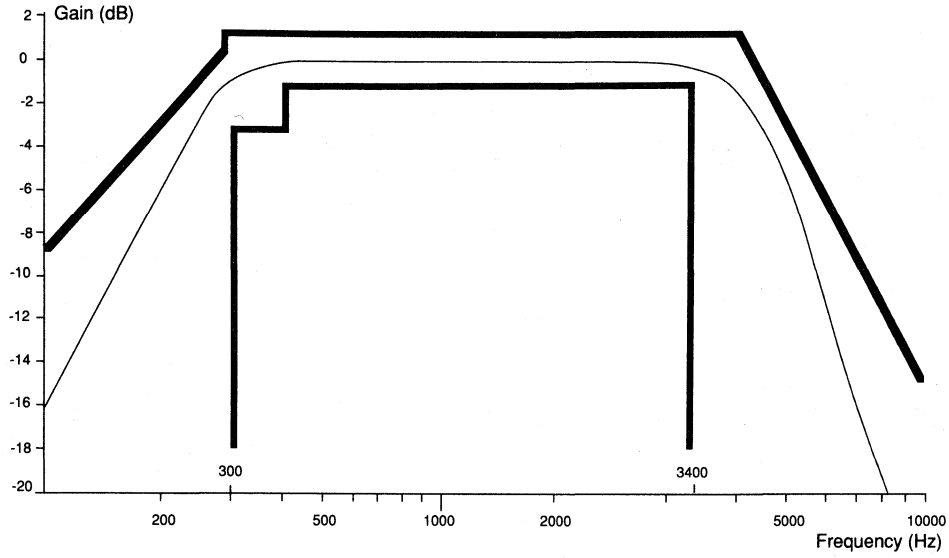


Fig.6 Typical Pre-Process Path Frequency Response

System Frequency Characteristics

Figure 6 shows a typical, response curve of the Pre-Process Path, in receive mode, set against the device specification. The general characteristic shape is produced by the Input Highpass and Lowpass Filters, without the internal pre-emphasis element.

Figure 7 shows a typical response curve of the Post-Process Path set against the device specification. The general characteristic shape is produced by the Post-Deviation Limiter Filter, without the de-emphasis element.

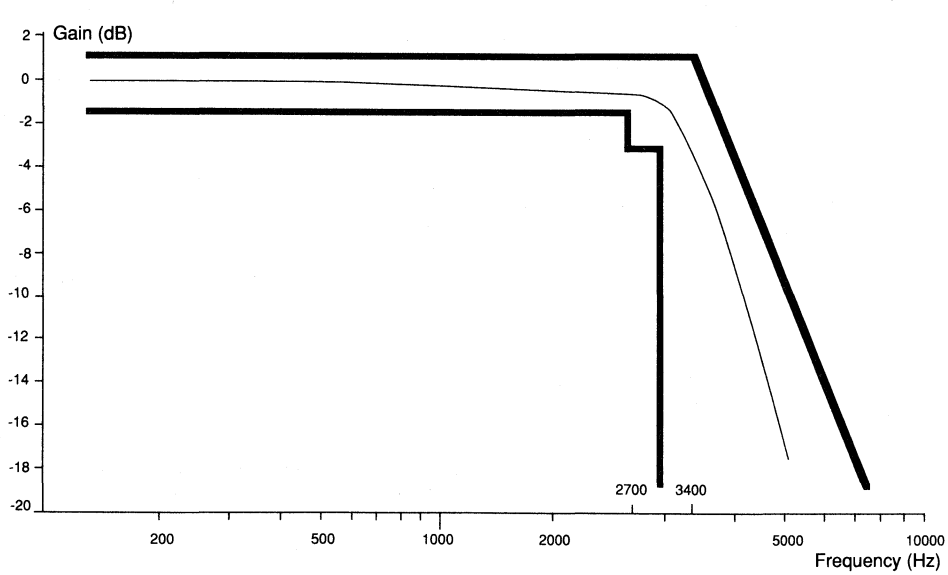


Fig.7 Typical Post-Process Path Frequency Response

Application Information .....

Suggested Evaluation Tests and Settings

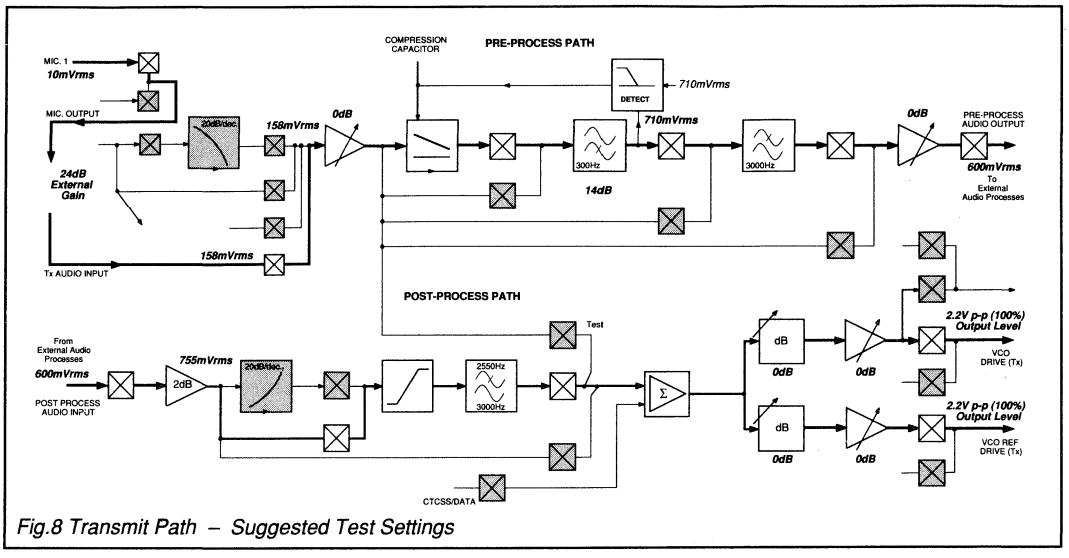


Fig.8 Transmit Path – Suggested Test Settings

Active elements used in the signal path.

Powersaved or by-passed elements that are not employed in the signal path.

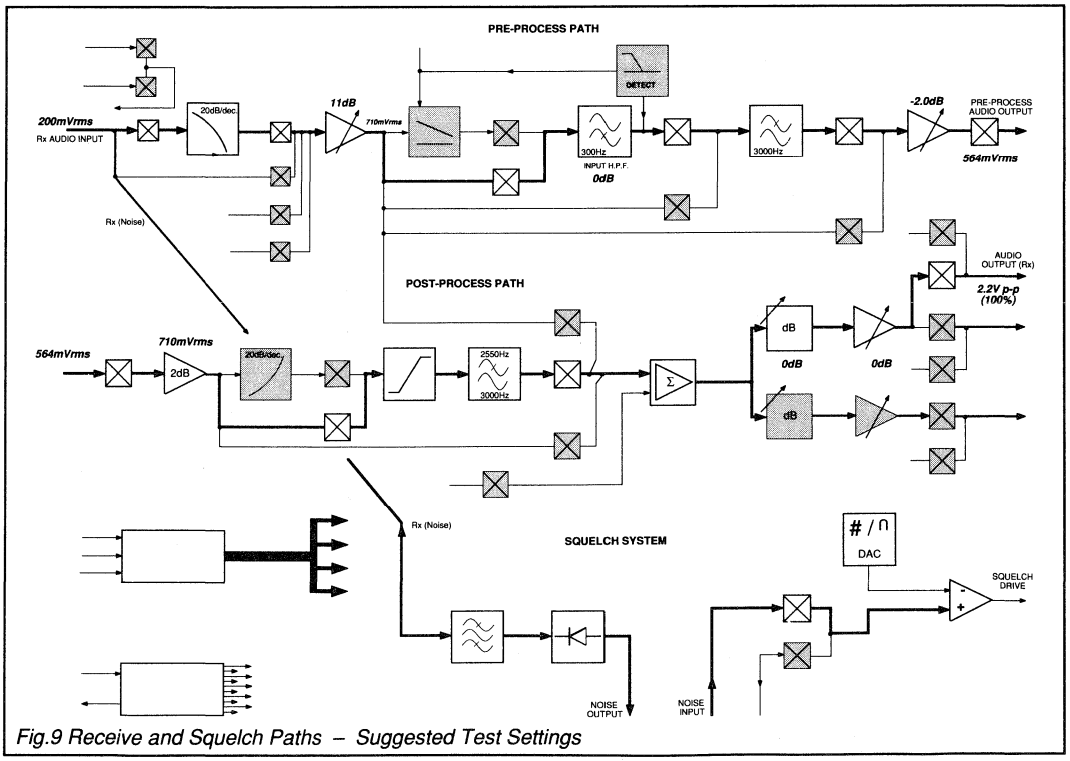


Fig.9 Receive and Squelch Paths – Suggested Test Settings

Application Information

Suggested Evaluation Tests and Settings

Operational Information

The functions of the FX506 are selected and controlled using the 47-bit Serial Data Input. This application section assists in the familiarization of control by providing example operational paths and system confidence tests.

The signal levels employed in these examples are to demonstrate the functions of the device. Maximum and minimum operational signal levels are detailed in the "Specification" pages. A final output signal level of 2.2V p-p is considered, operationally, to be 100% (FM deviation).

Set-up and enter the example data word in accordance with Figures 2 and 4.
Test the FX506 using levels and points detailed in Tables 1, 2 and 3.

Experimentation will indicate the signal element configuration and required control settings for various input and output levels.

Transmit Path – *The Serial Data word below will produce the transmit element configuration shown in Figure 8.*

bit 0 – **01000001 11110110 X0101111 10111111 11010XXX XXXXX10** – bit 46

0 = logic 0 **1** = logic 1 **X** = not important to the example

Step	Input	– Level (mV rms @ 1kHz)	Output	– Level (mV rms @ 1kHz)	Note	Output Level Ref. to Max.
1	Mic. 1	10	Pre-Process Audio	750	Ext +24.0dB	
2	Ext. Audio Process In	750	VCO Drive/Ref.	1.54≤ V_{OUT} ≤2.2Vp-p		70 – 100%
3	Mic. 1	4.8	Pre-Process Audio	410	Ext +24.0dB	60%
4	Ext. Audio Process In	410	VCO Drive and Ref.	466		60%

Table 1 Transmit Path Operational Check

To establish a 100% level for this device inject a large amplitude audio signal into the Post Process Audio Input, with the Limiter enabled.

Receive Path – *The Serial Data word below will produce the receive element configuration shown in Figure 9.*

bit 0 – **X0111010 11110010 X010XXXX XXX01111 11011XXX XXXXX10** – bit 46

0 = logic 0 **1** = logic 1 **X** = not important to the example

Step	Input	– Level (mV rms @ 1kHz)	Output	– Level (mV rms @ 1kHz)	Note	Output Level Ref. to Max.
1	Rx Audio In	200	Pre-Process Audio	564		
2	Ext. Audio Process In	564	Audio Out (Rx)	1.54≤ V_{OUT} ≤2.2Vp-p		70 -100%
3	Rx Audio In	145	Audio Out (Rx)	466		60%
4	Rx Audio In	145	Audio Out (Rx)	466±	vary bits 28 – 35 for Volume	60%±

Table 2 Receive Path Operational Check

To establish a 100% level for this device inject a large amplitude audio signal into the Post Process Audio Input, with the Limiter enabled.

Squelch Path – *The Serial Data word below will produce the squelch element configuration shown in Figure 9.*

bit 0 – **X00XXXXX XXXXXX0X X010XXXX XXX0XXXX XXXX1110 1110110** – bit 46

0 = logic 0 **1** = logic 1 **X** = not important to the example

Step	Input	– Level (mV rms @ 25kHz)	Output	– Level	Note
1	Rx Audio In	0	Squelch Drive	logic "1"	No noise – "Noise Out" = V_{BIAS}
2	Rx Audio In	50.0	Squelch Drive	logic "0"	Noise In – "Noise Out" decreases

Table 3 Squelch Path Operational Check

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX506P**	-30°C to +70°C (plastic)
	FX506LG/LS	-30°C to +70°C (plastic)
Storage temperature range:	**FX506P**	-40°C to +85°C (plastic)
	FX506LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.0MHz. Audio level 0dB ref: = 466mV rms @ 1.0kHz *(60% deviation, FM).*

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage			4.5	5.0	5.5	V
Supply Current	(All Elements Enabled)		–	8.0	–	mA
	(Listening Powersave)		–	–	1.0	mA
	(Maximum Powersave)		–	–	1.0	mA
Dynamic Values						
Input Logic "1"		1	3.5	–	–	V
Input Logic "0"		1	–	–	1.5	V
Input Impedances						
Digital			0.1	1.0	–	MΩ
Mic.1 or 2			–	0.5	–	kΩ
Rx Audio			30.0	–	–	kΩ
Tx Audio			30.0	56.0	–	kΩ
CTCSS/Data			50.0	100	–	kΩ
External Audio Process			1.0	–	–	MΩ
Noise, R.S.S.I.			1.0	–	–	MΩ
Output Impedances						
Pre-Process Audio			–	–	3.0	kΩ
Audio Out (Rx)			–	–	3.0	kΩ
VCO Drive and Ref. Out			–	–	3.0	kΩ
Squelch Drive	(Logic "1")		–	5.0	–	kΩ
	(Logic "0")		–	500	–	Ω
Noise Output	(Diode conducting)		–	1.0	–	kΩ
	(Diode not conducting)		–	500	–	kΩ
Signal Path Switch Isolation (Disabled)						
Switches			40.0	–	–	dB
Test Path			–	60.0	–	dB
Signal Input Levels		10				
Mic.1 or 2			1.0	–	100	mV rms
Rx Audio			–	145	200	mV rms
Tx Audio			–	–	1414	mV rms
CTCSS/Data			–	–	4.0	V p-p
Post Process			–	–	1123	mV rms
Noise, R.S.S.I.		2	–	–	4.0	V p-p
Signal Output Levels		10				
Pre-Process Audio	(Compressor enabled)		–	600	–	mV rms
VCO – (Drive, Ref.)	(Limiter in circuit)		–	2.2	–	V p-p
Audio (Rx)	(Limiter in circuit)		–	2.2	–	V p-p
Variable Element Step						
Input Gain Amp			0.7		1.3	dB
Pre-Process Gain			0.2		0.3	dB
VCO Ref. Attenuator			3.5		4.5	dB
VCO Drive Attenuator I			2.7		3.7	dB
VCO Drive Attenuator II			25.0		26.2	dB
VCO Amplifiers (Drive and Ref.)			0.2		0.3	dB

Specification .....

Characteristics		See Note	Min.	Typ.	Max.	Unit
Output Distortion						
Output Signal-to-Noise Ratio		3, 12	48.0	52.0	–	dBp
Total Harmonic Distortion Level		4, 11	–	-40.0	-30.0	dB
Compressor						
Dynamic Range			–	30.0	–	dB
Attack Time			–	7.0	–	ms
Decay Time			–	1000	–	ms
Deviation Limiter						
Input Thresholds		4	–	2.0	–	V p–p
Frequency Responses						
Pre-Process Path		6				
Passband Frequencies						
-3dB (Lower)			–	240	–	Hz
-3dB (Upper)			–	4.7	–	kHz
Passband Ripple	(300Hz - 400Hz)	5	-3.0	–	1.0	dB
	(400Hz - 3400Hz)	5	-1.5	–	1.0	dB
Stopband Attenuation	(f = 5kHz)		3.0	4.2	–	dB
High Frequency Roll-off	(f = >5kHz, <20kHz)		12.0	–	–	dB/oct.
Stopband Attenuation	(f = 250Hz)		–	2.3	–	dB
Low Frequency Roll-off	(f = <250Hz)		6.0	–	–	dB/oct.
Post-Process Path		7				
Wideband : Lowpass Frequency (-3dB)			–	3.4	–	kHz
Passband Ripple	(< 2700Hz)	8	-1.5	–	1.0	dB
	(2700Hz - 3000Hz)	8	-3.0	–	1.0	dB
Stopband Attenuation	(f = 5kHz)		12.2	17.0	–	dB
High Frequency Roll-off	(f = >3kHz, <20kHz)		18.0	–	–	dB/oct.
Narrowband: Lowpass Frequency (-3dB)			–	2.9	–	kHz
Passband Ripple	(< 2300Hz)		-1.5	–	1.0	dB
	(2300Hz - 2550Hz)		-3.0	–	1.0	dB
Stopband Attenuation	(f = 4.25kHz)		12.2	17.0	–	dB
High Frequency Roll-off	(f = >2.3kHz, <5.1kHz)		18.0	–	–	dB/oct.
Pre-emphasis: Passband Frequencies			300		3000	Hz
Gain at 1kHz			–	0	–	dB
Slope Characteristic			–	6.0	–	dB/oct.
De-emphasis: Passband Frequencies			300		3000	Hz
Gain at 1kHz			–	0	–	dB
Slope Characteristic			–	6.0	–	dB/oct.
Squelch Bandpass Filter						
Centre Frequency Gain	(Wide and Narrow)		–	35.0	–	dB
Selectable Gain	(8 x 1.0dB steps)	9	-3.0	–	4.0	dB
Narrow Band:						
Centre Frequency	(fc)		–	18.75	–	kHz
Bandwidth	(fc ±)		–	6.5	–	kHz
Wideband:						
Centre Frequency	(fc)		–	25.5	–	kHz
Bandwidth	(fc ±)		–	8.5	–	kHz

Notes

1. A percentage of the applied V_{DD} (70% or 30%).
2. These inputs are compared internally with the Digital-to-Analogue converter.
3. With a minimum signal input level of 50mVrms at the Tx I/P or 65mVrms at the Rx I/P and an output level of 466mVrms.
4. Levels at the input of the Limiter element, centred about V_{BIAS} (Note 2).
5. This parameter remains within specification when pre-emphasis is employed.
6. With both Input HPF and LPF in circuit, but without pre-emphasis.
7. With Limiter LPF, but without de-emphasis characteristics.
8. This parameter remains within specification when de-emphasis is employed.
9. The gain variation around the centre frequency (fc).
10. See Application Information pages (Suggested Evaluation Tests) for information on gain element settings.
11. Mode: Tx with Compressor "OFF;" or in Rx, signal below limiter thresholds; Output level 466mVrms. Measured in a 30kHz bandwidth.
12. In the Tx mode with the Input Gain Amp set to ≤ 4.0dB.

Package Outlines

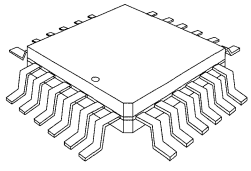
The FX506 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX506 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX506LG 24-pin quad plastic encapsulated bent and cropped (L1)

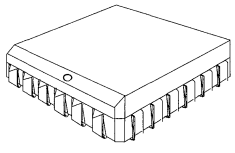
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX506LS 24-lead plastic leaded chip carrier (L2)

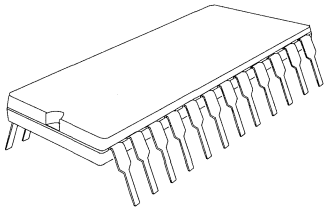
NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

FX506P 24-pin plastic DIL (P4)

NOT TO SCALE



Max. Body Length 31.85mm
Max. Body Width 13.82mm

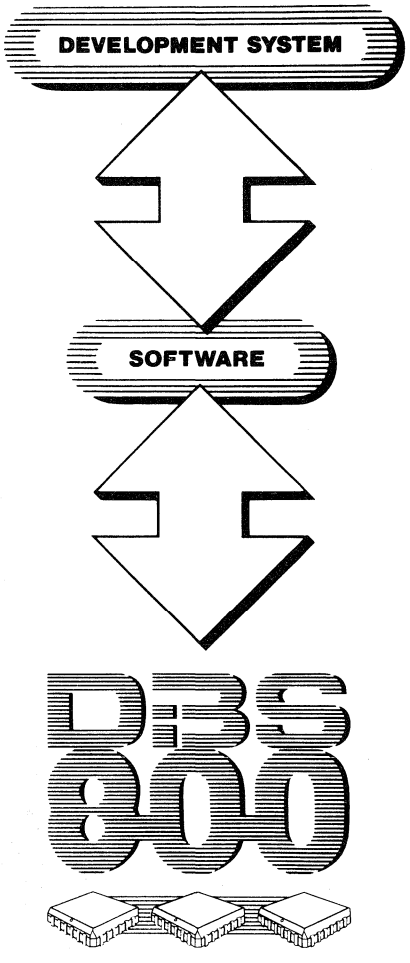
Ordering Information

FX506LG	24-pin encapsulated bent and cropped	(L1)
FX506LS	24-lead plastic leaded chip carrier	(L2)
FX506P	24-pin plastic DIL	(P4)

System Overview

Publication D/800/Intro/3 December 1991

Concept



DBS 800 Concept

The World's first **D**igitally-**I**ntegrated **B**aseband **S**ystem consisting of audio processing and signalling devices for use within a two-way mobile or trunked radio. Whilst supporting all internationally mandated or system specific requirements for processing and signalling, DBS 800 incorporates many powerful higher-level functions which offer a flexible and low-cost route to the "Added Value" opportunities in the PMR market.

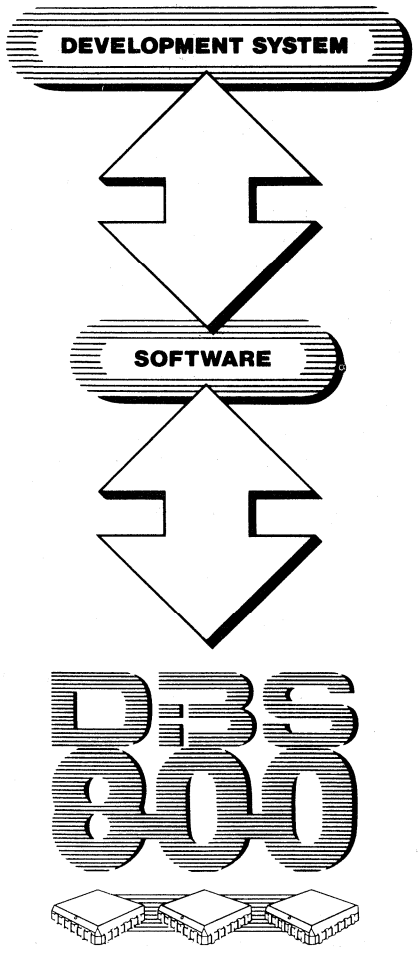
In support of the products functions, a development kit including all DBS 800 integrated circuits, together with a support microprocessor and software, allows evaluation, demonstration and software development to be completed in a fraction of the time normally taken.

DBS 800 has been conceived with the mobile radio hardware and software development engineer in mind. All ICs have been designed as peripherals to the radio's host microprocessor and require the minimum amount of software to control them. A single Address and Data hardware bus ("C-BUS") is used on all ICs, ensuring ease of connection to the host microprocessor and minimum track layout.

The advanced features offered by DBS 800 will have implications in reducing design, test, manufacture and service time whilst offering new and advanced facilities to the user and service provider.

In summary, DBS 800 provides a single, low-cost, fast turn-around design approach for simple or the most sophisticated multi-mode mobile or trunked radios intended for world-wide markets.

Features



DBS 800 Features

- Complete audio processing (CEPT, EIA, etc.)
- Universal Signalling
  Selcall (CCIR, ZVEI I, II, III, EEA etc.)
  CTCSS (EIA, EEA)
  DPL™, Digital Coded Squelch (DCS)
  Digital Selcall 1200 BAUD FFSK (MPT1317/1327)
  DTMF encode
  LTR™, NRZ Data
  2-Tone, Special Tones
- Data communications with data storage and buffering
- Voice/Data Scrambling
- Voice Management
  Voice storage, Mailbox, delay, busy buffer, alarms and status – Reduced airtime usage – Increased spectrum efficiency – VOX/Handsfree operation
- System Management
  Over-air programming/re-configuration and cloning – Call billing/monitoring/blocking – Tx time-out/selective lockout – Repeater access/control – Direct control of all system radio units
- ANI (automatic number ident)
- Half-duplex repeater
- Common Control and Data Bus ("C-BUS")
- Hardware Development Kit
- Software Support
  Evaluation – Demonstration – Development
- Electronic digital trimming and volume control
- Adaptive compensation for non-linear and temperature effects
- Two-Point Modulation for trunked/scanning schemes
- Fully automated test/alignment/servicing
- Self-Test mode
- Single hardware design approach
  software reconfigurable
- Fully integrated solution reduces PCB area
- Greatly reduced development time
- Multi-level powerdown modes
- -40°C to +85°C operating range
- +5-volt low-power CMOS
- Surface Mount packaging

Benefits

Design Electronic

- **DBS 800** offers a single design approach for all mandatory and system specific audio processing and signalling requirements. Inherent value-added features are provided for future upgrades, purely by modifying software.
- Single Address/Data/Audio I/O bus simplifies electronic interconnections between devices. Future 'option' upgrades can be added by simple connection to the "C-BUS" structure.
- Development Kit greatly reduces timescales, from initial mobile radio concept to pre-production stage, by utilizing the following software support.

  1. Evaluation software - allows the design engineer to check within a few hours the electrical performance of all DBS 800 devices, e.g. Dynamic range, SNR, current consumption etc.

  2. Demonstration software - offers a quick route to demonstrate the advanced features offered by DBS 800.

  3. Application software - offers numerous software routines which perform standard functions such as Selcall, Scrambling, Voice storage etc. These software packages may be used as part of the final operating software of the mobile radio.

  NOTE. This software is provided in a high-level language allowing ease of modification/addition and ultimate compilation for the chosen host microprocessor.
- Single design concept can be used for all models of mobile radio with differing features or market destinations: Software reconfigurable.
- One microprocessor is required to control all radio functions, DBS 800 devices contain additional hardware to minimize software overhead.
- Digitally controlled trimmers allow for 'adaptive adjustment' of non-linear "VCO conversion gain," and temperature effects. This allows use of cheaper, lower-tolerance components.
- "Non-predictive decoding of signalling" devices gives total design flexibility.
- Integrated solution offers higher relability.

Design Mechanical

- Fully integrated processing and signalling design approach, offered by DBS 800, minimizes PCB area.
- Adaptive trimming removes need for electro-mechanical trimmers, volume control etc. Trimmer tool access is no longer required through metal shielding.
- Fully electronic solution offers ease of design for harsh environments - waterproofing, intrinsic safety, vibration, etc.
- Smaller, lighter equipment design possible - handhelds.
- Surface mount packages allows fully automated assembly.
- "C-BUS" simplifies PCB layout and reduces tracking space.

System Operator

- By far the greatest advantage of DBS 800 to the system operator is the system management and control functions leading to more efficient airtime usage. The result being more users per channel and therefore higher revenue.
- Total system control and management; Selective lockout 'stun,' call-barring, call monitoring, billing, user specific Tx-timing etc.
- DBS 800 is compatible with all existing signalling schemes such as Selcall, CTCSS, DPL™, DCS, 2-Tone, DTMF, LTR™,/MPT1327 Trunking.
- Advanced signalling; Digital Selcall, ANI, overair re-configuration, cloning, channel dependent signalling.

Benefits .....

- Voice Compression and Pause Elimination may be used to reduce air-time usage.
- Non-predictive decoding offers features such as recognition and identification of own repeater CTCSS tone, multiple group call etc.
- Value-added voice management features voice security, voice mailbox, voice status, voice alarm, voice buffering when channel busy.
- Repeater use; adaptive signalling, software controlled selective Tx delay/timeout. Lower cost repeaters through use of non-predictive decoding. Additional sub-audible/ Selcall signalling schemes offers a greater coding capability.
- MPT1317/1327 trunking capability.

User

- Smaller, lower cost multi-feature mobile radios.
- Voice buffering allows user to speak into microphone at will regardless if channel is busy. The stored voice is transmitted automatically on channel clear down.
- Voice mailbox offers an answering machine facility to the mobile radio user.
- Handsfree/VOX facility, particularly in trunked radio applications having long call set-up times.
- Voice security, Call security for little or no hardware overhead, i.e. 'low cost Scrambling.'
- Data communications - ability to connect directly to mobile radio, with no external interface, laptop PC's, printers etc. RS232 interface or others possible. Data storage and security are purely software dependant.
- Integrated solution will result in greater equipment reliability and fewer service/repair intervals.

Manufacture

- Fully integrated surface mount packaged devices with few external passive components allows fully automated assembly.
- Low component count reduces manufacturing time/cost.
- Simplified inventory by using standard DBS 800 chip-set thus further reducing costs.
- Minimum labour content in manufacture and test.

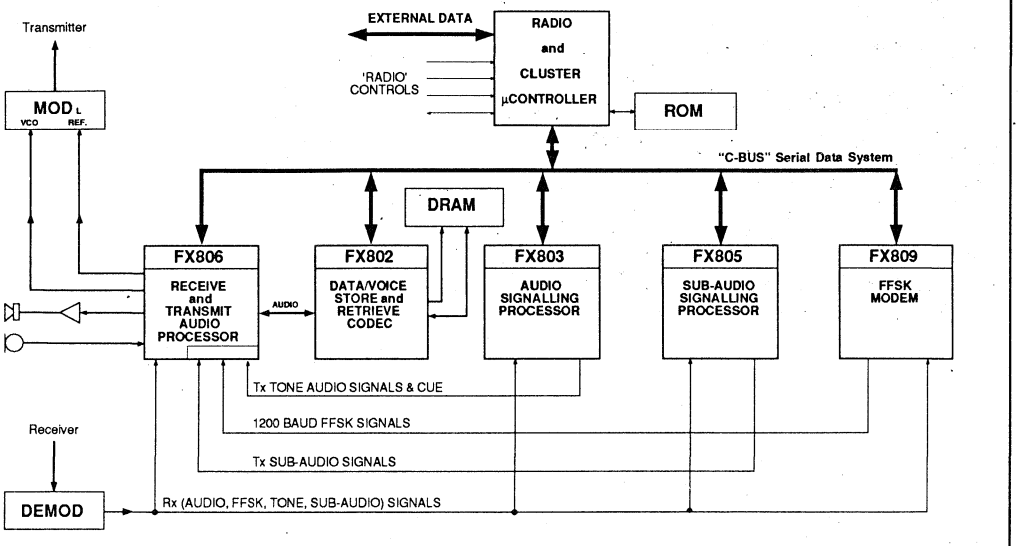
Test

- All radio parameters can be adjusted by ATE without the need for any manual adjustments, leading to; Tighter control, repeatability, higher quality/fully automated reporting.
- Radios can be calibrated and tested when completely assembled by using a single external audio/data/RF connection only.
- Simplified ATE design.
- Reduced test and alignment times - fully automated.

Servicing

- Fully computerized 'fast fault' diagnosis.
- Automated testing reduces service time.
- Radio test, re-calibration and reprogramming of radio functions can be carried out without need for removal of radio equipment.
- Self-test modes with audible/visual alert outputs.
- Lower service costs - "While-U-Wait" servicing or customer self-testing.
- Simple field-test unit can be used to test or reconfigure radios incorporating DBS 800.

System Introduction



DBS 800 Audio System

DBS 800

Digitally-integrated Baseband System

A family of digitally controlled low-power CMOS audio microcircuits with supporting evaluation/design hardware and software for use collectively or individually within the audio and auxilliary stages of Private Mobile Radio (PMR) communications systems.

As a system, the DBS 800 microcircuits will perform the "core" audio functions shown below, producing a true "multi-mode" radio.

DBS 800 Functions

- **FX802 DVSR Codec**
  Voice Digitization, Data and Voice Storage and Retrieval, using Continuously Variable Slope Delta Modulation. Data buffering and transfer is via an on-chip Dynamic RAM Controller, addressing up to 4Mbits of externally connected DRAM.

- **FX803 Audio Signalling Processor**
  In-Band Audio Signal processing. 2-/5-/6-/Multi-Tone Selective Call encoding/decoding. Dual-Tone Multi-Frequency (DTMF) encoding.

- **FX805 Sub-Audio Signalling Processor**
  Sub-Audio Tone (CTCSS) and Digitally Controlled Squelch (DCS) Signal processing.

- **FX806 Audio Processor**
  Audio, Speech and Data processing, using selective-gain, VOGAD and filter stages. Multiplexing of other DBS 800 audio outputs providing a common drive to transmitter modulation stages.

- **FX809 FFSK Modem**
  Intelligent 1200 baud data modulation/demodulation, compatible with MPT1317/1327 and other similar systems.

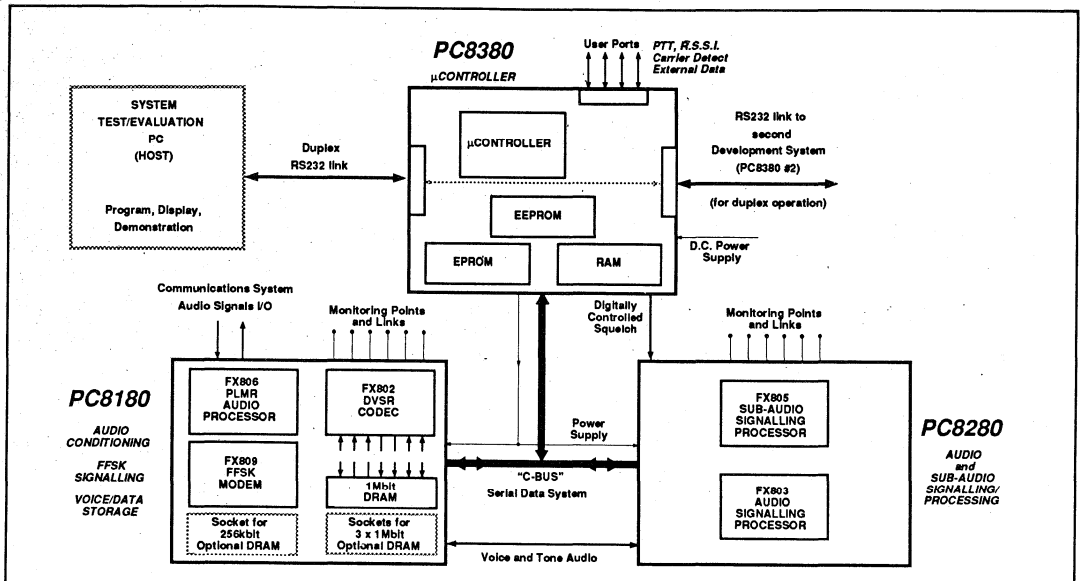
Management and operation of all system functions is under the control of a µProcessor. Communication and control is by means of a simple, two-way serial data system, the "C-BUS."

By this method, DBS 800 will fulfil the mandatory requirements of national communication specifications, such as CEPT, EIA, FTZ, MPT, as well as application-specific or system requirements.

To enable development and design with DBS 800, a Development System is provided, comprising printed circuit boards and operating software – thus ensuring that design time cycles are minimized.

All DBS 800 low-power 5-volt CMOS integrated circuits incorporate "Powersaving" modes to ensure maximum system efficiency.

System Development



DBS 800 "System Development" Hardware

DBS 800 Development System

A complete system designed to enable radio equipment designers to evaluate and design with DBS 800 integrated circuits.

The DBS 800 Development System is a combination of hardware and software. The hardware consists of 3 populated printed circuit boards described below:

- **PC8180**
  Audio Conditioning, Data/Voice Storage and Retrieval, FFSK Signalling. Provided on-board is the facility to install up to 4Mbit of optional DRAM.

- **PC8280**
  Audio and Sub-Audio Signal Processing.

- **PC8380**
  The development µController with supporting software and interface circuitry. Intended to run with an evaluation processor, this µController PCB can also be used stand-alone. The PC8380 will run integral PROM-based or modified/new example programmes. Additional user ports are provided to facilitate radio, communication functions and prompts; PTT, R.S.S.I., Carrier Detect, etc.

Monitor and test points are provided on all PCBs to enable ease of access to relevant data and audio signals. Each PCB has its own on-board Xtal/clock circuitry.

Development software is provided in EPROM and as example listings on floppy disk, and takes the form of:

- **Microcircuit Evaluation** Software
  Measurement and functional tests of DBS 800 devices. Enabling the designer to set-up, step-through and run evaluation tests.

- **System Demonstration** Software
  External control of development application programmes, running PMR based routines, such as; Audio Processing, Signalling, Voice Messaging, Data Storage and Transmission.

- **Design Application** Software
  Functional software and listings are provided to operate PMR orientated routines. From these the Mobile Radio designer is able to create application sub-routines for use in specific radio system projects.

The DBS 800 Development System, which contributes to faster evaluation and design cycles by providing total flexibilty in the investigation of PMR applications, ensures that the Mobile Radio designer can:

(1) Quickly evaluate the electrical performance of each individual microcircuit, and
(2) Demonstrate some of the new features offered by DBS 800, and
(3) Investigate usable Application Specific software routines in a high-level language, suitable for modification and translation to the ultimate choice of µController.

System Applications

Application	802	803	805	806	809	Example
● **Direct Voice** All mandatory audio filtering, gain adjustment, VOGAD and limiter blocks required for audio signal processing within a PMR Radio.				■		Basic two-way radio, operating open channel with carrier squelch only.
● **Voice Mailbox** (Open Channel) Receipt and storage of voice calls for instant replay.	■			■		Taxi companies or Police to replay the last received message e.g. customer or incident address.
● **Voice Mailbox** (Personal Call) Storage of selectively called voice message during unattended vehicle operation.	■			■		Service engineer may receive information regarding the next call whilst away from the vehicle.
● **Voice Status Announcement** Transponding a pre-recorded voice 'status' message when selectively addressed.	■			■		Security companies can leave a recorded message in the vehicle as to their present location.
● **Voice Alarm** Automatically transmit a pre-recorded voice message when externally triggered.	■			■		Security vehicle under attack may send a distress message and a 'voice status' noting last known location.
● **Voice Buffer** Storing speech temporarily until a transmission channel is free. Used to buffer speech during 'busy channel' periods or 'link establishment' delays encountered on Trunked and Common Base Station systems.	■			■		Allows the operator to talk immediately, regardless if the transmission channel is free. The initial voice, once stored, is sent when the link is established. Squelch Tail elimination can be performed by delaying speech and muting the unwanted section.
● **VOX** Voice Buffering allows speech to be delayed, allowing the VOX to operate with an effective ZERO attack time.	■			■		Trunked systems with long 'link establishment' times can be operated "hands free" using 'buffered' VOX.
● **Speech Delay** A fixed delay introduced into speech. (similar to 'voice buffering')	■			■		'Skip' play-back features or delay equalization of speech in 'Quasi-Sync' systems.
● **Answering Machine Facility** A combination of Voice Status and Voice Mailbox applications to give a complete Answering Machine facility.	■			■		Offers Trunked radio users similar voice messaging facilities to those available to Cellular radio users.
● **Voice Security** (Time Domain) Digitising and scrambling voice information according to a cryptographic key code and then re-combining the scrambled digits into an analogue signal for onward transmission. Synchronization is achieved using the 1200 baud FFSK Modem.	■			■	■	Police, Military and other commercial applications requiring radio communications with no fear of eavesdropping.

System Applications .....

Application	802	803	805	806	809	Example
● Voice Compression Time compressing segments of speech for injection of signalling information into the inter-segment gaps.	■			■	■	Continuous ANI or synchronization systems for scramblers. Simultaneous transmission of data and speech over a standard 3000Hz bandwidth.
● Pause Elimination Using VOX feature - store only "voiced" sounds for transmission. This method eliminates pauses and gaps in speech.	■			■	■	Efficient use of both the storage medium and the air time by sending the voice with short, standard length gap where required.
● Two-Way Mobile Relay By storing speech, a half-duplex radio may be converted into a repeater station. Storing incoming voice for re-transmission when the message ends.	■			■	■	Temporary repeater function. "Over the hill" communication from a base station to a handheld radio via a mobile radio.
● Mobile Data Transmission Transmission and Reception of data using a 1200 baud, or other speed modem. Faster data from or to an external peripheral may use the DVSR and memory to buffer data prior to transfer using the 1200 baud Modem product.	■			■	■	Connection of a 'laptop' PC dumping data at 19kbits/s to the radio's 1200 baud modem. Formatting, packeting and error correction/detection achieved by the µC whilst data is buffered in RAM using the DVSR product.
● Sub-Audio Signalling Transmission and non-predictive detection of analogue or digital Sub-Audio signalling for Mobile and Trunked Radio.			■	■		CTCSS – Non-Predictive Decode and Encode DCS – Digitally Coded Squelch DPL™ – Motorola Digital Private Line LTR™ – Logic Trunked Radio Multi-standard squelch and repeater access schemes.
● In-Band Tone Signalling Transmission and non-predictive detection of Selective Call or Single tone systems. Generation of DTMF or "Special" tones.		■		■		Selcall – (CCIR, ZVEI {I, II and III} and EEA) 2-/5-/6-/Multi-Tone signalling Dual Tone Multi-Frequency (DTMF) transmission Group/All Call/Data/Status/ANI Over-Air unit assignment/ reconfiguration Special Tone generation/Reception Radio Telemetry/Alarms
● 1200 Baud Signalling Transmission and reception of data in the form of audio tones (1200Hz, 1800Hz) at 1200 baud. Checksum and Synchronization word provision and detection.				■	■	1200 Baud FFSK MPT1317/1327 Trunked Radio signalling (Band III UK) Data-Over-Air. Mobitex, MCA, ANI, Scrambler Synchronization etc.

● **Microcircuits**

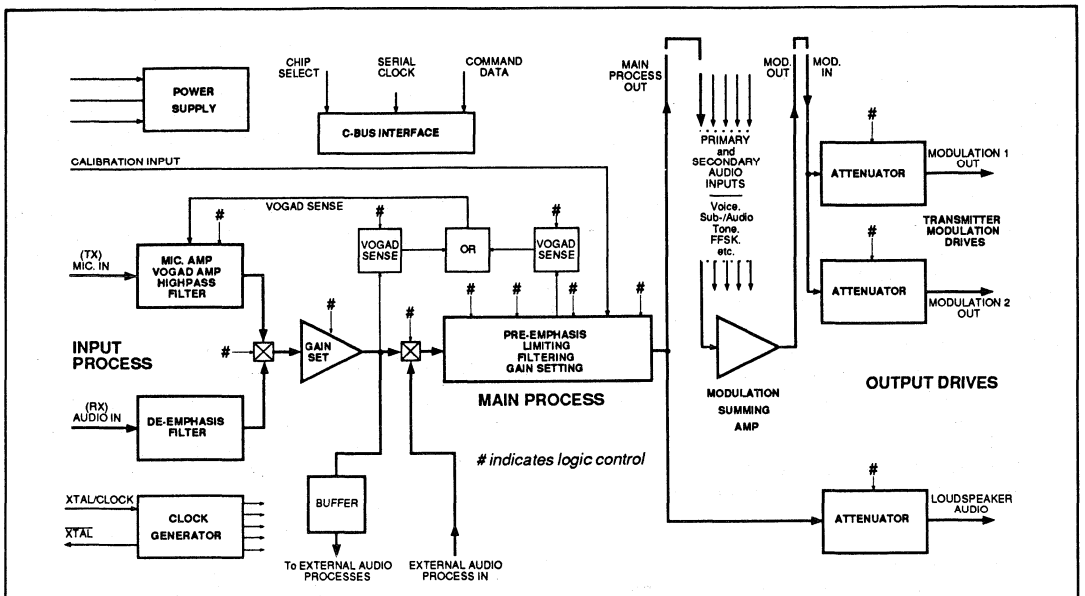
FX802	**DVSR Codec**
FX803	**Audio Signalling Processor**
FX805	**Sub-Audio Signalling Processor**
FX806	**Audio Processor**
FX809	**FFSK Modem**

● **Key:**

■ Recommended microcircuits required to achieve the illustrated application.

□ Alternative signalling options.

FX806A
Audio Processor



FX806 – Audio Processor

FX806A Audio Processor

All DBS 800 system signal conditioning and filtering requirements for both transmit and receive paths are carried out by this half-duplex audio processor.

In transmit the FX806 conditions input voice-band audio and combines this with in-band/sub-audio signalling and data for transmitter modulation. The FX806 in receive processes audio from the radio discriminator for presentation to the loudspeaker drive circuitry.

The signal path of the FX806 can be divided into three sections:

- **Input Process**

This stage has a selectable transmit and receive path. Transmit signals pass through microphone pre-amplifier, VOGAD and highpass filter stages. The receive audio passes through a de-emphasis stage.
This initial audio, after gain adjustment, may be switched to external audio processes (such as scrambling) or the Main Process block.

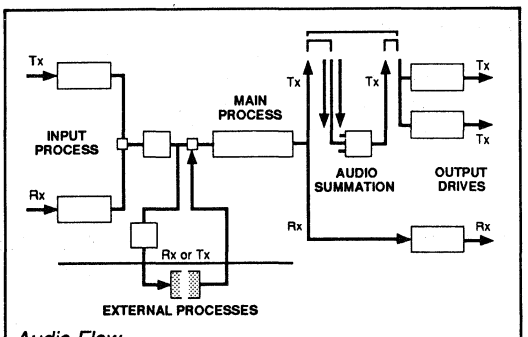
- **Main Process**

Conditioning for the input or external process signals. Comprising pre-emphasis, high and lowpass switched-capacitor filtering and a deviation limiter. Conditioned audio is now presented to the output stages.

- **Summation and Output Drives**

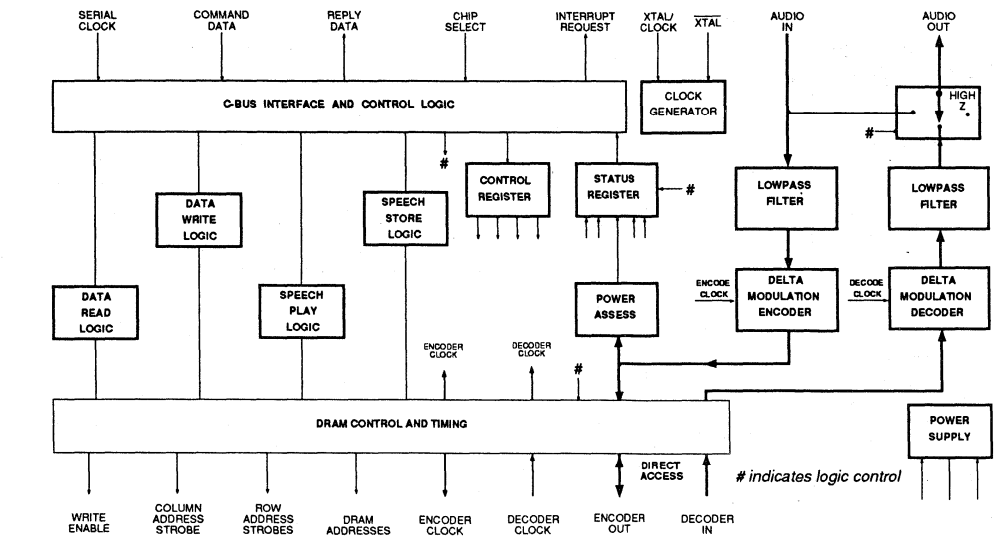
Main audio for transmission is combined with signalling and data from external sources to provide the transmitter modulation drives. Received audio is level adjusted for output to loudspeaker circuitry.

FX806 circuit elements and signal paths are controlled and digitally adjusted by the µController using the "C-BUS" protocol.
Signal levels can therefore be dynamically controlled offering 'dynamic-compensation' for factors such as, temperature drift, VCO non-linearity etc.



Audio Flow

FX802
DVSR Codec



FX802 – DVSR Codec

FX802 Data/Voice Storage Codec (DVSR)

A Continuosly Variable Slope Delta Modulation encoder and decoder with the abilty to store, retrieve and control data within external Dynamic Random Access Memory (DRAM). This microcircuit includes, on-chip, all address and refresh circuitry for control of up to 4Mbits of external DRAM.

The FX802 has four primary functions:

- **Speech Digitization**
  Digitally encoding an analogue (voice) input signal and presenting the resulting bit stream for output as a digital signal.
- **Speech (Data) Decoding**
  Producing an analogue (voice) signal from an input digital bit stream.
- **Data Storage**
  Storing in DRAM, either encoded speech data or data loaded from "C-BUS."
- **Data Recovery**
  Recovery of data from DRAM for output to either the Delta Decoder or the µController via "C-BUS."

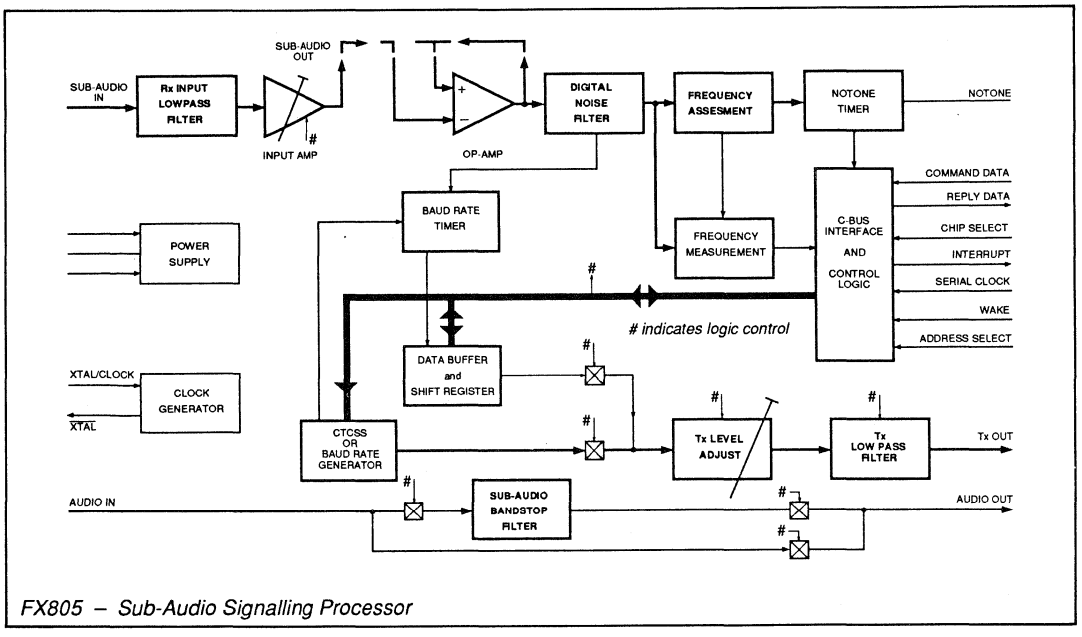
Encoded speech is available for transmission or storage in the connected DRAM. Input (speech-band) data from either the received signal or DRAM, is decoded, shaped and available for output to loudspeaker circuitry via the Audio Processor.

On-chip, the Delta Codec is supported by; input and output analogue switched-capacitor filters, switching control circuitry, input analogue power assessment circuitry (for pause-management or VOX systems) and DRAM control (refresh and timing logic).

The storage, recovery and replay functions of this device are ideal for "Time Domain Scrambling," "Temporary Voice (Busy) Buffering," "Answering Machine" and "Temporary Data Storage (fast in – slow out to the FX809 FFSK Modem)" applications. A Force Idle instruction provides a 10101010.....1010 perfect idle pattern to the decoder input.

"C-BUS" commands can be 'buffered' (stored temporarily) to allow instruction continuity.

FX805 Sub-Audio Signalling Processor



FX805 – Sub-Audio Signalling Processor

FX805 Sub-Audio Signalling Processor

A sub-audio frequency signalling processor to provide an outband audio and digital signalling facility for PMR radio systems.

This half-duplex device, which caters for the transmission and non-predictive reception of:

- Continuous Tone Controlled Squelch (CTCSS) tones and other non-standard frequencies.
- Digitally Coded Squelch – DCS/DPL™.

comprises:

- A non-predictive CTCSS Tone Decoder and DCS demodulator.
- A CTCSS/DCS Tone Encoder with Tx level adjustment and lowpass filter output stage.
- A selectable sub-audio bandstop filter.

The CTCSS tone data for transmission is loaded to this device, via "C-BUS," encoded and output from the Tx Lowpass filter.

Received non-predicted CTCSS input tone frequencies are measured and the resulting data presented to the µController for matching against a 'look-up' table.

Noise filtering is provided to improve the signal quality prior to measurement.

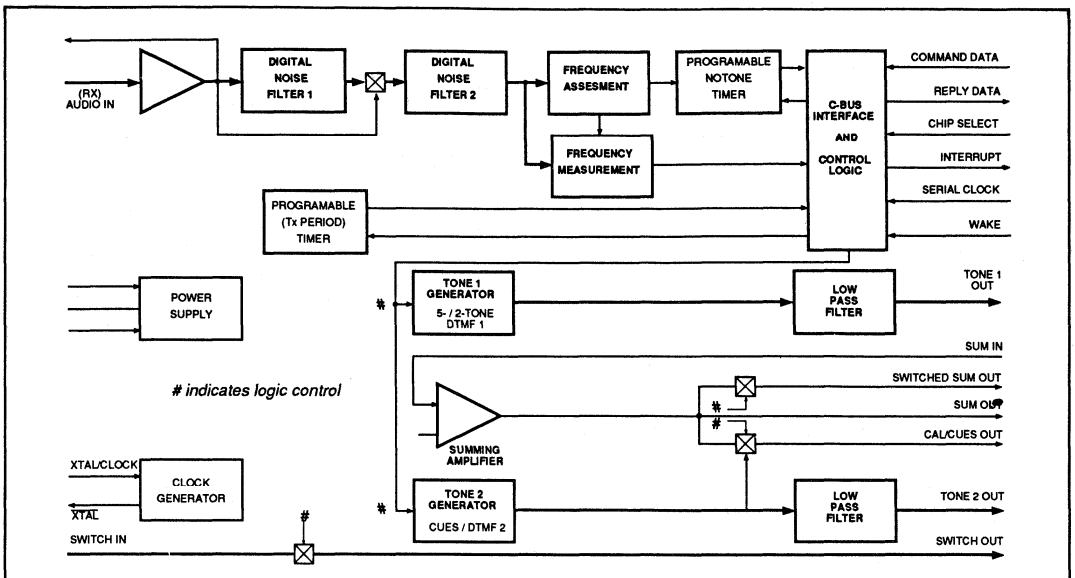
DCS coded data for transmission is loaded to the shift register and output, in bytes, through the tone output circuitry as sub-audio frequencies. DCS coding is produced by the µController.

Received DCS frequencies are filtered, detected and transfered in bytes from the shift register to the µController for decoding by software. Clock extraction circuitry is provided on chip.

Provision is made in both hardware and system software allocations to address two FX805 Sub-Audio Signalling Processors consecutively to achieve full-duplex operation.

Powersaving may be controlled by software or a dedicated input.

FX803 Audio Signalling Processor



FX803 – Audio Signalling Processor

FX803 Audio Signalling Processor

An audio signalling processor to provide an inband tone signalling facility for PMR radio systems. Signalling systems supported include selcall (CCIR, ZVEI I, II and III, EEA), 2-tone selcall and DTMF encode.

Using a non-predictive decoder and versatile encoder gives the FX803 the capability to work in any standard or non-standard tone system.

This full-duplex device consisting of;

- A tone decoder with programmable NOTONE timer.
- Two individual tone encoders and a programmable (Tx) period timer.
- An on-chip summing amplifier

For use with Single Tone or Selective Call systems.

Under the control of the µController, via "C-BUS," the FX803 will encode and transmit 1 or 2 audio tones simultaneously, and detect, decode and indicate the frequency of the non-predicted input tones. The transmit frequency range available is 208Hz to 3kHz and the receive frequency range is 313Hz to 6kHz.

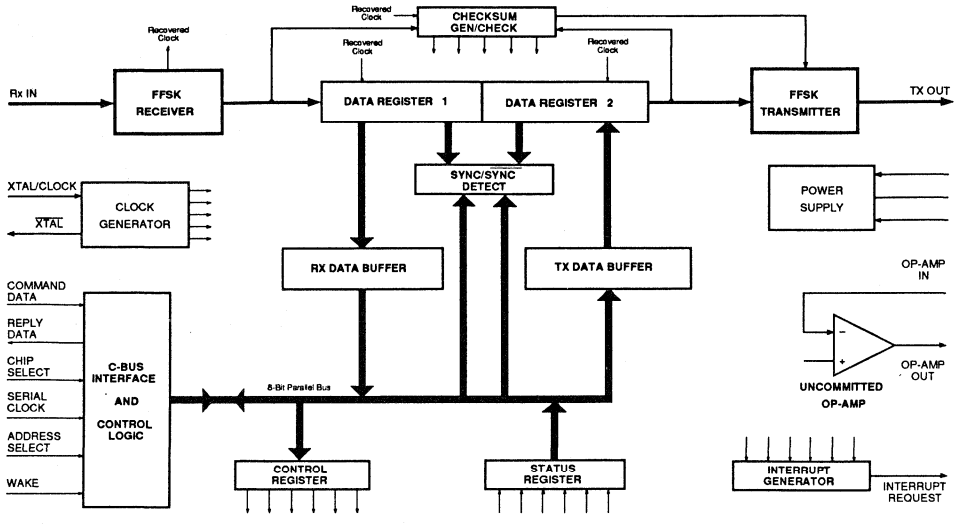
The output frequencies are produced from data loaded to the device, with the tone transmit period indicated by the programmable on-chip timer.

A Dual Tone Multi-Frequency (DTMF) output is obtained by combining the 2 independent output frequencies in the integral summing amplifier. This is also available for level correction.

Tones produced by the FX803 can be used in the system as modulation calibration inputs and as "CUE" audio indications to the operator.

Received tones are measured and their frequency indicated to the µController in the form of a received data word. A poor quality or incoherent tone will indicate NOTONE.

FX809
FFSK Modem



FX809 – 1200 Baud FFSK Modem

FX809 FFSK Modem

An intelligent, half-duplex, 1200 baud FFSK/MSK modem which under "C-BUS" control can transmit and receive data directly input. In addition this modem provides automatic checksum generation and error checking, in accordance with MPT1327, with the facility to load a customer-specific synchronization word.

Fully "C-BUS" compatible, this device, using Interrupt and Status Register procedures, will load and transmit preamble, synchronization and 8-bit data words (bytes) producing a 16-bit checksum if instructed.

In the Receive mode synchronization (SYNC) word detection is carried out, and received data bytes made available to the "C-BUS interface. Received input tones are demodulated in the FFSK Receiver and placed as 8-bit words into the Rx Data Buffer for transfer to the serial Reply Data line.

Information (data) for transmission is written to the Tx Data Buffer from the Command Data line, to be modulated as 1200Hz (logic "1") and 1800Hz (logic "0") tones.

Checksum generation (Tx) and checking (Rx) is enabled by software control.

Provision is made in the FX809 and "C-BUS" protocol to address 2 x FX809 Modems consecutively to produce "full-duplex" data operation.

The FX809 has a non-committed Op-Amp on-chip for general applications in the DBS 800 "cluster."

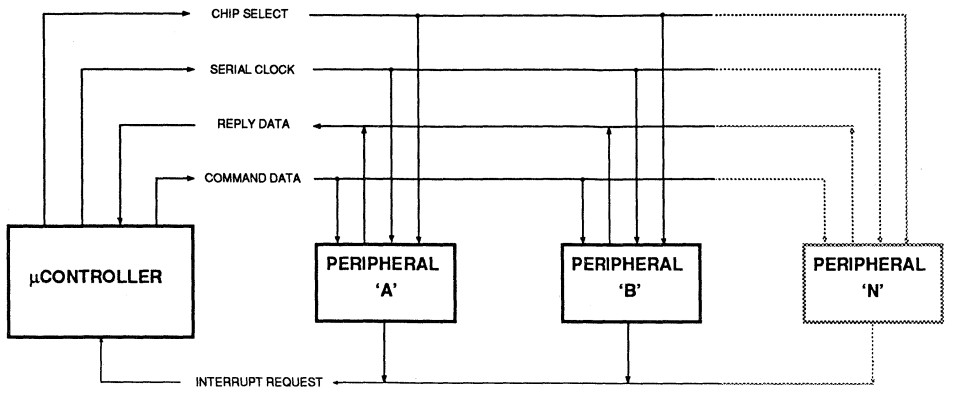
This modem is designed to interrupt (the µController) for the following events:

Received Data Ready
Transmit Data (Buffer) Ready
SYNC Detected
$\overline{\text{SYNC}}$ Detected
Transmitter Idle

Input timing is carried out by a 1200 baud clock recovered from the input bit stream and the output tones timed to the transmit clock. On-Chip filter, register clocks and tone frequencies are derived from an external Xtal or clock input.

Interrupt, SYNC Detection and Checksum functions can be enabled or disabled by software commands.

"C-BUS" Serial Interfacing



The "C-BUS" Hardware Concept

"C-BUS"

The software and hardware interface for all members of the DBS 800 family. "C-BUS" enables the serial, bi-directional transfer of commands and data throughout the system, allowing total flexibility of operational control and data handling. System upgrades can be achieved by a simple software or firmware change.

Hardware Interface

Physically, the Bus consists of 5 lines as described below:

- **"Serial Clock"** – Driven by the µController to all peripherals. All "C-BUS" commands and data transfers are synchronized to this clock.
- **"Command Data"** – to Address/Command and transfer data from µController to an addressed peripheral, in serial format.
- **"Reply Data"** – transfer of "requested (commanded)" data from an addressed peripheral, in serial format.
- **"Chip Select" (CS)** – carrying the CS timing command to the peripheral, from the µController. DBS 800 audio microcircuits are designed to work with a common CS line, using the Address/Command as a chip identifier. Transfer sequences are initiated, completed or aborted by the CS signal.
- **Interrupt Requests (IRQ)** – interactive peripheral devices have an output for connection to the µController Interrupt input.

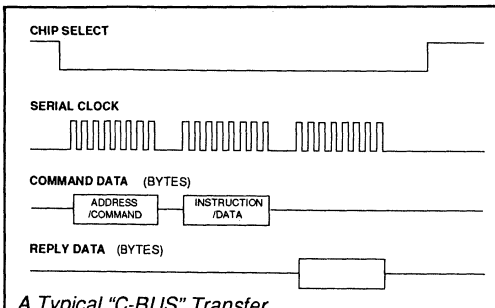
All future DBS 800 integrated circuits will be "C-BUS" compatible.

Software and Protocol

"C-BUS" protocol consists of 3 categories of transaction:

- **"Address/Command"**
  i.e. Modem X – Enable Tx.
- **"Address/Command, and data byte/s"**
  i.e. DVSR – Write to Tx Data Buffer – 'n' data byte/s.
- **"Address/Command (Request) and reply data bytes"**
  i.e. Modem X – Read Rx Data Buffer – 'n' data byte/s.

A complete description of all "C-BUS" Address/Commands is provided in Document 2 of the DBS 800 Documentation, System Support Information.



A Typical "C-BUS" Transfer

Controlling System

"C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's PLMR microcircuits — The FX802, FX803, FX805, FX806 and FX809.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

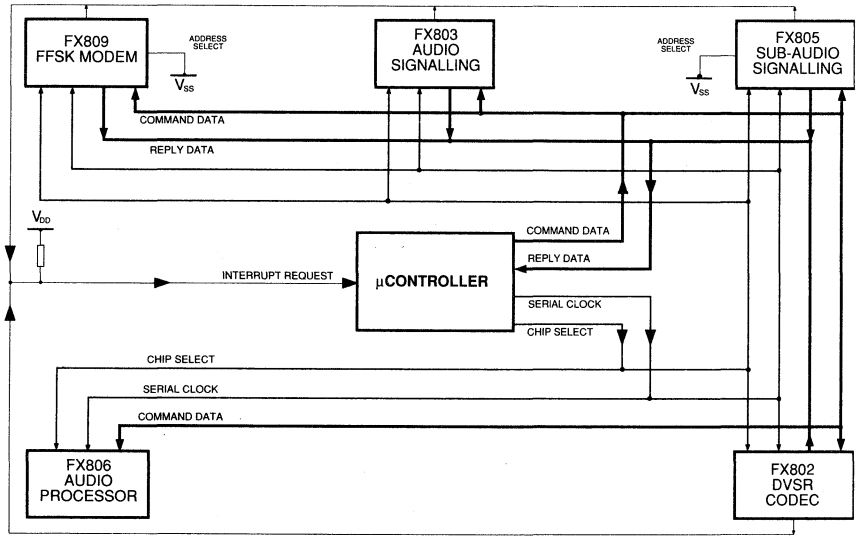


Fig.1 Example "C-BUS" Hardware Interconnections

"C-BUS" Hardware Interface

Physically, the "BUS" consists of the 5 lines shown in Figure 1 and described below:

- **"Serial Clock" line** – driven by the µController and connected to all DBS 800 microcircuits.
- **"Command Data" line** – driven by the µController and connected to all DBS 800 microcircuits.
- **"Reply Data" line** – connected to the µController and driven by the 3-state outputs of relevant DBS 800 microcircuits.
- **"$\overline{\text{Chip Select}}$" ($\overline{\text{CS}}$) line** – driven by the µController and connected to all DBS 800 microcircuits.
- **"$\overline{\text{Interrupt Request}}$" ($\overline{\text{IRQ}}$) line** – interactive DBS 800 microcircuits have a 'wire-or'-able Interrupt Request output ($\overline{\text{IRQ}}$) for connection to the µController's Interrupt input.

Configurations for Full-Duplex Signalling

Figure 2 shows how two FX809 FFSK Modems may be connected to the "C-BUS" to provide full-duplex FFSK signalling. Two FX805 Sub-Audio Signalling Processors may be connected in a similar manner when full-duplex sub-audio and NRZ signalling is required.

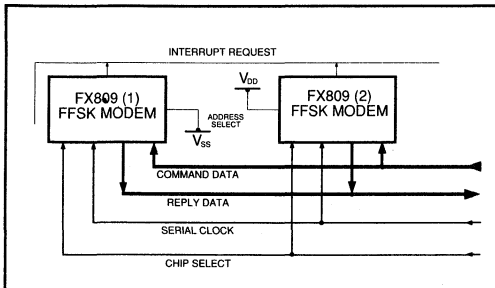


Fig.2 FX809 Modems for Full-Duplex Operation

Publication D/800/Sys/3 July 1994

Controlling Protocol

The Use of "C-BUS" Software and Protocol

Each individual DBS 800 Data Sheet contains a table listing the "C-BUS" commands and instructions relevant to that peripheral. Table 1 gives an abridged list of all DBS 800 Address allocations. All "C-BUS" data transfer is based on the serial transmission of 8-bit bytes, sent to the BUS MSB (bit 7) first, LSB (bit 0) last, and synchronized to a burst of 8 Serial Clock pulses generated by the µController.

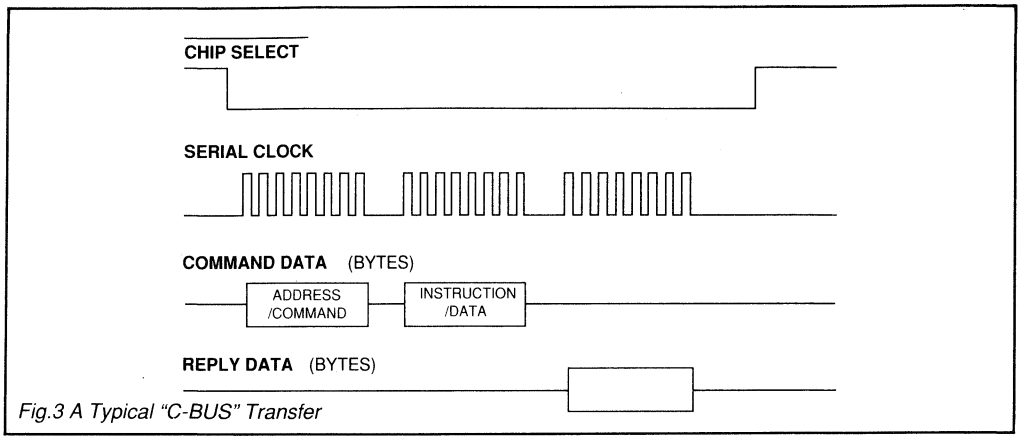


Fig.3 A Typical "C-BUS" Transfer

Address/Command (A/C) Byte

Under the "C-BUS" protocol, this byte is the first to be transmitted on the Command Data line after the Chip Select line becomes active (logic "0"), and is an 'Address' specifying which chip is selected for a particular "C-BUS" transaction.

A particular chip may recognise more than one address. Each address recognised by a chip signifies a particular command.

Three types of "C-BUS" transaction are possible:

A Transmission of a single Address/Command byte.

B Transmission of an Address/Command byte followed by one or more Command Data bytes.

C Transmissions of an Address/Command byte (plus possibly one or more data bytes) resulting in one or more Reply bytes being sent back from the selected DBS 800 microcircuit to the µController.

With the Chip Select line being used to define the beginning and end of each transaction. The Timing Diagrams (Figures 4 and 5) show the transfer procedure.

When transaction types 'B' or 'C' involve the transmission of more than one data byte, then the Most Significant data Byte is transmitted first, the Least Significant data Byte last.

System Addressing

Table 1 (a) shows the present allocation of Address/Command byte values to "C-BUS" compatible chips, some Address/Command byte values have been reserved for specific general commands such as General Reset and "C-BUS" performance testing. These particular values may be recognised by more than one chip.

In general, however, the exact effect of an Address/Command byte value will depend on the detailed specification for the particular DBS 800 microcircuit, and are explained in detail in the relevant current DBS 800 Data Sheet.

Command Data Bytes to DBS 800 Microcircuits

Under the "C-BUS" protocol, the Address/Command byte sent from the µController may be followed by one or more data bytes to be loaded into register(s) on the selected DBS 800 microcircuit (transactions type 'B' and "C").

The exact number, destination and effect of these data bytes is determined by the Address/Command byte value and the specification of the particular peripheral microcircuit.

The µController must always transmit the correct number of data bytes - as each byte is received by the peripheral it may have an immediate effect, or may not take effect until the Chip Select line goes high (inactive), (see Timing Figures 4 and 5) at the end of the transaction, depending on the specification for that particular peripheral microcircuit.

Reply Data Bytes from DBS 800 Microcircuits

Are transmitted from the selected DBS 800 peripheral to the µController and are clocked into the µController when the Serial Clock is 'high.'

Under the "C-BUS" protocol, the format of the Address/Command byte may request that the selected chip responds by sending one or more Reply Data bytes to the µController (transaction type 'C').

The exact number, source, and meaning of these byte(s) is determined by the Address/Command byte value and the specifications of the particular peripheral microcircuit.

The transmission of each byte from the peripheral microcircuit is governed by the Serial Clock pulse generated by the µController. In some cases, the µController may not wish to read-in all of the bytes which the peripheral would normally expect to transmit. In these cases, the µController will raise the Chip Select line to a high (inactive) level as soon as it has read in sufficient bytes, and on detecting the Chip Select line going high the peripheral microcircuit will abort its transmission sequence.

Controlling Protocol...

The Use of "C-BUS" Software and Protocol .....

Serial Clock Pulses

Are generated by the µController to synchronize the transfer of data bits between the µController and DBS 800 microcircuits as illustrated in Figures 3, 4 and 5. For each 8-bit byte, Command or Reply, the µController must generate 8 Serial Clock pulses taking into account the inter-byte period (t_{NXT}).

To allow for differing µController capabilities, "C-BUS" compatible ICs are able to work with either 'polarity' of Serial Clock, ie. the Serial Clock line may be at a 'high' or a 'low' level at the start of each transaction, as long as:

(i) Data sent from the µController is clocked into the DBS 800 ICs on the rising edge of the Serial Clock pulses.

(ii) Reply Data sent from a DBS 800 IC to the µController is clocked into the µController when the Serial Clock is 'high.'

"C-BUS" Serial Clock Rate

Generally "C-BUS" Serial Clock rates that are harmonically related to the 'XTAL/CLOCK ÷ 32'–FREQUENCY cannot produce alias effects within a microcircuit, therefore employment of a "C-BUS" Serial Clock rate at this frequency is preferable.

If it proves impractical to select a synchronous "C-BUS" clock, coupling between sensitive analogue inputs (such as the FX806 Mic. inputs) and the "C-BUS" should be avoided.

Chip Select ($\overline{CS}$)

Data transfer sequences are initiated, completed or aborted by the CS signal. This input, provided by the µController to all DBS 800 microcircuits, is active at a logic "0" and inactive at a logic "1." See Figure 4.

"C-BUS" Specifications

Operating Limits

All "C-BUS" characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5 Volts d.c. T_{AMB} = 25°C. Reply Data Line loaded with 50pF//200kΩ to V_{SS}.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Input Logic Levels					
Logic "1"	1	3.5	–	–	V
Logic "0"	1	–	–	1.5	V
I_{IN} (logic "1" or "0")	1	–	–	1.0	µA
Output Logic Levels					
Logic "1" (-120µA)	2	4.6	–	–	V
Logic "0" (360µA)	3	–	–	0.4	V
I_{Out} Tristate (logic "1" or "0")	3	–	–	4.0	µA
Input Capacitance	1	–	–	7.5	pF
IOX (V_{Out} = 5V)	4	–	–	4.0	µA

Notes

1. Serial Clock, Command Data and Chip Select inputs.
2. Reply Data output.
3. Reply Data and IRQ outputs.
4. Leakage current into the "Off" IRQ output.

"C-BUS" Addressing

To assist in the efficient use of "C-BUS" and System addressing, Table 1 shows the distribution of the DBS 800 Address allocations.

(a) "C-BUS" Address Listing – "C-BUS" Addresses (HEX) currently allocated to DBS 800 microcircuits

"C-BUS" Performance Testing			00
General (all device) Reset			01
Audio Processor			**FX806**
Control Command			10
Mode Command			11
Modulator Levels Set			12
Volume Set			13
Audio Signalling Processor			**FX803**
Write to Control Register			30
Read Status Register			31
Read Rx Tone Frequency			32
Write to NOTONE Timer			33
Write to Tx Tone Generator 1			34
Write to Tx Tone Generator 2			35
Write to G/Purpose Timer			36
FFSK Modem 1			**FX809**
Write to Control Register			40
Read Status Register			41
Read Rx Data Buffer			42
Write to Tx Data Buffer			43
Write to Sync Program			44
FFSK Modem 2			**FX809**
Write to Control Register			48
Read Status Register			49
Read Rx Data Buffer			4A
Write to Tx Data Buffer			4B
Write to Sync Program			4C
"C-BUS" Performance Testing			55

DVSR Codec			**FX802**
Write to Control Register			60
Read Status Register			61
Store 'N' pages,	Start page 'X'	(immediate)	62
Store 'N' pages,	Start page 'X'	(buffered)	63
Play 'N' pages,	Start page 'X'	(immediate)	64
Play 'N' pages,	Start page 'X'	(buffered)	65
Write Data,	Start page 'P'		66
Read Data,	Start page 'P'		67
Write Data,	Continue		68
Read Data,	Continue		69
Sub-Audio Signalling Processor 1			**FX805**
Write to Control Register			70
Read Status Register			71
Read CTCSS Rx Data			72
Write to CTCSS/NRZ Tx			73
Read NRZ Rx Data			74
Write to NRZ Data Tx			75
Write to Gain Set			76
Sub-Audio Signalling Processor 2			**FX805**
Write to Control Register			78
Read Status Register			79
Read CTCSS Rx Data			7A
Write to CTCSS/NRZ Tx			7B
Read NRZ Rx Data			7C
Write to NRZ Data Tx			7D
Write to Gain Set			7E
"C-BUS" Performance Testing			AA
"C-BUS" Performance Testing			FF

(b) Reserved Addresses – "C-BUS" Addresses (HEX) reserved for future DBS 800 microcircuit/system use

General Functions	02	to	07
Future Audio Processors	14	to	1F
Future Speech Products	20	to	2F
Future Audio Signalling Processors	37	to	3F
Future FFSK Modems	45	to	47
Future FFSK Modems	4D	to	4F
Future DVSR Codecs	6A	to	6F

Future Sub-Audio Signalling Processors			77
Future Sub-Audio Signalling Processors			7F
Future Products	80	to	8F
Future Products	90	to	9F
Future Products	D0	to	DF
Future Products	E0	to	EF

(c) Spare Addresses – "C-BUS" Addresses (HEX) that will not be allocated for DBS 800 microcircuit/system use and are available for custom use

08 to 0F	50 to 54	56 to 5F	A0 to A9
AB to AF	B0 to BF	C0 to CF	F0 to FE

Table 1 DBS 800 "C-BUS" Address Allocations

"C-BUS" Performance Testing

To enable the effect of "C-BUS" activity on audio microcircuit noise levels to be assessed 4 addresses are allocated for "C-BUS" performance testing:

00_H	00000000	– all 0's
55_H	01010101	– bit reversals
AA_H	10101010	– bit reversals
FF_H	11111111	– all 1's

These 'Performance' Address/Command bytes, when following an active Chip Select are ignored by the DBS 800 chip-set.

Controlling Protocol...

"C-BUS" Timing Information

Figure 4 shows the timing parameters for two-way communication between the µController and DBS 800 peripherals on the "C-BUS." Figure 5 shows the timing relationships between the Serial Clock and Data.

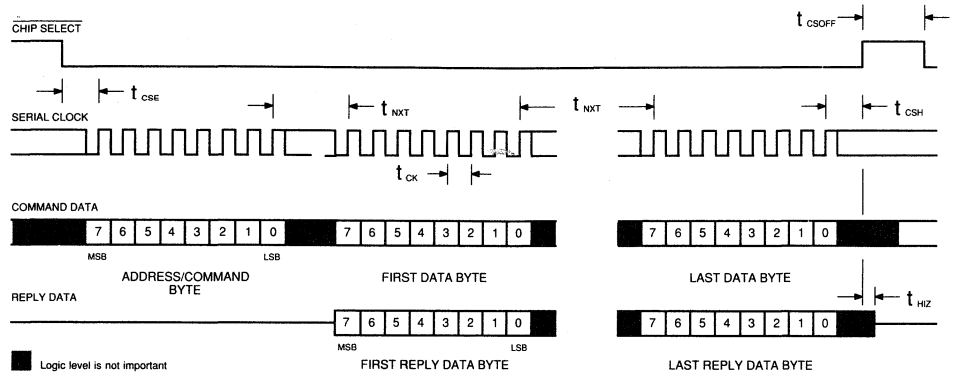


Fig.4 "C-BUS" Timing Information

NOT TO SCALE

Timing Specification – Figures 4 and 5

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"	1	2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"	1	4.0	–	–	µs
t_{HIZ}	"CS-High to Reply Output Tri-state"		–	–	2.0	µs
t_{CSOFF}	"CS-High" Time between transactions	1	2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time	1	2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time	1	4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns
t_{RDS}	"Reply Data Set-Up" Time		250	–	–	ns
t_{RDH}	"Reply Data Hold" Time		50.0	–	–	ns

Notes

1. These Minimum "C-BUS" Timing values are altered during operation of the FX802 DVSR Codec.
2. When addressing DBS 800 microcircuits on the "C-BUS," always use the information published in current Data Sheet documents.

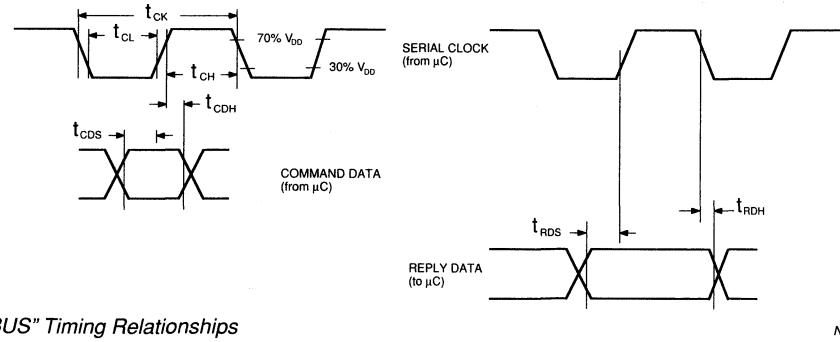


Fig.5 "C-BUS" Timing Relationships

NOT TO SCALE

System Audio Interconnections

Figure 6 gives an example of DBS 800 microcircuit transmit and receive audio paths and interconnections.

External components shown are those recommended in the individual Data Sheet documents. Components identified by an "S" are viewed in this diagram as System Components, which are calculated to perform a specific function within the overall DBS 800 audio system. Table 2 shows recommended System Component values together with brief notes on their calculation.

System Component	Recommended Value	Remarks – *with reference to Figure 6*
SC_1 SC_2 SC_3	See Remarks	These capacitor values should be chosen with regard to the desired frequency response and input impedances of the modulation and loudspeaker amplifier circuits.
SR_1	100kΩ	The feedback resistor of the FX806 Modulation Summing Amplifier. This amplifier satisfies the input gain and matching requirements of the remaining DBS 800 devices.
SR_2	1.0MΩ	Chosen, in conjunction with SR_1, to provide a sub-audio signal level of -20.0dB to the Modulator.
SR_3 SR_4	100kΩ 100kΩ	Chosen, in conjunction with SR_1, to present audio and in-band signalling levels of 0dB to the Modulator.
SR_5	100kΩ	The feedback resistor of the FX803 Summing Amplifier. This amplifier regulates the signal level output of Tone Generators 1 and 2 which in turn are input to the Transmit Audio BUS by Switch 2 and SR_4.
SR_6 SR_7	82.0kΩ 120kΩ	Chosen, in conjunction with SR_5, to produce a 3.0dB tone-differential (twist) when the FX803 is employed as a DTMF decoder. For selcall applications different output levels may be required, or the signal level from Tone Generator 1 attenuated by the FX806 Modulator Drivers.
SR_8	100kΩ	Chosen, in conjunction with SR_1, to provide an FFSK signalling level of 0dB to the Modulator.

Table 2 Recommended "System Component" Values

Notes – *with reference to Figure 6*

(1) The Audio Switch (Sw1) of the FX803 is used, in this example application, to allow interruption of the transmitter modulation path if it is required to provide a CUE (beep) from the tone generator to the loudspeaker.

(2) To demonstrate the versatility of the FX806 microphone input stage, microphone input components are shown in a single-ended configuration. The current FX806 Data Sheet shows a differential input configuration. Relevant component values are the same for both applications.

(3) It is recommended that, to improve screening and reduce noise levels around DBS 800 microcircuits, any unused pins are connected to V_{SS}. This includes inputs to on-chip amplifiers and switches if not employed within an application.

(4) Table 3 gives a guide to the relevant signal levels used in the DBS 800 System.

Signal Level (dB)	Amplitude (mVrms)	Tx Deviation (%)
-30.0	9.7	
-20.0	30.8	
-15.5	51.3	10
-9.6	102	20
-6.0	154	30
-3.5	205	40
-1.6	256	50
0	308	60
1.3	359	70
2.5	410	80
3.5	462	90
4.4	513	100

Table 3 Audio Signal Levels

System Audio Interconnections...

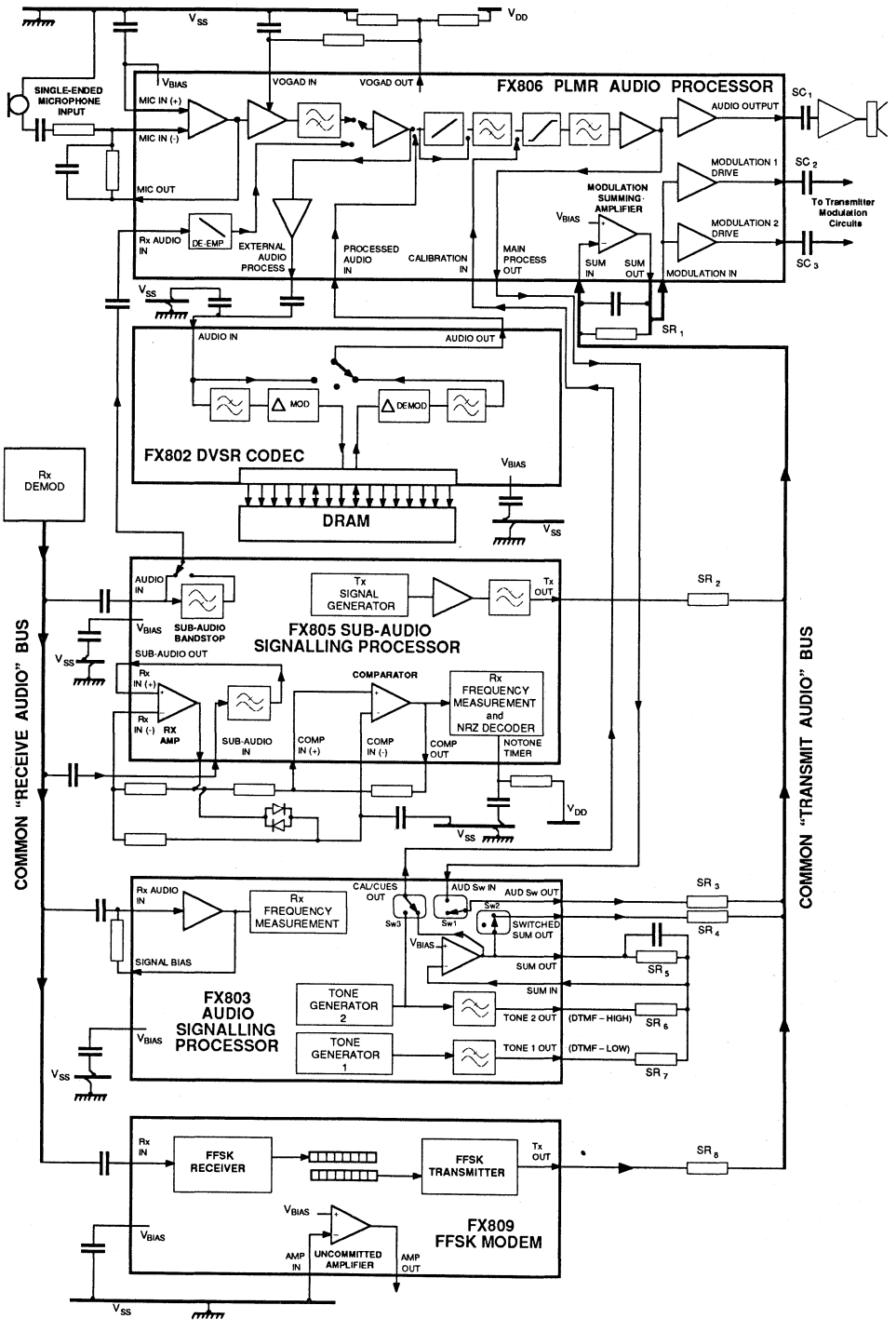


Fig.6 Example "DBS 800 System" Analogue Signal Connections

Application Information

Xtal Oscillator Circuits

These Application Notes, which are derived from CML Application Note *D/XT/1 April 1986*, discuss a general Xtal oscillator circuit applicable to most individual CML microcircuits, and a recommended oscillator configuration that can be used with the DBS 800 Series microcircuits.

Figure 7 shows the standard Xtal oscillator circuit from which most recommended Data Sheet circuits, including DBS 800, are derived.

The standard on-chip CML CMOS oscillator circuit will function correctly with the majority of Xtals, however the use of this circuit with a few Xtal types may cause the following problems:

1 Excessive drive level to the Xtal.

2. Excessive over-voltage, outside the device maximum ratings, at the oscillator input pin. This over-voltage may show itself as degraded microcircuit performance.

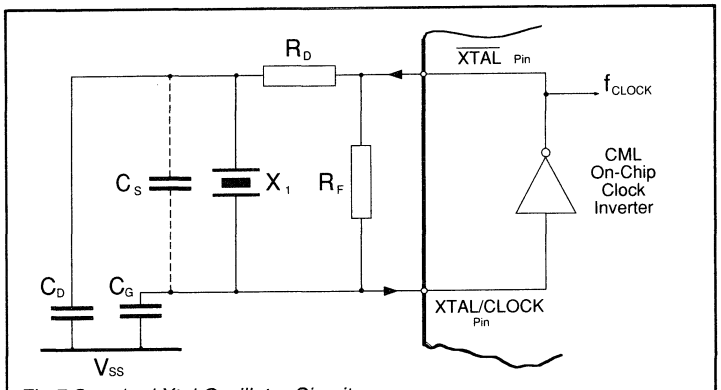


Fig.7 Standard Xtal Oscillator Circuit

Standard Xtal Oscillator Components

R_F Feedback Resistor

To set the bias point of the internal amplifier. Low values of R_F will reduce loop-gain and disturb the phase of the feedback network. *Typical value = 1.0MΩ ± 20% in a range of 1.0MΩ to 20MΩ.* In the DBS 800 series, this resistor is included within the FX806.

R_D Drive Resistor

Used to limit the Xtal drive level by forming a voltage-divider between R_D and C_D. R_D also stabilizes the oscillator against changes in the output impedance of the inverter. To verify that the maximum operating supply voltage does not overdrive the Xtal, observe the output frequency as a function at the buffered output. Under proper operating conditions the frequency should increase slightly (a few ppm) as the supply voltage increases. If the Xtal is being overdriven, an increase in supply will normally cause a decrease in frequency or instability. If the latter is the case (i.e. Xtal being overdriven), increase the value of R_D *(refer to the Xtal manufacturers recommendations).*

X_1 Xtal

A parallel resonant Xtal to the value recommended in the relevant Data Sheet.

C_D Drain Capacitor

To provide phase shift and reduce Xtal drive. Large values of C_D tend to stabilize the oscillator against variations in power supply voltage but also reduce the tuning capability of the oscillator and overtone activity. *A typical value is 33.0pF ± 20% (Xtal manufacturer may recommend 5 – 40pF).*

C_G Gate Capacitor

To provide phase shift and input voltage for the amplifier. In some oscillator circuits C_G is used to adjust the oscillator to frequency although this generally may not be required. Large values of C_G reduce loop-gain and increase stability. C_G may be used to reduce over-voltage at the inverter input. However, the reduction in loop-gain may cause oscillator start-up problems. *C_G value will be typically 5 – 65pF ± 20%, (refer to Xtal manufacturers recommendations).*

C_S Stray Capacitance

Due to the low motional capacitance of small Xtals and the high inverter input impedance, the designer should be concerned with circuit board layout. For best oscillator performance C_S should be less than 1.0pF.

Application Information .....

DBS 800 Xtal Oscillator Configurations

It is recommended that the standard Xtal Oscillator circuit shown in Figure 8 be used for all stand-alone DBS 800 microcircuits, whilst noting that the FX806A PLMR Audio Processor has the feedback resistor R_F incorporated on chip.

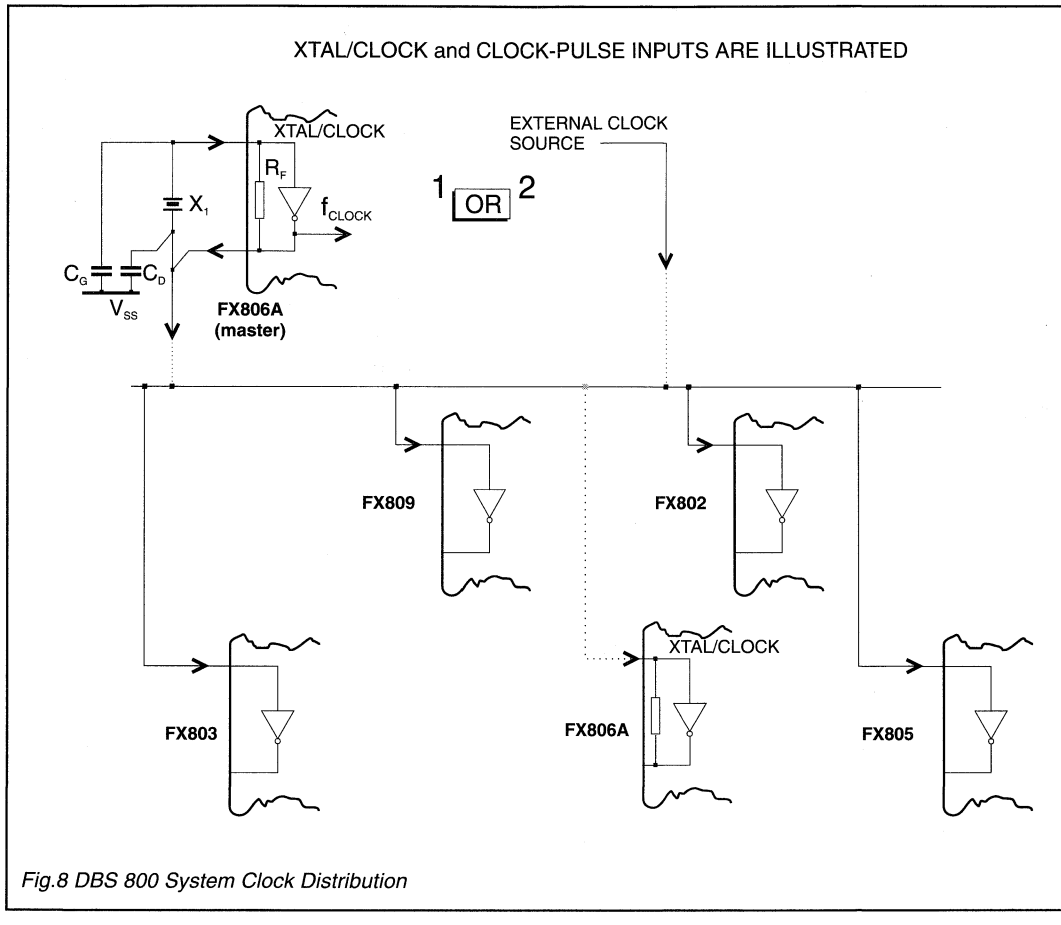


Fig.8 DBS 800 System Clock Distribution

Xtal/Clock Distribution

Although all DBS 800 microcircuits (with the exception of the 24-pin/lead versions of the FX802 DVSR Codec) have on-chip oscillator inverters and may therefore operate independently, there are however obvious advantages to driving all of the microcircuits in a system from a single Xtal/clock source.

Figure 8 shows two methods of driving DBS 800 microcircuits from a single source:

1 Using a single Xtal at the FX806A 'Master', and using this output clock signal to supply the remaining microcircuit inverters in parallel. The value of C_D should be adjusted to allow for the additional driven microcircuits.

2 Supplying all DBS 800 microcircuits, in parallel, from an external low-impedance source.

In any application, when using clock frequencies of this order, care should be taken, in the layout and length of tracks, to minimise stray capacitances and inductances.

Application Information...

DBS 800 Xtal/Clock Frequencies

The DBS 800 family of microcircuits can be driven from either a Xtal circuit or an externally derived clock-pulse input, such as the output from a µProcessor or system clock oscillator. Table 4 shows the Sample Clock Rates employed within DBS 800 microcircuits relative to Xtal/clock input frequencies.

All DBS 800 microcircuits will operate with Xtal/clock frequencies of between 4.00MHz and 4.10MHz, it should be noted that:

(a) a 4.032MHz Xtal/clock input will produce an accurate 1200 baud rate in the FX809 FFSK Modem.

(b) a 4.096MHz Xtal/clock input will generate an accurate 16kb/s and 32kb/s sampling clock rate in the FX802 DVSR Codec.

(c) driving all DBS 800 microcircuit clock generators (and if possible, the µController) from a single clock source prevents possible 'beat-frequencies' and is therefore preferable.

DBS 800 microcircuit audio frequency responses and internal sampling clock rates will vary with respect to Xtal/clock frequency.

		Xtal/Clock Frequencies (MHz)		
		4.000	4.032	4.096
Microcircuit Functions		**Sample Clock Rates (kHz)**		
FX802 DVSR Codec				
Voice Filters	at 16, 32 & 64kbit/s	125	126	128
Voice Filters	at 25 & 50kbit/s	100	100.8	102.4
Voice Sample Rates *(Nominal)*	16.0kbit/s	15.625	15.75	16.0
	25.0kbit/s	25.0	25.2	25.6
	32.0kbit/s	31.25	31.5	32.0
	50.0kbit/s	50.0	50.4	51.2
	64.0kbit/s	62.5	63.0	64.0
FX803 Audio Signalling Processor				
Tone Filters	Max.	166	168	170
	Min.	13.15	13.26	13.47
Digital Filters	High	13.8	14.0	14.2
	Mid.	6.9	7.0	7.1
	Ext.	27.0	28.0	28.4
FX805 Sub-Audio Signalling Processor				This Xtal/clock frequency (4.096MHz), if employed with these microcircuits (FX805 or FX806), may produce sampling clock rates that place the voice-filter passband frequencies outside CEPT specifications.
Voice Filters		125	126	
Tx Filters	Max.	62.5	63.0	
	Min.	12.5	12.6	
Rx Filters		35.7	36.0	
	or	25.0	25.2	
Digital Filters		1.04	1.05	
FX806 PLMR Audio Processor				
Voice Filters		125	126	
FX809 FFSK Modem				
Tx Filters		250	252	256
	or	166	168	170
Rx Filters		125	126	128

Table 4 Examples of DBS 800 Microcircuit Sample Rates

FX802
DVSR CODEC

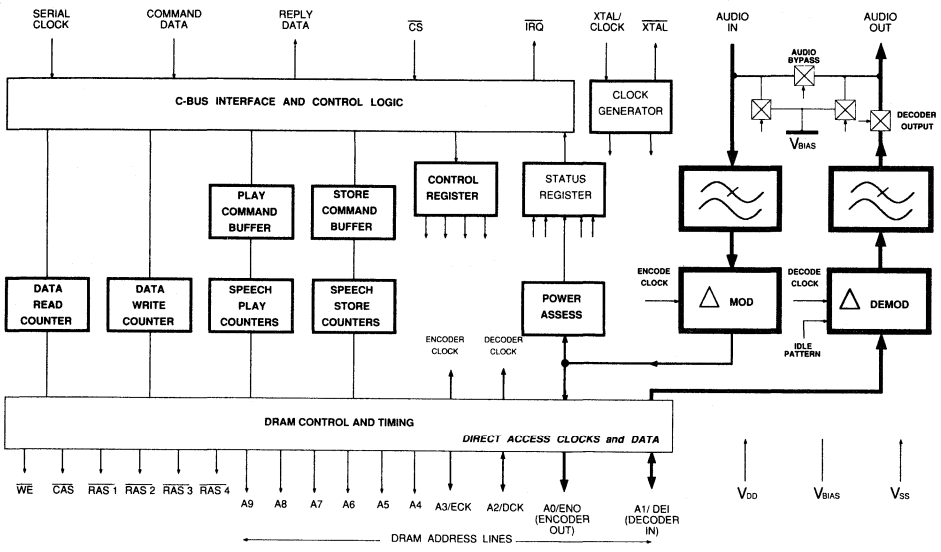


Fig.1 FX802 DVSR Codec

Brief Description

The FX802 DVSR Codec contains:

A Continuously Variable Slope Delta Modulation (CVSD) encoder and decoder.

Control and timing circuitry for up to 4Mbits of external Dynamic Random Access Memory (DRAM).

"C-BUS" µProcessor interface and control logic.

When used with external DRAM, the FX802 has four primary functions:

- **Speech Storage**
  Speech signals present at the Audio Input may be digitized by the CVSD encoder, and the resulting bit stream stored in DRAM. This process also provides readings of input power level for use by the system µController.
- **Speech Playback**
  Previously digitized speech data may be read from DRAM and converted back into analogue form by the CVSD decoder.
- **Data Storage**
  Digital data sent over the "C-BUS" from the system µController may be stored in DRAM.
- **Data Retrieval**
  Digital data may be read from DRAM and sent over "C-BUS" to the system µController.

Speech storage and playback may be performed concurrently with data storage or retrieval.

The FX802 may also be used without DRAM (as a "stand-alone" CVSD Codec), in which case direct access is provided to the CVSD Codec digital data and clock signals.

All functions are controlled by "C-BUS" commands from the system µController.

The Storage, Recovery and Replay functions of the FX802 can be used for:

- Answering Machine applications, where an incoming speech message is stored for later recall.
- Busy Buffering, an outgoing speech message is stored temporarily until the transmit channel becomes free.
- Automatic transmission of pre-recorded 'Alarm' or status announcements.
- Time Domain Scrambling of speech messages.
- VOX control of transmitter functions.
- Temporary Data Storage applications, such as buffering of over-air data transmissions.

On-chip the Delta Codec is supported by input and output analogue switched-capacitor filters and audio output switching circuitry. The DRAM control and timing circuitry provides all the necessary address, control and refresh signals to interface to external DRAM.

The FX802 DVSR Codec is a low-power 5-volt CMOS LSI device.

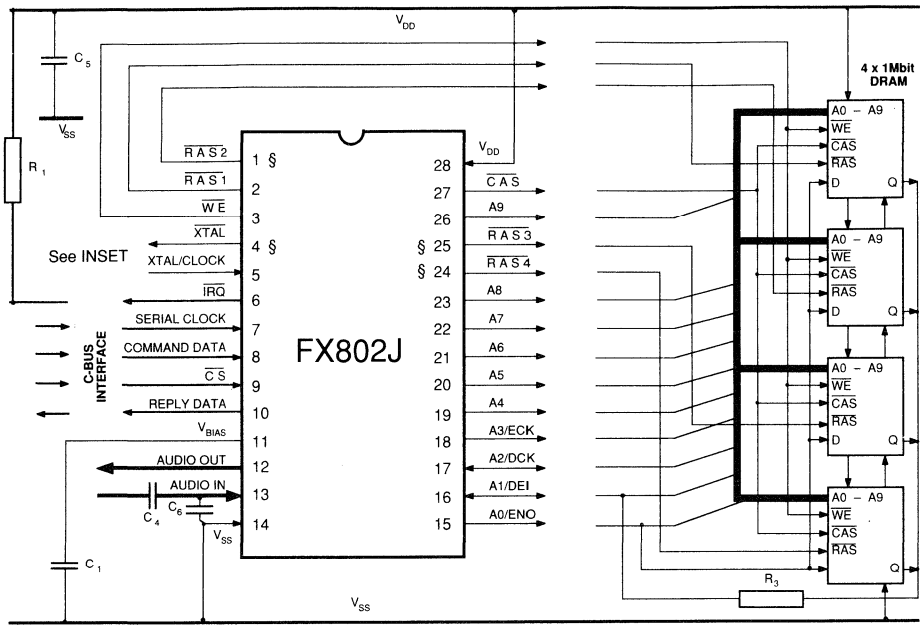
Publication D/802/3 July 1994
Provisional Issue

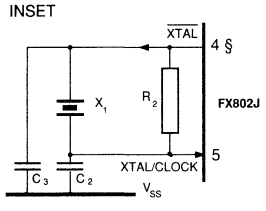
Pin Number FX802 J	Pin Number FX802 LG/LS	Function
1		**Row Address Strobe 2 ($\overline{RAS2}$):** Should be connected to the Row Address Strobe input of the second 1Mbit DRAM chip (if fitted).
2	1	**Row Address Strobe 1 ($\overline{RAS1}$):** Should be connected to the Row Address Strobe input of the first DRAM chip.
3	2	**Write Enable ($\overline{WE}$):** The DRAM Read/Write control pin.
4		**$\overline{Xtal}$:** The output of the on-chip clock oscillator. External components are required at this output when a Xtal is employed. A Xtal cannot be used with the 24-pin version.
5	3	**Xtal/Clock:** The input to the on-chip clock oscillator inverter. A 4.0MHz Xtal or externally derived clock should be connected here, see Figure 2. This clock provides timing for on-chip elements, filters etc. A Xtal cannot be used with the 24-pin version. Various Xtal frequencies can be used with this device, see Table 3 for the sampling clock rate variations.
6	4	**Interrupt Request ($\overline{IRQ}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. The pin has a low-impedance pulldown to logic "0" when active and a high impedance when inactive. Conditions indicated by this function are: Power Reading Ready, Play Command Complete, Store Command Complete.
7	5	**Serial Clock:** The "C-BUS," serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the DVSR Codec. See Timing Diagrams and System Support Document, Document 2. The clock-rate requirements vary for differing FX802 functions.
8	6	**Command Data:** The "C-BUS," serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams and System Support Document, Document 2.
9	7	**Chip Select ($\overline{CS}$):** The "C-BUS", data transfer control function, this input is provided by the µController. Command Data transfer sequences are initiated, completed or aborted by the CS signal. See Timing Diagrams and System Support Document, Document 2.
10	8	**Reply Data:** The "C-BUS," serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Data Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the µController. See Timing Diagrams and System Support Document, Document 2.
11	9	**V_{BIAS}:** The output of the on-chip analogue circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by a capacitor C_1, See Figure 2.
12	10	**Audio Out:** The analogue signal output.
13	11	**Audio In:** The audio (speech) input. The signal to this pin must be a.c. coupled by a capacitor C_4 and decoupled to V_{SS} by an HF bypass capacitor C_6. For optimum noise performance this input should be driven from a source impedance of less than 100Ω.
14	12	**V_{SS}:** Negative supply rail (GND).

Pin Number Function

FX802 J	FX802 LG/LS	
15	13	**DRAM Data In/A0/ (Direct Access – Encoder Out (ENO)):** Connected to the DRAM data input and address line A0. With no DRAM employed this output is available (in Direct Access mode) as the Delta Encoder digital data output. Direct Access control is achieved by Control Register byte 1 – bit 6.
16	14	**DRAM Data Out/ A1/ (Direct Access – Decoder In (DEI)):** Connected to the DRAM data output and address line A1. With no DRAM employed this pin is available (in Direct Access mode) as the Delta Decoder digital data input. Direct Access control is achieved by Control Register byte 1 – bit 6.
17	15	**DRAM A2/ (Direct Access – Decoder Clock (DCK)):** DRAM address line A2. With no DRAM employed this pin is available (in Direct Access mode) as the Delta Decoder Clock input. Direct Access control is achieved by Control Register byte 1 – bit 6.
18	16	**DRAM A3/ (Direct Access – Encoder Clock (ECK)):** DRAM address line A3. With no DRAM employed this pin is available (in Direct Access mode) as the Delta Encoder Clock output. Direct Access control is achieved by Control Register byte 1 – bit 6.
19	17	**DRAM A4:** DRAM address line A4.
20	18	**DRAM A5:** DRAM address line A5.
21	19	**DRAM A6:** DRAM address line A6.
22	20	**DRAM A7**: DRAM address line A7.
23	21	**DRAM A8:** DRAM address line A8.
24		**$\overline{\text{Row Address Strobe 4}}$ ($\overline{\text{RAS4}}$):** Should be connected to the Row Address Strobe input of the fourth 1Mbit DRAM chip (if fitted).
25		**$\overline{\text{Row Address Strobe 3}}$ ($\overline{\text{RAS3}}$):** Should be connected to the Row Address Strobe input of the third 1Mbit DRAM chip (if fitted).
26	22	**DRAM A9:** DRAM address line A9. This pin is not connected when a 256kbit DRAM is employed. **Note:** To simplify PCB layout, the DRAM address inputs A0 – A8 may be connected in any physical order to the DVSR Codec output pins A0 – A8.
27	23	**$\overline{\text{Column Address Strobe}}$ ($\overline{\text{CAS}}$):** The DRAM Column Address Strobe pin. Should be connected to the CAS pins of all DRAM chips.
28	24	**V_{DD}**: Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the DVSR Codec are dependant upon this supply.

External Components





Component		Value			
R_1	=	22.0kΩ	C_4	=	1.0µF
R_2		1.0MΩ	C_5		1.0µF
R_3		1.0kΩ	C_6		1.0nF
C_1		1.0µF	X_1		4.00MHz
C_2		33.0pF		or	4.032MHz
C_3		33.0pF		or	4.096MHz

Tolerance: R = ±10% C = ±20%

Fig.2 Recommended Component and DRAM Connections

Notes

1. Xtal circuitry shown INSET is in accordance with CML Application Note D/XT/1 April 1986.

2. External Xtal circuitry is not applicable to the 24-pin/lead versions of this device, only a clock pulse input can be used.

3. Functions whose pins are marked § above are not available on the 24-pin/lead versions of this device. Pin numbers illustrated are for 28-pin versions.

4. Table 3 details the actual encoder/decoder sample rates available using the Xtal frequencies recommended above.

5. R_1 is used as the DBS 800 system common-pullup for the "C-BUS" Interrupt Request ($\overline{IRQ}$) line, the optimum value will depend upon the circuitry connected to the $\overline{IRQ}$ line. Up to 8 peripherals may be connected to this line.

6. Recommended DRAM Parameters:
   256kbit x 1 or 1Mbit x 1 Dynamic Random Access Memory with 'CAS before RAS' refresh mode, maximum Row Address Access time = 200nsec.

   Example DRAM types:
   256kbit (262,144bits)
   - Texas Instruments TMS4256–20
   - Hitachi HM51256–15

   1Mbit (1,048,576bits)
   - Texas Instruments TMX4C1024–15
   - Hitachi HM511000–15

7. Figure 2 (above) shows connections to 4 x 1Mbit sections of DRAM. If desired, to simplify PCB layout, the DRAM inputs A0 to A8 may be connected in any order to the FX802 DVSR Codec output pins A0 to A8. Connections to 256kbit DRAM are similar, but A9 unconnected.

8. When using the FX802 "stand-alone (Direct Access)," no DRAM should be connected.

Controlling Protocol

Control of the functions of the FX802 DVSR Codec is by a group of Address/Commands (A/Cs) and appended instructions or data to and from the system µController (see Figure 5). The use and content of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB	+	Data Byte/s
General Reset	01	0 0 0 0 0 0 0 1		
Write to Control Register	60	0 1 1 0 0 0 0 0	+	2 byte Instruction to Control Register
Read Status Register	61	0 1 1 0 0 0 0 1	+	1 byte Reply from Status Register
Store 'N' pages. Start page 'X'	62	0 1 1 0 0 0 1 0	+	2 bytes Command – Immediate
Store 'N' pages. Start page 'X'	63	0 1 1 0 0 0 1 1	+	2 bytes Command – Buffered
Play 'N' pages. Start page 'X'	64	0 1 1 0 0 1 0 0	+	2 bytes Command – Immediate
Play 'N' pages. Start page 'X'	65	0 1 1 0 0 1 0 1	+	2 bytes Command – Buffered
Write Data. Start page 'P'	66	0 1 1 0 0 1 1 0	+	2 bytes 'P' + Write data
Read Data. Start page 'P'	67	0 1 1 0 0 1 1 1	+	2 bytes 'P' + Read data
Write Data – Continue	68	0 1 1 0 1 0 0 0	+	Write data
Read Data – Continue	69	0 1 1 0 1 0 0 1	+	Read data

Table 1 "C-BUS" Address/Commands

Address/Commands

Instruction and data transactions to and from this device consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data, or
(ii) a Status or data Reply.

Control and configuration is by writing instructions from the µController to the Control Register (60_H).
Reporting of FX802 configurations is by reading the Status Register (61_H). Instructions and data are transferred, via "C-BUS," in accordance with the timing information given in Figures 5 and 6.
A complete list of DBS 800 "C-BUS" Address locations is published in the System Support Document, Document 2.

Speech

The delta encoder and decoder sampling rates are independently set, via the Control Register (Table 4), to (nominally) 16, 25, 32, 50 or 64kbits/s (see Tables 2 and 3), allowing the user to choose between speech-quality and storage-time, whilst providing for time-compression or expansion of the speech signals.

The DVSR Codec can handle from 256kbits to 4Mbits of DRAM, giving, in the case of 32kbit/s sampling rate, from 8 to 131 seconds of speech storage.

For speech storage purposes, the memory is divided into 'pages' of 1024 bits each, corresponding to 32ms at a 32kbit/s sampling rate.

A 256kbit DRAM contains	256 pages.
A 1Mbit DRAM contains	1024 pages.
4Mbit of DRAM contains	4096 pages.

The Delta Codec may be used without DRAM, when the decoder sampling rate (8 to 64 kbits/s) is determined by an external clock source applied to the Decoder Clock pin.

Operation with DRAM

The FX802 can operate with up to 4Mbits of DRAM. When used with DRAM the DVSR Codec performs four main functions under the control of commands received over the "C-BUS" interface from the µController:

Stores Speech by digitally encoding the analogue input signal and writing the resulting digital data into the associated Dynamic RAM (DRAM).

Plays stored speech by reading the digital data stored in the DRAM and decoding it to provide an analogue output signal.

Writes data sent over the "C-BUS" from the µController to DRAM.

Reads data from DRAM, sending it to the µC over the "C-BUS".

'Data' is directed to and from DRAM by the on-chip DRAM Controller.

Store and Play Speech Commands
Speech storage and playback may take place simultaneously.

These commands are transmitted, via "C-BUS," to the FX802, in the form:

STORE or PLAY 'N' (1024-bit) pages (of encoded speech data) starting at page 'X.'

'N' is any number from 1 to 16 (pages) and **'X'** from (page) 0 to 4095 (4Mbit DRAM), as illustrated below.
Preceded by the A/C, this command writes 16-bits (byte 1 (first) and byte 0) of data from the µC to the FX802 Store or Play Command Buffer.

MSB Byte 1								Byte 0 LSB							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
'N'								'X'							

Store and Play Speech

Speech Store Commands

62_H STORE 'N' PAGES – START PAGE 'X' (immediate).

63_H STORE 'N' PAGES – START PAGE 'X' (buffered).

The digitised speech from the Delta Encoder is stored in consecutive DRAM locations with the Speech Store Counters sequencing through the DRAM addresses and counting the number of complete 'pages' stored since the start of execution of the command.
As soon as the command has terminated the following events take place:

(1) The "Store Command Complete" bit in the Status Register (Table 6) is set.

(2) An "Interrupt Request" ($\overline{IRQ}$) is sent (if enabled) to the µC.

(3) The next Speech Store command (if present) is immediately taken from the Store Command Buffer and execution of the new command commences.

The $\overline{IRQ}$ output is cleared by reading the Status Register.

61_H READ STATUS REGISTER (Table 6).

To provide continuity of speech commands, both Store and Play commands can be presented to the FX802 in one of two formats; *Immediate or Buffered.*

An *Immediate* command will be started on completion of its loading, irrespective of the condition of the current command.

A *Buffered* command will be acted upon on the completion of the current Store or Play command, unless Speech Synchronization Bits (Control Register) are set.

Buffering of commands lets the DVSR Codec execute a series of commands without intervening gaps, even though the µController may take several milliseconds to respond to each "Command Complete" Interrupt Request.

In either case, the Store or Play Command Complete bit of the Status Register will be cleared.

Speech Playback is controlled by similar commands:

64_H PLAY 'N' PAGES – START PAGE 'X' (immediate).

65_H PLAY 'N' PAGES – START PAGE 'X' (buffered).

using the Speech Play Counters and Play Command Buffer.

As soon as the Play Command has completed, the "Play Command Complete" bit in the Status Register is set and an Interrupt Request generated (if enabled).

If no 'next' command is waiting in the Play Command Buffer when a speech Play command finishes, a continuous idle code (0101.....0101) will be fed to the Delta Decoder.

Speech "data" is stored or recovered at the selected Encode or Decode sample rate (Table 3).
Store or Play Command Complete bits in the Status Register are cleared by the next Store or Play command received from the µC, or by a General Reset command.

Store/Play Speech Synchronization – (Table 4)

This facility is provided, primarily, for Time Domain Scrambling applications.

Speech Synchronization bits in the Control Register will produce the effects described below:

No Speech Sync Set; Store and Play operations may take place completely independently.

Store after Play; The next "buffered" Store command will start *on completion of a Play operation*, whilst the next Play command (if any) sequence continues normally.

Play after Store; The next "buffered" Play command will start *on completion of a Store operation*, whilst the next Store command (if any) sequence continues normally.

These actions will continue whilst 'Speech Sync' bits remain set.

DRAM Speech Capacity

28-pin/lead versions of the FX802 may be used with a single 256kbit DRAM or with up to 4 x 1Mbit DRAM.
24-pin/lead versions may only be used with a single 256kbit or 1Mbit DRAM. The different Encode and Decode sampling clock rates available enable the user to set voice store and play times against recovered speech quality. Table 2 gives information on storage capacity and Store/Playback times. Speech data can be replayed at a different sample rate or in a reverse sequence, see Control Register for details.

DRAM Size	Available Bits	"Speech Pages"	Nominal Sample Rates (kbits/s) 16	25	32	50	64
256kbits	262144	256	16.0	10.0	8.0	5.0	4.0
1024k	1048576	1024	65.0	42.0	32.0	20.0	16.0
2Mbits	2097152	2048	131.0	84.0	65.0	42.0	32.0
3M	3145728	3072	196.0	126.0	98.0	63.0	49.0
4M	4194304	4096	262.0	168.0	131.0	84.0	65.5
			Store and Play Times (seconds)				

Table 2 Sampling Clock Rates vs Speech Storage/Playback Times

Data Operations

Data Storage and Recovery

For the purpose of storing data sent via "C-BUS" from the µC, the memory (DRAM) is divided into 'data-pages' of 64-bits (8-bytes).

A single 256kbit DRAM contains 4096 data-pages.
A single 1Mbit DRAM contains 16384 data-pages.
4Mbit DRAM contains 65536 data-pages.

In accordance with "C-BUS" timing specifications, data is handled 8-bits (1-byte) at a time although any number of 8-bit blocks of data may be written-to or read-from the DRAM by a single command.

The data transfer action is terminated by the Chip Select line being taken to a logic "1.

"C-BUS" Data Transfer Limitations

For those commands which transfer data over the "C-BUS" between DRAM and the µController (Write and Read Data) the "C-BUS" Serial Clock rate is limited to a maximum of:

125kHz if the VSR Codec is executing Store and Play commands.

250kHz if no speech Store or Play commands are active.

All other commands and replies (Control, Status, General Reset) may use a maximum clock rate of 500kHz. See Figure 5.

Read and Write Data actions are explained below

Read Data

67_H READ DATA – START PAGE "P"

Sets the Data Read Counter to "P" page and then reads data bytes from successive DRAM locations, sending them to the µC as Reply Data bytes incrementing the Data Read Counter by 1 for each bit read.

69_H READ DATA – CONTINUE

Reads data bytes from successive DRAM locations determined by the Data Read Counter incrementing the counter by 1 for each bit read.

Write Data

66_H WRITE DATA – START PAGE "P"

Sets the Data Write Counter to "P" page and then writes data bytes to successive DRAM locations, incrementing the Data Write Counter by 1 for each bit received via the "C-BUS."

The Start Page "P," is indicated by loading a 2-byte word after the relevant Address/Command byte. This 16-bit word allows data-page addresses from 0 to 65535 (4Mbits DRAM).

68_H WRITE DATA – CONTINUE

Writes data bytes to successive DRAM locations determined by the Data Write Counter, incrementing the counter by 1 for each bit received over the "C-BUS."

Encoder and Decoder Sampling Clocks

Encoder and decoder sampling clock rates are programmable via the Control Register. Table 3 shows the range of sampling rates available for differing Xtal/clock input frequencies, and the counter ratios used to produce them.
If different "Store and Play" sampling rates are used in a single operation, only combinations of 25kb/s with 32kb/s or 50kb/s with 64kb/s will give correct output levels in accordance with current specifications. Consideration should be given to the effect of differing Xtal/clock frequencies upon the audio frequency performance of the device.

Control Register *Byte 0, Bits* 5 2	4 1	3 0	Dec. Enc.	Internal Counter Division Ratio	Xtal/clock Frequency (MHz) 4.0	4.032	4.096
					Sampling Rate (kbits/s)		
0	1	1		256	15.625	15.75	16.0
1	0	0		160	25.0	25.20	25.60
1	0	1		128	31.25	31.50	32.0
1	1	0		80	50.0	50.4	51.20
1	1	1		64	62.50	63.0	64.0

Table 3 Sampling Clock Rates Available

With respect to using a single Xtal/clock frequency for all DBS 800 devices in use it should be noted that:
(a) a 4.032MHz Xtal/clock input will produce an accurate 1200 baud rate for the FX809 FFSK Modem
(b) a 4.096MHz Xtal/clock input will generate exactly 16kb/s and 32kb/s Codec sampling clock rates.

"Write to Control Register" — Address/Command 60_H, followed by 2 bytes of Command Data

Setting			Function
Byte 1			***First Byte for Transmission***
(MSB) Bit 7			Not used – Set to "0"
6			**Direct Access**
1			– Encoder Data Out to A0/ENO – Encoder Clock to A3/ECK – Decoder Input from A1/DEI – Decoder Clock from A2/DCK
0			Normal DVSR Operation
5			**Play Counter**
1			Decrement
0			Increment
4			**DRAM Control**
1			Disable DRAM
0			Enable DRAM
3			**Codec Powersave**
1			Powersave Delta Codec
0			Enable Delta Codec
2			**Store Command Interrupt**
1			Enable Interrupt
0			Disable
1			**Play Command Interrupt**
1			Enable Interrupt
0			Disable
0			**Power Reading Interrupt**
1			Enable Interrupt
0			Disable
Byte 0			***Last Byte for Transmission***
(MSB) 7	***6***		**Store/Play Speech Sync**
0	0		No Sync
0	1		No Sync
1	0		Sync – Play after Store
1	1		Sync – Store after Play
5	***4***	***3***	**Decoder Control**
0	0	0	Idle (32kbit/s); Aud O/P via L.P.F.
0	0	1	Idle (32kbit/s); Aud By-Pass
0	1	0	Idle (32kbit/s); Aud O/P at High Z
0	1	1	On – Sampling Rate 16kbit/s
1	0	0	On – " 25kbit/s
1	0	1	On – " 32kbit/s
1	1	0	On – " 50kbit/s
1	1	1	On – " 64kbit/s
2	***1***	***0***	**Encoder Control**
0	0	0	I/P at V_{BIAS} – F/Idle (32kbit/s)
0	0	1	I/P at High Z – F/Idle (32kbit/s)
0	1	0	I/P at High Z – F/Idle (32kbit/s)
0	1	1	On – Sampling Rate 16kbit/s
1	0	0	On – " 25kbit/s
1	0	1	On – " 32kbit/s
1	1	0	On – " 50kbit/s
1	1	1	On – " 64kbit/s

Table 4 Control Register

General Reset

Upon Power-Up the "bits" in the FX802 registers will be random (either "0" or "1"). A General Reset command (01_H) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX802:

Control Register	Set as 00_H
Status Register	Set as 00_H
Clear Store and Play Command Buffers	

Direct Access

Allows external circuitry "Direct Access" to the Delta Codec data and sampling clocks, disabling the DRAM timing circuitry. This permits the Delta Codec section of the FX802 to be used as a "stand-alone" delta modulation voice encoder and decoder.

Input Audio is encoded and made available at the Encoder Out (ENO) pin. Speech data input to the Decoder In (DEI) pin is decoded to give voice-band audio at the Audio Output.

The following points, with respect to Control Register settings, should be considered. Analogue output switching remains under the control of the Control Register, but the Decoder sampling clock rate (8kbit/s to 64kbit/s) must be provided from an external source to the Decoder Clock (DCK) pin. To ensure correct filter setting, Decoder Control bits (Byte 0, Bits 5, 4, 3) should be set to (binary) 1, 1, 1, where the required rate approximates to a multiple of 16kb/s, or (binary) 1, 1, 0, where the required rate approximates to a multiple of 25kb/s.

Both the Encoder internal sampling clock rate and input switching (Table 5) remain under the control of the Control Register. The sampling clock rate is available to external circuitry at the Encoder Clock Out (ECK) pin.

Play Counter

The Play Counter direction may be set to run backwards as well as forwards. This can be used in a scrambling system by replaying speech data in reverse order.

DRAM Control

A logic "1" will disable the DRAM Control timing circuits and associated counters. The "C-BUS" Interface, Clock Generator, Delta Codec and filters remain active. This bit should be set to logic "1" when the FX802 is used in the Direct Access mode.

Minimum DVSR Codec power consumption is achieved by setting both DRAM Control and Powersave bits to a logic "1."

Codec Powersave

A logic "1" puts the Delta Codec and filters into a Powersave mode, with V_{BIAS} maintained.

The Clock Generator, "C-BUS" Interface and DRAM Control and Timing remain active.

Command Interrupt Enable

A logic "1" set at the relevant bit will enable Interrupt Requests to the µController when that command operation is complete.

Store and Play Speech Synchronization

Intended, primarily, for Time Domain Scrambling.

Decoder and Encoder Control

Sets individually, decoder and encoder sampling clock rates and the source of the Audio Output.

Decoder and Encoder Control

Analogue Input and Output Switching

The Control Register, Byte 0 – bits 0 to 5, are used, in conjunction with the codec Powersave Bit (Byte 1 – bit 3) to control codec input/output conditions and sample rates. Figure 3 shows the codec functional situation.

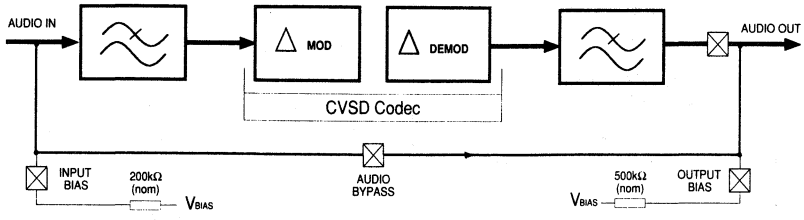


Fig.3 Analogue Control – with reference to Fig.1

Control Register				Circuit Switches			OFF = Switch Open ON = Switch Closed	
Codec Powersave Bit	**Decoder Control "5"**	**"4"**	**"3"**	**Audio By-Pass**	**Audio Out**	**Output Bias**		**Note**
0	0	0	0	OFF	ON	OFF	Decoder 'idling' fed with "1010101 ...." pattern at 32kb/s.	1
0	0	0	1	ON	OFF	OFF		
0	0	1	0	OFF	OFF	OFF		
0	0	1	1	OFF	ON	OFF	Decoder running at the selected sampling rate.	1
–	–	–	–	–	–	–		
0	1	1	1	OFF	ON	OFF		
1	0	0	0	OFF	OFF	ON	Decoder circuits Powersaved	
1	0	0	1	ON	OFF	OFF		
1	0	1	0	OFF	OFF	ON		
1	0	1	1	OFF	OFF	ON		
–	–	–	–	–	–	–		
1	1	1	1	OFF	OFF	ON		
	Encoder Control "2"	**"1"**	**"0"**		**Input Bias**			**2**
0	0	0	0		ON		Encoder running at 32kb/s but Encoder Data Output forced to 'idle' pattern "01010 ..."	
0	0	0	1		OFF			
0	0	1	0		OFF			
0	0	1	1		OFF		Encoder running at selected Sampling Rate	
–	–	–	–		–			
0	1	1	1		OFF			
1	0	0	0		ON		Encoder circuits Powersaved	
–	–	–	–		–			
1	1	1	1		ON			

Table 5 Analogue Control – with reference to Fig.3

Notes

1. If the Delta Codec is in the Direct Access mode, these sampling rates will be as provided by the externally applied clock.
2. The Input Bias switch is operated by the Control Register Codec Powersave' and 'Encoder Control' bits to provide a relatively low impedance path for V_{BIAS} to charge the input coupling capacitor whenever the codec is powersaved, or the Encoder control bits are set to "0," so that input bias can be established quickly prior to operation.

Time Compression of Speech

The 25kb/s and 50kb/s sampling rate options are provided for time compression (and subsequent expansion) of speech signals.

For example, 1.0 second of speech stored at 50kb/s may be transmitted in 0.8 seconds if played out at 64kb/s, and finally restored to its original speed at the receiver by storing at 64kb/s and playing out at 50kb/s. A similar result (with a degraded SINAD) may be achieved by using 25kb/s and 32kb/s sampling rates.

However, the speech frequencies are raised by time compression, and since the signal transmitted to air must be band limited to 3400Hz, the effective end-to-end bandwidth is 0.8 x 3400Hz, which is approximately 2700Hz.

"Read Status Register" – Address/Command, 61_H, followed by 1 byte of Reply Data.

Reading	Function
MSB Bit 7 1	**Power Reading** Ready
6 1	**Store Command** Complete
5 1	**Play Command** Complete

4	***3***	***2***	***1***	***0***	**Power Register Pwr**	**Compand Bits**/page
0	0	0	0	0		0
0	0	0	0	1		1
0	0	0	1	0		2
0	0	0	1	1		3
0	0	1	0	0		4
0	0	1	0	1		5
0	0	1	1	0		6
0	0	1	1	1		7
0	1	0	0	0	-39.0 dB	8
0	1	0	0	1		10
0	1	0	1	0	-36.0	12
0	1	0	1	1		14
0	1	1	0	0	-33.5	16
0	1	1	0	1		18
0	1	1	1	0	-30.0	20
0	1	1	1	1		22
1	0	0	0	0	-28.0	24
1	0	0	0	1		32
1	0	0	1	0	-25.0	40
1	0	0	1	1		48
1	0	1	0	0	-22.0	56
1	0	1	0	1		64
1	0	1	1	0	-19.0	72
1	0	1	1	1		80
1	1	0	0	0	-16.0	88
1	1	0	0	1		128
1	1	0	1	0	-10.0	192
1	1	0	1	1		256
1	1	1	0	0	-6.0	320
1	1	1	0	1		384
1	1	1	1	0	0dB	448
1	1	1	1	1		512

Table 6 Status Register

Interrupts
An Interrupt Request (IRQ), (if enabled by the Control Register) is produced by the FX802 to report the following actions:

Power Reading Ready
Store Command Complete
Play Command Complete.

When an Interrupt Request is produced the Status Register must be read to ascertain the source of the interrupt. This action will clear the $\overline{IRQ}$ output.

Store Command Complete bit
(and an interrupt) is set on completion of a Store command. This bit is cleared by loading the next Store command, or by a General Reset command (01_H).

Play Command Complete bit
(and an interrupt) is set on completion of a Play command. This bit is cleared by loading the next Play command, or by a General Reset command (01_H).

Power Reading Ready bit
(and an interrupt) is set for every 1024 (1 page) voice-data bits from the Encoder. This bit is cleared after reading the Status Register, or by a General Reset command (01_H).

Power Register
The power assessment element shown in Figure 1 assesses the input signal power for each encoded 'page' (every 1024 encoder output bits) by counting the number of 'compand bits' (000 or 111 sequences in the output bit-stream) produced during that 'page,' shown in Table 6, with typical encoder input power levels (dB).
Power Reading measurements (Bits 0 – 4) are produced under the same conditions as in Figure 4.

At the end of each 'page' the "Power Reading Ready" bit of the Status Register is set, an Interrupt Request is generated (if enabled) and the resulting count converted to a 5-bit quasi-logarithmic form.

The Power Register reading is interpreted as below.

00000 represents	0 compand bits
00001 represents	1 compand bit
11111 represents	512 compand bits – the maximum.

This "Power" reading is placed in the Status Register where it can be read by the µC.

Figure 4 shows this output in graphical form, indicating the typical Input Power Level.

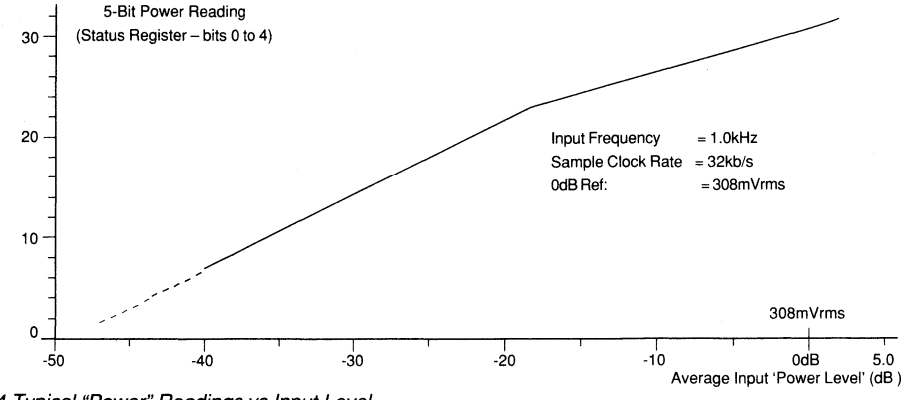


Fig.4 Typical "Power" Readings vs Input Level

Timing Information

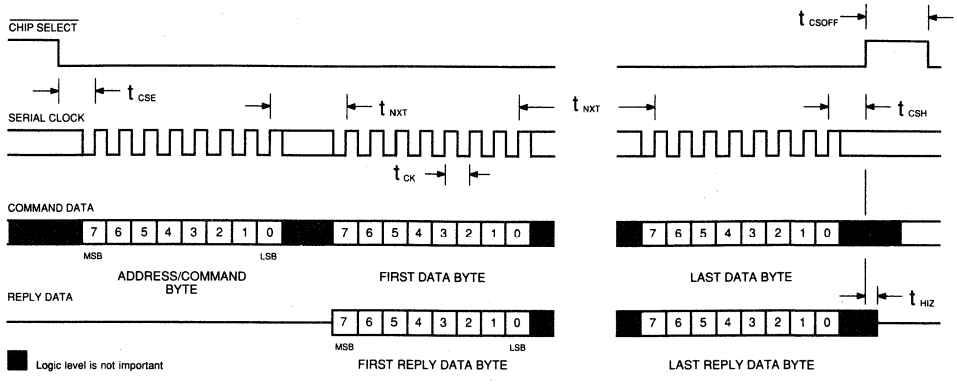


Fig.5 "C-BUS" Timing Information

NOT TO SCALE

"C-BUS" Timing – Figure 5

Parameter	Min.			Max.	Unit
	a	b	c		
t_{CSE}	2.0	4.0	8.0	–	µs
t_{CSH}	4.0	4.0	8.0	–	µs
t_{HIZ}	–	–	–	2.0	µs
t_{CSOFF}	2.0	4.0	8.0	–	µs
t_{NXT}	4.0	8.0	16.0	–	µs
t_{CK}	2.0	4.0	8.0	–	µs

Direct Access Timing – Figure 6

Parameter	Min.	Typ	Max.	Unit
t_{CH}	1.0	–	–	µs
t_{CL}	1.0	–	–	µs
t_{SU}	450	–	–	ns
t_H	600	–	–	ns
t_{PCO}	–	–	750	ns

$t_{SU} + t_H$ = Data True Time

Notes

(1) **Minimum Timing Values**
- (a) For all commands except "Read Data" and "Write Data" commands.
- (b) For "Read Data" and "Write Data" commands when no "Speech Store" or "Speech Play" commands are active.
- (c) For "Read Data" and "Write Data" commands when "Speech Store" or "Speech Play" commands are active.

(2) Depending on the command, 1 or 2 bytes of Command Data are transmitted to the peripheral MSB (bit7) first, LSB (bit0) last. Reply Data is read from the peripheral MSB (bit7) first, LSB (bit0) last.

(3) To allow for differing µController serial interface formats "C-BUS" compatible ICs are able to work with either polarity Serial Clock pulses.

(4) Data sent from the µController is clocked into the FX802 on the rising edge of the Serial Clock pulses. Reply Data sent from the FX802 to the µController is clocked into the µController when the Serial Clock is "high."

(5) Loaded commands are acted upon at the end of each command.

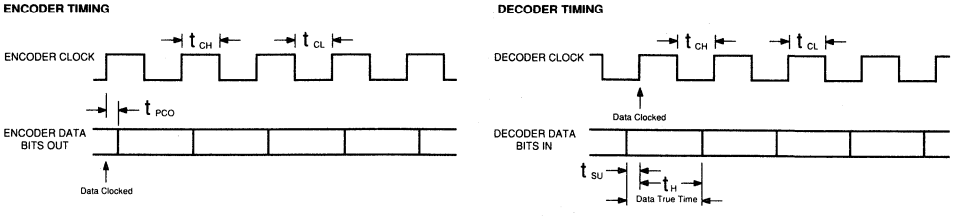


Fig.6 Codec Direct Access Timing

NOT TO SCALE

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX802J**	-40°C to +85°C (cerdip)
	FX802LG/LS	-40°C to +85°C (plastic)
Storage temperature range:	**FX802J**	-55°C to +125°C (cerdip)
	FX802LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.0MHz. Standard Test Signal f_0 = 1.0kHz. Sample Rate = 31.25kbits/s
Audio Level 0dB ref: = 308mVrms .

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply Current (enabled)	1	–	7.0	–	mA
Supply Current (all powersaved)	1	–	1.0	–	mA
Digital Interface					
Input Logic "1"	2, 4	3.5	–	–	V
Input Logic "0"	2, 4	–	–	1.5	V
Output Logic "1"					
at IOH = -120µA	8, 4	4.6	–	–	V
at IOH = -50µA	3, 4	4.6	–	–	V
at IOH = 20µA	4, 10	4.6	–	–	V
Output Logic "0"					
at IOL = 20µA	4, 10	–	–	0.4	V
at IOL = 100µA	3, 4	–	–	0.4	V
at IOL = 360µA	4, 8, 9	–	–	0.4	V
Digital Input Current (V_{IN} = Logic "1" or "0")	2	–	–	1.0	µA
Leakage Current into IRQ "OFF" Output	5	–	–	4.0	µA
Digital Input Capacitance	2	–	–	7.5	pF
Analogue Impedance					
Input Impedance	13	–	500	–	kΩ
Output Impedance		–	1.5	–	kΩ
Dynamic Values					
Encoder					
Analogue Signal Input Levels	6	-24.0	–	4.0	dB
Passband	11, 12	–	3400	–	Hz
Decoder					
Analogue Signal Output Levels	6	-24.0	–	4.0	dB
Passband	11, 12	300	–	3400	Hz
Encoder/Decoder (Full Codec)					
Passband	11, 12	300		3400	Hz
Passband Gain	12	–	0	–	dB
Passband Ripple	12	-3.0	–	3.0	dB
Stopband		6.0	–	10	kHz
Stopband Attenuation		–	50.0	–	dB
SINAD Level (-6dB)		–	23.0	–	dB
Output Noise (Input short circuit)		–	-50	–	dBp
Idle Channel Noise (Forced)		–	-55	–	dBp
Xtal/clock Frequency	7	–	4.0	–	MHz

Notes

1. Does not include current drawn by any attached DRAM.
2. Serial Clock, Command Data, CS, A1/DEI and A2/DCK inputs.
3. CAS, WE and A0 to A9 outputs.
4. All measurements are made at 5.0 volts V_{DD}, any variations may alter parameters accordingly.
5. When the IRQ Output is at V_{DD}.
6. The optimum range of levels for a good Signal-to-Noise Ratio.
7. Audio frequency responses will vary with respect to Xtal/clock frequency.
8. Reply Data output.
9. IRQ output.
10. RAS Outputs.
11. Passband is reduced to (typically) 2700Hz when a sample rate of 25kb/s or 50kb/s is employed.
12. Measured with a -20dB input level to avoid codec slope-overload.
13. For optimum noise performance this input should be driven from a source impedance of less than 100Ω.

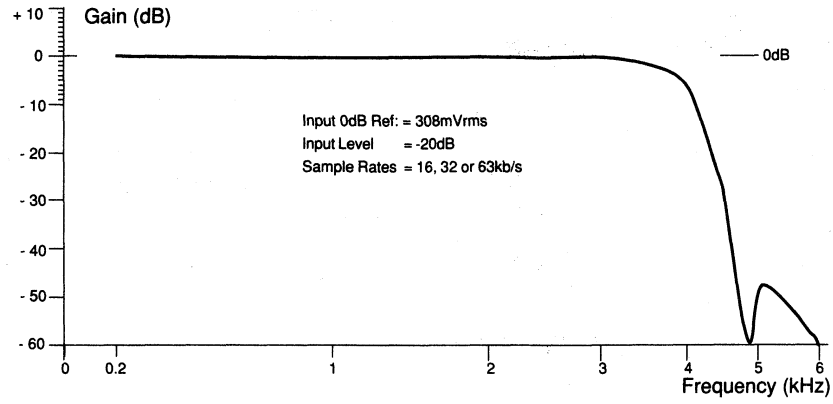


Fig.7 Typical Overall (Encoder + Decoder) Frequency Response

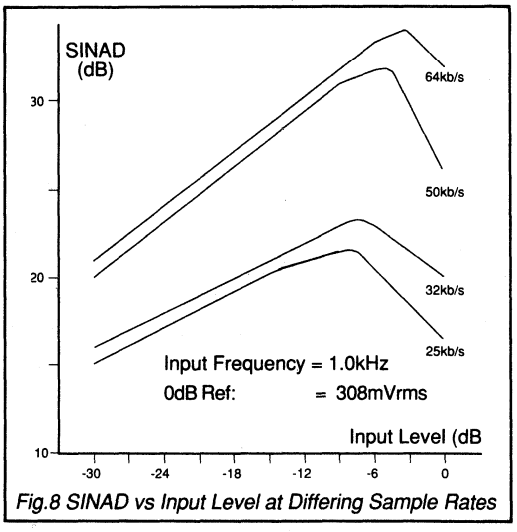


Fig.8 SINAD vs Input Level at Differing Sample Rates

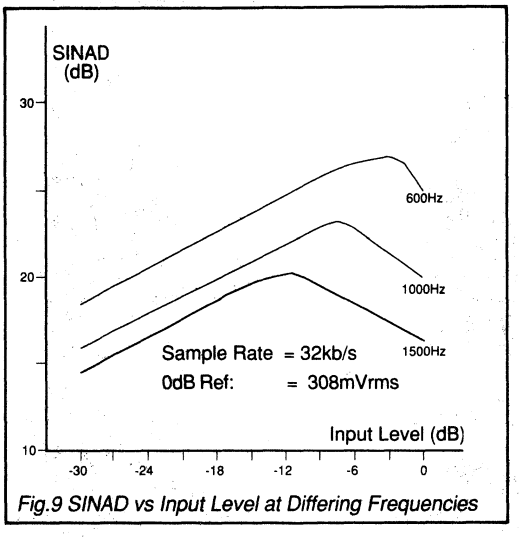


Fig.9 SINAD vs Input Level at Differing Frequencies

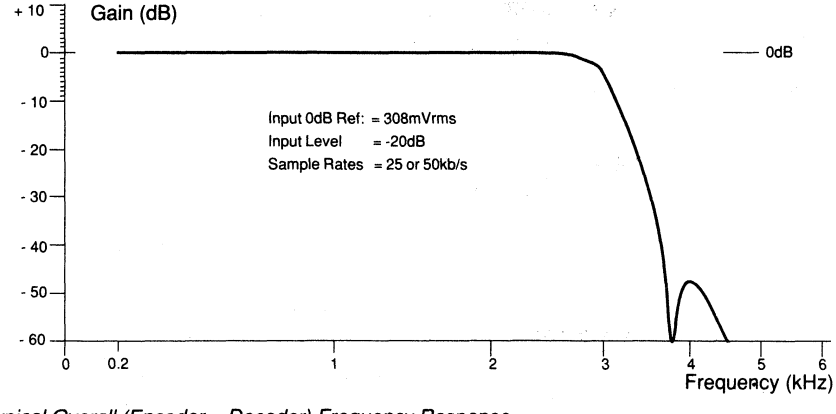


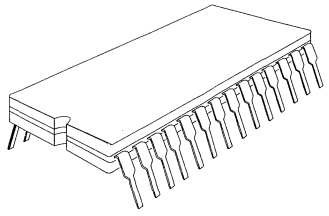
Fig.10 Typical Overall (Encoder + Decoder) Frequency Response

Package Outlines

The FX802 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX802J 28-pin cerdip DIL (J5)

NOT TO SCALE



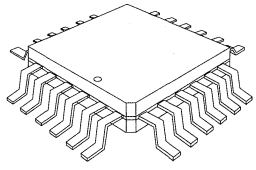
Max. Body Length 37.05mm
Max. Body Width 13.36mm

Handling Precautions

The FX802 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX802LG 24-pin quad plastic encapsulated bent and cropped (L1)

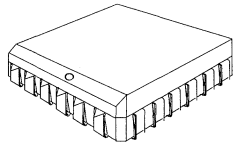
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX802LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX802J	28-pin cerdip DIL	(J5)
FX802LG	24-pin encapsulated bent and cropped	(L1)
FX802LS	24-lead plastic leaded chip carrier	(L2)

FX803 Audio Signalling Processor

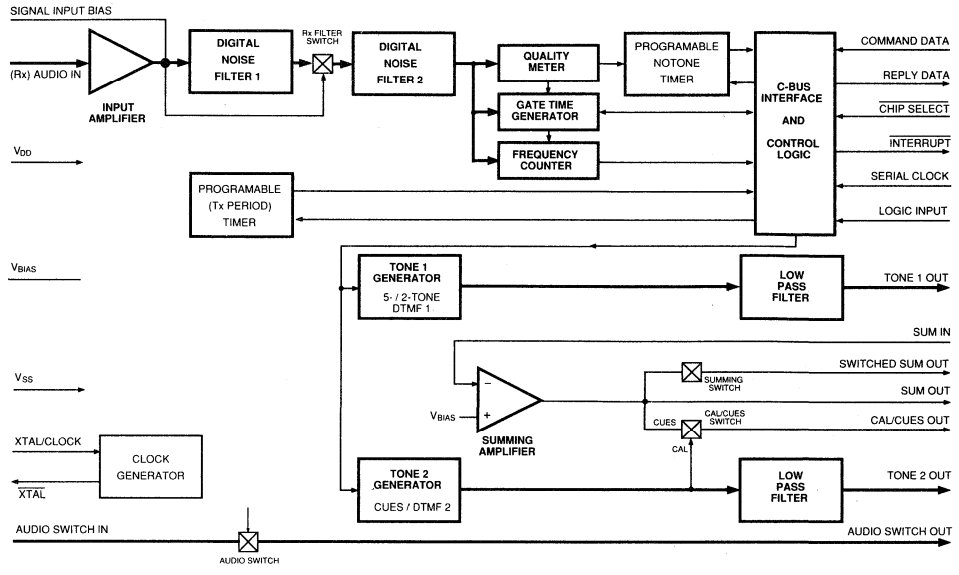


Fig.1 FX803 Audio Signalling Processor

FX803 Audio Signalling Processor

As part of the DBS 800 System, this audio signalling processor will provide an inband tone signalling facility for PMR radio systems. Signalling systems supported include Selcall (CCIR, ZVEI I, II and III, EEA), 2-Tone Selcall and Dual Tone Multi-Frequency (DTMF) encode.

Using a non-predictive tone decoder and versatile encoders gives the FX803 the capability to work in any standard or non-standard tone system.

This is a full-duplex device consisting of:

- Two individual tone generators and a programmable (Tx) period timer.
- A tone decoder with programmable NOTONE Timer.
- An on-chip summing amplifier.

For use with Single Tone or Selective Call systems.

Under the control of the µController, via "C-BUS," the FX803 will encode and transmit a single or pair of audio tones, in the frequency range 208Hz to 3kHz, simultaneously, and detect, decode and indicate the frequency of non-predicted input tones in the frequency range 313Hz to 6kHz.

Both tone generators can be individually placed into a power economical "Powersave" mode.

A general purpose logic input, interfacing directly with the Status Register, is provided. This could be used as an auxiliary method of routeing digital information to the µController via the "C-BUS."

The output frequencies are produced from data loaded to the device, with a programmable, general purpose, on-chip timer available to indicate the tone transmit periods.

A Dual Tone Multi-Frequency (DTMF) output is obtained by combining the 2 independent output frequencies in the integral summing amplifier. This Summing Amplifier output is also available for level adjustment.

Tones produced by the FX803 can also be used in the DBS 800 system as modulation calibration inputs and for "CUE" audio indications for the operator.

Received tones are measured and their frequency indicated to the µController in the form of a received data word. A poor-quality or incoherent tone will, after a programmed period, indicate NOTONE.

The FX803 is a low-power, 5-volt CMOS integrated circuit and is available in 24-pin DIL cerdip and 24-pin/lead plastic SMD packages.

Publication D/803/ 4 July 1994

Pin Number Function

FX803 J/LG/LS	
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this input when a Xtal input is used. See Figure 2.
2	**Xtal/Clock:** The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock (f_{XTAL}) should be connected here. See Figure 2.
3	**Reply Data:** The "C-BUS" serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high-impedance when not sending data to the µController. See Timing Diagrams.
4	**$\overline{\text{Chip Select}}$ ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the CS signal. See Timing Diagram.
5	**Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams.
6	**Logic Input:** This 'real-time' input is available as a general purpose logic input port which can be read from the Status Register. See Table 3.
7	**$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, allowing the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low-impedance pulldown to logic "0" when active and a high-impedance when inactive. The System IRQ line requires one pullup resistor to V_{DD}. The conditions that cause interrupts are indicated in the Status Register and are shown below: G/Purpose Timer Period Expired — NOTONE Timer Period Expired Rx Tone Measurement Complete These interrupts are inactive during relevant Powersave conditions and can be disabled by Bits 5 and 6 in the Control Register.
8	No internal connection, connect to V_{SS}.
9	No internal connection, connect to V_{SS}.
10	**Audio Switch In:** The input to the stand-alone, on-chip Audio Switch. This switching function (Control Register Bit 7) may be used to break the system transmitter modulation path when it is required to provide a CUE (beep) from Tone Generator 2 to the loudspeaker via the FX806 PLMR Audio Processor.
11	**Audio Switch Out:** The output of the stand-alone, on-chip Audio Switch.
12	**V_{SS}:** Negative Supply (Signal Ground).

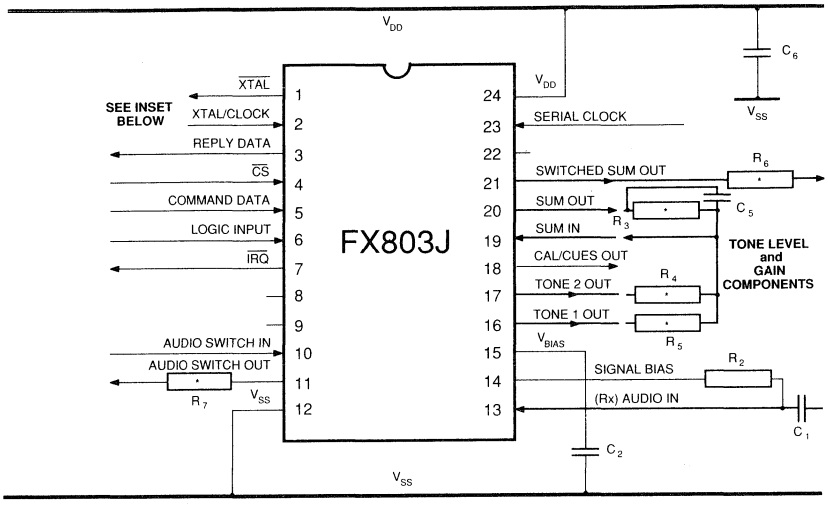
Pin Number Function

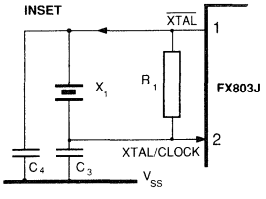
FX803 J/LG/LS	
13	**(Rx) Audio In:** The received audio tone signalling input to the Input Amplifier. This input requires to be a.c. coupled and connected, using external components, to the Signal Input Bias pin. See Figure 2.
14	**Signal Input Bias:** External components are required between this input and the (Rx) Audio In pin See Figure 2.
15	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS} by capacitor C_2 See Figure 2.
16	**Tone 1 Out:** Tone 1 Generator (2-/5- tone Selcall or DTMF 1) output. External gain and coupling components will be required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to Tx Tone Generator 1 Register (Table 4). See Figure 2.
17	**Tone 2 Out:** Tone 2 Generator (2-/5- tone Selcall, CUES or DTMF 2) output. External gain and coupling components will be required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to Tx Tone Generator 2 Register (Table 5). See Figure 2.
18	**CAL/CUES Out:** An auxiliary, selectable tone frequency output, providing a square wave CALibration signal from Tone 2 Generator or a sine wave CUES (beep) signal from the Summing Amplifier. The output mode (CAL or CUES) is selected by Bit 14 in the Tx Tone Generator 2 Register (Table 5). In a DBS 800 audio installation, this output should be connected to the Calibration Input of the FX806 PLMR Audio Processor. When Tone Generator 2 is set to V_{BIAS} (NOTONE), the CAL output is pulled to V_{BIAS} and during a powersave of Tone Generator 2 it is held at V_{SS}.
19	**Sum In:** The input to the on-chip Summing Amplifier. This amplifier is available for combining Tone 1 and Tone 2 outputs (DTMF). Gain and coupling components should be used at this input to provide the required system gains. See Figures 2 and 3.
20	**Sum Out:** The output of the on-chip Summing Amplifier. Combined tones (1 and 2) are available at this output. See Figures 2 and 3.
21	**Switched Sum Out:** The combined tone output available for transmitter modulation. The switch allows control of the FX803 final output to the FX806. Control of this switch is by Bit 4 of the Control Register. See Figures 2 and 3.
22	No internal connection, connect to V_{SS}.
23	**Serial Clock:** The "C-BUS" serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the Audio Signalling Processor. See Timing Diagrams.
24	**V_{DD}:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within the Audio Signalling Processor are dependent upon this supply.

NOTE: (i) Pins 8, 9 and 22 may be connected to V_{SS} to improve screening.
(ii) Further information on external components and DBS 800 system integration of this microcircuit are contained in the System Support Document, Document 2.
(iii) A glossary of abbreviations used in this document can be found on Page 14.

***"C-BUS"** is CML's proprietary standard for the transmission of commands and data between a µController and DBS 800 microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController.*

External Components





Component		Value			
R_1	=	1.0MΩ	C_1	=	0.1µF
R_2		2.0MΩ	C_2		1.0µF
*R_3		100kΩ	C_3		33.0pF
*R_4		82.0kΩ	C_4		33.0pF
*R_5		122kΩ	C_5		22.0pF
*R_6		100kΩ	C_6		1.0µF
*R_7		100kΩ	X_1	f_{XTAL}	4.032MHz

Tolerance: R = ± 10% C = ± 20%

Fig.2 Recommended External Components

Notes

1. Xtal/clock circuitry components shown INSET are recommended in accordance with CML Application Note D/XT/1 April 1986. The DBS 800 System Support Document contains additional notes on the use of Xtal/clock frequencies (f_{XTAL}).

2. It is recommended that, to improve screening and reduce noise levels around the FX803, Pins 8, 9 and 22 are connected to V_{SS}.

3. Resistors marked with an asterisk (*) are System Components, calculated to operate in a system with other DBS 800 microcircuits. Figure 3 shows in detail, these components used in the System signal paths.

   R_3, R_4, R_5, C_5 – Tone mixing components to provide a 3dB tone-differential (twist) when used in a DTMF configuration. Single tone output levels are set independently or by the FX806 Modulator Drivers.

   R_7 – Modulation level and matching for inputs to the FX806.

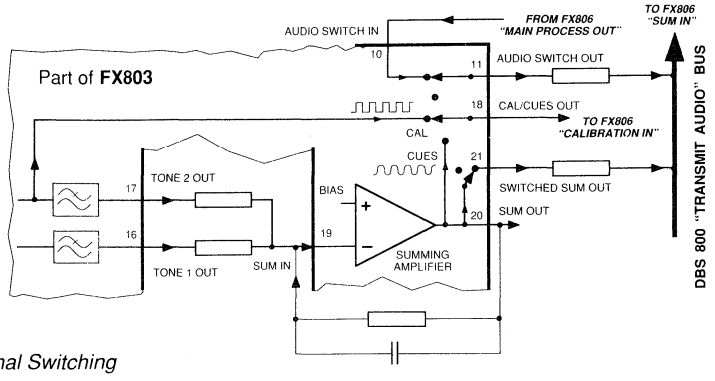


Fig.3 Output Signal Switching

Controlling Protocol

Control of the FX803 Audio Signalling Processor's operation is by communication between the µController and the FX803 internal registers on the "C-BUS," using Address/Commands (A/Cs) and appended instructions or data (see Figure 7). The use and content of these instructions is detailed in the following paragraphs and tables.

FX803 Internal Registers

FX803 internal registers are detailed below:

Control Register (30_H) – Write Only, control and configuration of the FX803.

Status Register (31_H) – Read Only, reporting of device functions.

Rx Tone Frequency Register (32_H) – Read Only, indicates frequency of the last received input.

Rx NOTONE Timer Register (33_H) – Write Only, setting of the Rx NOTONE period.

Tx Tone Generator 1 Register (34_H) – Write Only, setting the required output frequency from Tx Tone Generator 1.

Tx Tone Generator 2 Register (35_H) – Write Only, setting required output frequency from Tx Tone Generator 2.

General Purpose Timer Register (36_H) – Write Only, setting of a general purpose, sequential time period.

Address/Commands

The first byte of a loaded data sequence is always recognized by the "C-BUS" as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an Address/Command byte followed by either:

(i) further instructions or data or,

(ii) a Status or data Reply.

Instructions and data are loaded and transferred, via "C-BUS," in accordance with the timing information given in Figures 7 and 8.

Table 1 shows the list of A/C bytes relevant to the FX803. A complete list of DBS 800 "C-BUS" Address allocations is published in the System Support Document, Document 2.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB	+	Data Byte/s
General Reset	01	0 0 0 0 0 0 0 1		
Write to Control Register	30	0 0 1 1 0 0 0 0	+	1 byte Instruction to Control Register
Read Status Register	31	0 0 1 1 0 0 0 1	+	1 byte Reply from Status Register
Read Rx Tone Frequency	32	0 0 1 1 0 0 1 0	+	2 byte Reply from Rx Tone Register
Write to NOTONE Timer	33	0 0 1 1 0 0 1 1	+	1 byte Instruction to NOTONE Register
Write to Tx Tone Gen. 1	34	0 0 1 1 0 1 0 0	+	2 byte Instruction to Tx Tone Gen. 1
Write to Tx Tone Gen. 2	35	0 0 1 1 0 1 0 1	+	2 byte Instruction to Tx Tone Gen. 2
Write to G/Purpose Timer	36	0 0 1 1 0 1 1 0	+	1 byte Instruction to G/Purpose Timer

Table 1 "C-BUS" Address/Commands

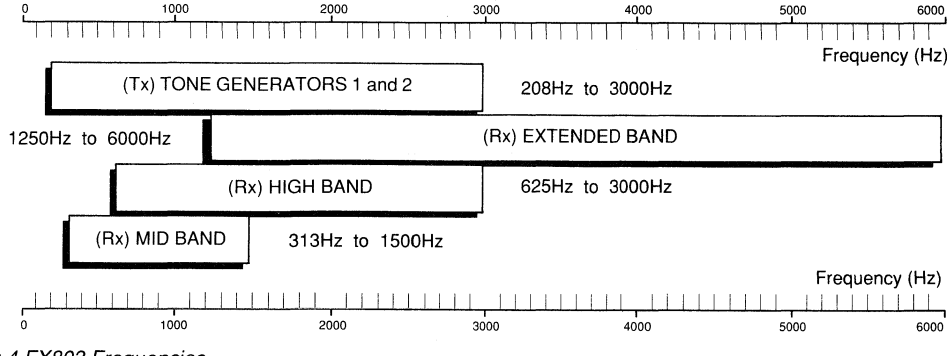


Fig.4 FX803 Frequencies

Controlling Protocol...

"Write to Control Register" – A/C 30_H, followed by 1 byte of Command Data.

Audio Switch

See the Signal Switching diagram (Figure 3) and DBS 800 Document 2 for application examples.

General Purpose Timer

Should be set up before interrupts are enabled, as a General Reset command will set the timer period to 00_H – 0ms (permanent interrupt). See Page 14, Operational Recommendations.

Interrupt Enable Instructions

Status Bits 0, 1 and 2 are produced regardless of the state of these settings.

Band Selection

Bits 2 and 3 set the required frequency range (see Figure 4, FX803 Frequencies).

Summing Switch

To break the FX803 drive to the FX806 PLMR Audio Processor (see Figure 3, Signal Switching).

Interrupt Designation

Decoder Interrupts:
No Tone Timer and Rx Tone Measurement.

Transmitter Interrupt:
G/Purpose Timer Interrupt.

Setting	*Control Bits*
MSB Bit 7	***Transmitted First***
1	**Audio Switch** Enable
0	Disable
6	
1	**G/Purpose Timer Interrupt** Enable
0	Disable
5	
1	**Decoder Interrupts** Enable
0	Disable
4	
1	**Summing Switch** Enable
0	Disable
3 ***2***	**Band Selection**
0 0	High Band
0 1	Mid Band
1 0	Extended Band
1 1	Do Not use this setting
1	Set to "0"
0	
0	Set to "0"
0	

Table 2 Control Register

"Read Status Register" – A/C 31_H, followed by 1 byte of Reply Data.

Reading	*Status Bits*
MSB Bit 7	***Received First***
0	Set to "0"
6	
0	Set to "0"
5	
0	Set to "0"
4	
0	Set to "0"
3	**Logic Input Status**
1	"1"
0	"0"
2	**G/Purpose Timer Period**
1	Expired (IRQ generated if enabled) *(Table 2)*
1	**NOTONE Timer Period**
1	Expired (IRQ generated if enabled) *(Table 2)*
0	**Rx Tone Measurement**
1	Complete (Interrupt Generated)

Table 3 Status Register

Interrupt Requests ($\overline{IRQ}$)

Interrupts on this device are available to draw the attention of the µController to a change in the condition of the bit in the Status Register. However Bits are set in the Status Register irrespective of the setting of interrupt enable bits (Table 2) and these changes may be recognized by 'polling' the register.

General Purpose Timer Period

Set to a logic "1" when the timer period has expired.
Cleared to a logic "0,"

i By a read of the Status Register or,
ii New G/Purpose Timer information or,
iii General Reset Command

NOTONE Timer Period

Set to a logic "1" when the timer period has expired.
Cleared to a logic "0,"

i By a read of the Status Register or,
ii New NOTONE Timer information or,
iii General Reset Command

Rx Tone Measurement

Set to a logic "1" when the Rx Tone measurement is complete.
Cleared to a logic "0,"

i By a read of the Status Register or,
ii General Reset Command

Tx Tone Generator Registers 1 and 2

Each Tx Tone Generator is controlled individually by writing a two-byte command to the relevant Tx Tone Generator Register. The format of this command word, which is different for each tone generator, is shown below with the calculations required for tone frequency (f_{TONE}) generation described in the following text.

"Write to Tx Tone Generator 1 Register" – A/C 34_H followed by 2 bytes of Command Data.

MSB (loaded first)			Bit Numbers												LSB (loaded last)
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
"0"	"0"	V_{BIAS}/ Enable	These 13 bits (0 to 12) are used to produce a binary number, designated "**A**." "**A**" is used in the formulas below to set the Tx Tone 1 frequency (f_{TONE} 1).												

The binary number produced by bits 0 to 12 (MSB) is designated "A."
If "A" = all logic "0" then Tx Tone Generator 1 is Powersaved.

Bit 13 at logic "1" = Tone 1 Output at V_{BIAS} (NOTONE).
"0" = Tone 1 Output Enabled.
Bits 14 and 15 (MSB) must be logic "0."

Table 4 Setting Tx Tone Generator 1

"Write to Tx Tone Generator 2 Register" – A/C 35_H followed by 2 bytes of Command Data.

MSB (loaded first)			Bit Numbers												LSB (loaded last)
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
"0"	CAL/ CUES	V_{BIAS}/ Enable	These 13 bits (0 to 12) are used to produce a binary number, designated "**B**." "**B**" is used in the formulas below to set the Tx Tone 2 frequency (f_{TONE} 2).												

The binary number produced by bits 0 to 12 (MSB) is designated "B."
If "B" = all logic "0" then Tx Tone Generator 2 is Powersaved.

Bit 13 at logic "1" = Tone 1 Output at V_{BIAS} (NOTONE).
"0" = Tone 1 Output Enabled.
Bit 14 at logic "1" = Squarewave CAL Output.
"0" = Sinewave CUES Output.
Bit 15 (MSB) must be a logic "0."

Table 5 Setting Tx Tone Generator 2

Notes

(1) Programming Tone Generator 2 to V_{BIAS} (NOTONE) (Bit 13) will place the CAL/CUES Output at V_{BIAS} via a 40kΩ internal resistor.
(2) Programming Tone Generator 2 to Powersave will place the CAL/CUES Output at V_{SS}.
(3) If both Tone Generators (1 and 2) are Powersaved, the Summing Amplifier is also Powersaved.

Calculations

As can be seen from Tables 4 and 5 (above), a binary number ("A" or "B" – Bits 0 to 12) is loaded to the respective Tx Tone Generator. The formulas shown below are used to calculate the required output frequency.

Required Tx Tone output frequency	=	f_{TONE} 1 or 2
XTAL/clock frequency	=	f_{XTAL}
Input Data Word (Bits 0 to 12)	=	"A" or "B"

Formula

$$f_{TONE\ (Hz)} = \frac{f_{XTAL\ (Hz)}}{4 \times \text{"A" (or "B")}} \quad \textit{or} \quad \text{Input "A" (or "B")} = \frac{f_{XTAL\ (Hz)}}{4 \times f_{TONE\ (Hz)}}$$

Tx Tone Frequencies

With reference to Tables 4 and 5 (above), whilst Input Data Words "A" or "B" can be programmed for frequencies outside the stated limits of 208Hz and 3000Hz, any output frequencies obtained may not be within specified parameters (see "Specification" page).

"Read Rx Tone Frequency Register" – A/C 32_H, followed by 2 bytes of Reply Data.

Measurement of Rx Signal Frequency (S_{INPUT})

The measurement details given are for a Xtal/clock frequency (f_{XTAL}) of 4.032MHz, a scaling formula for other values of f_{XTAL} is given at the bottom of page 10.

The input audio signal (S_{INPUT}) is filtered and measured in the Frequency Counter over a specified "measurement period" (9.125 ms or 18.250 ms).

The measuring function counts the number of complete input cycles occurring within the measurement period and then the number of measuring-clock cycles necessary to make up the period.

When the count period of a successful decode is complete, the Rx Tone Measurement bit in the Status Register, and the Interrupt bit (if enabled) are set.

The Rx Tone Frequency Register will now indicate the signal frequency (S_{INPUT}) in the form of 2 bytes (1 and 0) as illustrated in Figure 6 below.

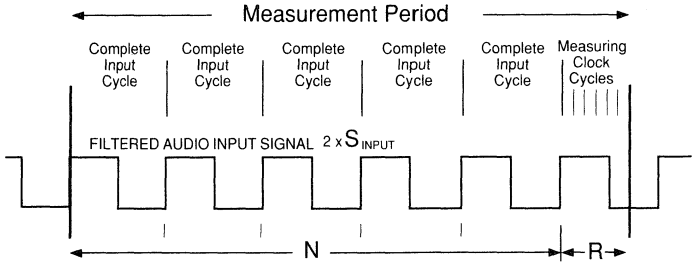


Fig.5 Measurement of a Mid or High Band Rx Frequency

The Integer (N) – Byte 1

A binary number representing *'twice the number of complete input audio cycle periods'* counted during the specified measurement period, which is:

High Band Decode	=	9.125 ms	=	"t"
Mid Band Decode	=	18.250 ms	=	"t"
Extended Band Decode	=	9.125 ms	=	"t"

See the bottom of this page for "t" and "f" scaling factors

The Remainder (R) – Byte 0

A binary number representing the remainder part, R, of 2 x Input Signal Frequency (S_{INPUT}). *'R = number of specified measuring-clock cycles'* required to complete the specified measurement period (See N).

The clock-cycle frequencies are:

High Band Decode	=	56.00 kHz	=	"f"
Mid Band Decode	=	28.00 kHz	=	"f"
Extended Band Decode	=	56.00 kHz	=	"f"

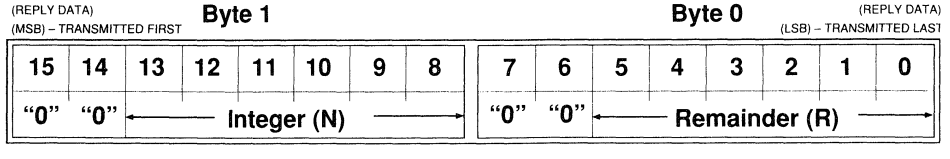


Fig.6 Format of the Rx Tone Frequency Register

f_{XTAL} Scaling Factors

The calculations above are for an f_{XTAL} of 4.032MHz. The following formulas enable the calculation of these values using any Xtal value. Note: f_{XTAL} values are stated in MHz.

$$"t"_{scaled} = "t" \times \left[\frac{4.032}{f_{XTAL}}\right]$$

$$"f"_{scaled} = "f" \times \left[\frac{f_{XTAL}}{4.032}\right]$$

Frequency Measurement Formulæ

To assist in the production of 'look-up' tables and limit-values in the µController and provide guidance upon the determination of N and R from a measured frequency, the following formulæ show the derivation of the Rx frequency, S_{INPUT}, from the measured data bytes (N and R), Figure 6.

High Band Measurement

S_{INPUT} – High Band

In the measurement period of 9.125ms, there are Nh cycles at $2S_{INPUT}$ and Rh clock cycles at 56.000kHz.

$$\text{so} \quad \frac{Nh}{2 \times S_{INPUT}} + \frac{Rh}{56000} = 9.125\text{ms}$$

$$\text{From which } S_{INPUT} = \frac{28000 \times Nh}{(511 - Rh)} \text{ Hz} \qquad [1]$$

Nh and Rh – High Band

The measurement period = 9.125ms
Clock Frequency = 56.000kHz
The measured frequency = $2 \times S_{INPUT}$ c/s
In the measurement period there are:
$2 \times S_{INPUT} \times 9.125 \times 10^{-3}$ cycles

Nh is the lower integer value of this decimal number:

$$Nh = \text{INT}(9.125 \times 10^{-3} \times 2 \times S_{INPUT}) \qquad [4]$$

Rh is rounded to the nearest integer of this decimal number:

$$Rh = (9.125 \times 10^{-3} - \frac{Nh}{2 \times S_{INPUT}}) \times 56000 \qquad [5]$$

Mid Band Measurements

S_{INPUT} – Mid Band

In the measurement period of 18.250ms, there are Nm cycles at $2S_{INPUT}$ and Rm clock cycles at 28.000kHz.

$$\text{so} \quad \frac{Nm}{2 \times S_{INPUT}} + \frac{Rm}{28000} = 18.250\text{ms}$$

$$\text{From which } S_{INPUT} = \frac{14000 \times Nm}{(511 - Rm)} \text{ Hz} \qquad [2]$$

Nm and Rm – Mid Band

The measurement period = 18.250ms
Clock Frequency = 28.000kHz
The measured frequency = $2 \times S_{INPUT}$ c/s
In the measurement period there are:
$2 \times S_{INPUT} \times 18.250 \times 10^{-3}$ cycles

Nm is the lower integer value of this decimal number:

$$Nm = \text{INT}(18.250 \times 10^{-3} \times 2 \times S_{INPUT}) \qquad [6]$$

Rm is rounded to the nearest integer of this decimal number:

$$Rm = (18.250 \times 10^{-3} - \frac{Nm}{2 \times S_{INPUT}}) \times 28000 \qquad [7]$$

Extended Band Measurements

S_{INPUT} – Extended Band

In the measurement period of 9.125ms, there are Ne cycles at S_{INPUT} and Re clock cycles at 56.000kHz.

$$\text{so} \quad \frac{Ne}{S_{INPUT}} + \frac{Re}{56000} = 9.125\text{ms}$$

$$\text{From which } S_{INPUT} = \frac{56000 \times Ne}{(511 - Re)} \text{ Hz} \qquad [3]$$

Ne and Re – Extended Band

The measurement period = 9.125ms
Clock Frequency = 56.000kHz
The measured frequency = S_{INPUT} c/s
In the measurement period there are:
$S_{INPUT} \times 9.125 \times 10^{-3}$ cycles

Ne is the lower integer value of this decimal number:

$$Ne = \text{INT}(9.125 \times 10^{-3} \times S_{INPUT}) \qquad [8]$$

Re is rounded to the nearest integer of this decimal number:

$$Re = (9.125 \times 10^{-3} - \frac{Ne}{S_{INPUT}}) \times 56000 \qquad [9]$$

"Write to the Rx NOTONE Timer Register" – A/C 33_H followed by 1 byte of Command Data.

Setting				Function/Period		
MSB						
7	6	5	4	Transmitted Bit 7 First		
0	0	0	0	These 4 bits must be "0"		
3	2	1	0		High/Extended Band	Mid Band
0	0	0	0	period (ms)	0	0
0	0	0	1	"	20 ±1%	40 ±1%
0	0	1	0		40 "	80 "
0	0	1	1		60 "	120 "
0	1	0	0		80 "	160 "
0	1	0	1		100 "	200 "
0	1	1	0		120 "	240 "
0	1	1	1		140 "	280 "
1	0	0	0		160 "	320 "
1	0	0	1		180 "	360 "
1	0	1	0		200 "	400 "
1	0	1	1		220 "	440 "
1	1	0	0		240 "	480 "
1	1	0	1		260 "	520 "
1	1	1	0		280 "	560 "
1	1	1	1		300 "	600 "

Table 6 Rx NOTONE Timer Settings

Operation of the Rx NOTONE Timer

An Rx NOTONE period is that period when no signal or a consistently bad-quality signal is received.

The Rx NOTONE Timer can be employed to indicate to the µController that a NOTONE situation has existed for a predetermined period.

This timer register can be written-to and set in any mode of the FX803.

The NOTONE Timer period is 'primed' by writing to the NOTONE Timer Register (33_H) using the settings given in Table 6.

"Priming" sets the timing period; ***this period can only start directly after a frequency (tone) measurement has been successfully completed.***

The NOTONE Timer is a one-shot timer being reset only by successful tone measurements.

If the quality of the received signal drops to an unusable level the NOTONE Timer will start its run-down.

On completion of the preset period, the NOTONE Timer Period Expired bit in the Status Register and the Interrupt (when enabled, *Table 2*) are set.

Upon detection of the Interrupt, the Status Register should be read by the µController to ascertain the source of the Interrupt.

The NOTONE Timer Period Expired bit is cleared:

i By a read of the Status Register or,
ii New NOTONE Timer information or,
iii General Reset command

This timer is set to 00_H (0ms) by a General Reset command.

The following situations may be encountered by the NOTONE Timer circuitry:

No Signal

The NOTONE Timer can only start its run down on completion of a valid frequency measurement.

No Signal after a Valid Tone Measurement

The timer will start to run down when the last Rx Tone Measurement complete bit is set. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

Signal Fades after a Valid Tone Measurement

The timer will start to run down when the signal becomes unreadable to the device. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

Signal Appears after the Timer has Started

If the frequency measurement is more than 75% complete when the timer period expires, neither the NOTONE bit nor the Interrupt will be set unless that frequency measurement is subsequently aborted.

"Write to General Purpose Timer Register" – A/C 36_H followed by 1 byte of Command Data.

Setting				*Function/Period*			
MSB							
7	*6*	*5*	*4*	***Transmitted Bit 7 First***			
0	0	0	0	These 4 bits must be "0"			
3	*2*	*1*	*0*	**High/Extended Band**		**Mid Band**	
				Reset Timer and Start Timing			
0	0	0	0	Period of	0		0
0	0	0	1	"	10 ms	±1%	20 ms ±1%
0	0	1	0		20	"	40 "
0	0	1	1		30	"	60 "
0	1	0	0		40	"	80 "
0	1	0	1		50	"	100 "
0	1	1	0		60	"	120 "
0	1	1	1		70	"	140 "
1	0	0	0		80	"	160 "
1	0	0	1		90	"	180 "
1	0	1	0		100	"	200 "
1	0	1	1		110	"	220 "
1	1	0	0		120	"	240 "
1	1	0	1		130	"	260 "
1	1	1	0		140	"	280 "
1	1	1	1		150	"	300 "

Table 7 General Purpose Timer Settings

Operation of the General Purpose Timer

This timer, which is not dedicated to any specific function within the FX803, can be employed within the DBS 800 system to indicate time-elapsed periods of between 10ms and 150ms in the High/Extended Band, 20ms and 300ms in the Mid Band, to the µController.

Setting of the timer is by loading a single-byte data word via the "C-BUS," as indicated in Table 7 (left), to the FX803 via the Command Data line.

The timer will be reset and the run-down started on completion of Timer Data Word loading.

When the programmed time period has expired, the General Purpose Timer Expired bit (Bit 2) in the Status Register and the Interrupt (if enabled) are set.

The General Purpose Timer Expired bit is cleared:

i By a read of the Status Register, or
ii New G/P Timer information, or
iii General Reset command.

When the programmed time period has expired, this timer will reset, restart and continue sequencing until;

i New G/P Timer information is written, or
ii A General Reset command.

The General Purpose Timer Expired bit and the Interrupt will remain set until cleared.

This timer is set to 00_H (0ms) by a General Reset command.

Powersave

Various sections of the FX803 can be placed independently into a power economical condition. Table 8 (below) gives a brief summary of the inactive, power-economical states available to the FX803.

Powersaved Section	Instruction Source		Table
Tone Encoder 1	Tx Tone Gen.1 Reg. (34_H)	All bits = "0"	4
Tone Encoder 2	Tx Tone Gen.2 Reg. (35_H)	All bits = "0"	5
Summing Amplifier	This action is automatic when both Tone Encoders are in the powersave condition.		

Table 8 FX803 Powersave Functions

Powersave Conditions

Xtal/Clock and "C-BUS": This circuitry is always active, on all DBS 800 microcircuits, under any powered/powersaved conditions.

Interrupt Requests

An Interrupt (IRQ), when enabled, is provided by the FX803 to indicate the following conditions to the µController.

NOTONE Timer Period Expired

Enabled: By Control Register Bit 5.

Set: When the preset Notone Flag is set.

Identified: By Status Register Bit 1.

Cleared: By reading the Status Register.

G/Purpose Timer Period Expired

Enabled: By Control Register Bit 6.

Set: When the General Purpose Timer has timed out.

Identified: By Status Register Bit 2.

Cleared: By reading the Status Register.

Rx Tone Measurement Complete

Enabled: By Control Register Bit 5.

Set: When an Rx Frequency Measurement has been successfully completed.

Identified: By Status Register Bit 0.

Cleared: By reading the Status Register.

On recognition of the "Read Status" Command byte, the interrupt output is cleared, the Status Bits are transferred to the µController via the "C-BUS" Reply Data line and the internal Status Bits are cleared.

Operational Recommendations

It is recommended that, following initial System power-up a General Reset command is sent to the FX803.

Receive Sequence

1. Send Control Command for Rx:
   Select Midband/Highband and Digital Filter length.
2. Disable transmitters, if desired by writing to Tone Frequency registers.
3. Prime the NOTONE Timer by sending the required period byte.
4. Enable Decoder interrupts as desired.
5. When a valid tone has been detected by a successfully completed measurement the Status Register is set to "Tone Measurement Complete" and an interrupt sent to the µC.
6. The µC examines the Status Register, if tone measurement is complete, reads in the Rx Tone Frequency in the form N + R (Figure 6).
7. Rx Tone Measurement Complete interrupts are periodically sent to the µC unless NOTONE is detected, in which case a NOTONE Interrupt is sent.

Transmit Control Sequence

1. Set Tone Frequency Generators to V_{BIAS} (setting both tone generators (Bit 13 = "1")) during the transmitter initialization period.
2. Send Control Command for Tx:
   Select Sum/Switched Sum o/p and Audio Switch states.
3. Send General Purpose (GP) Timer information for the V_{BIAS} (NOTONE) transmitter initialization period (Step 1). This will initiate the timer.
4. Enable the General Purpose Timer interrupt.
5. µC waits for "GP Timer Expired;" Reads the Status Register to check interrupt due to timer; Resets the Status Bit.
   If required, the µC sends the next timer period followed by the next tone(s) frequency information.
   A new timer period sent will reset the timer, otherwise the timer is self-sequencing.
6. The µC monitors the interrupts and repeats 5 & 6 as required.
7. After last loaded tone the µC turns off the Tone Generator(s) by setting tone outputs to V_{BIAS} (NOTONE) (Tables 4 and 5).

General Reset

Upon Power-Up the "bits" in the FX803 registers will be random (either "0" or "1"). A General Reset Command (01_H) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX803.

Control Reg.	Set as 00_H
Status Reg. Bits 0, 1, 2.)	Set as 00_H
NOTONE Timer Reg.	Set as 00_H
Tone Gen. 1 Reg. (2 bytes)	Set as 0000_H
Tone Gen. 2 Reg. (2 bytes)	Set as 0000_H
Gen/Purpose Reg.	Set as 00_H

Sets the FX803 to:
Encoder High Band (625Hz to 3000Hz) – with interrupts disabled, both timers set to 00_H.

It is recommended that both timers are set-up before interrupts are enabled, to prevent initial, undesired interrupts.

Glossary of Abbreviations

Below is a list of abbreviations used within this Data Sheet.

f_{XTAL}	Xtal/clock frequency
S_{INPUT}	Audio input signal
f_{TONE}	Tone frequency

Timing Information

Timing Diagrams

Figure 7 shows the timing parameters for two-way communication between the µController and the FX803 on the "C-BUS." Figure 8 shows, in detail, the timing relationships for "C-BUS" information transfer.

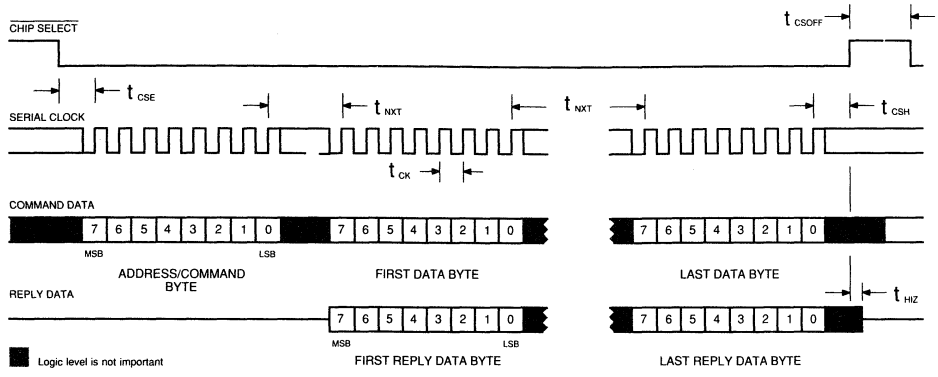


Fig.7 "C-BUS" Timing Information *NOT TO SCALE*

Parameter	Min.	Typ.	Max.	Unit
t_{CSE}	2.0	–	–	µs
t_{CSH}	4.0	–	–	µs
t_{CSOFF}	2.0	–	–	µs
t_{NXT}	4.0	–	–	µs
t_{CK}	2.0	–	–	µs
t_{CH}	500	–	–	ns
t_{CL}	500	–	–	ns
t_{CDS}	250	–	–	ns
t_{CDH}	0	–	–	ns
t_{RDS}	250	–	–	ns
t_{RDH}	50.0	–	–	ns
t_{HIZ}	–	–	2.0	µs

Notes

(1) Command Data is transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. Reply Data is read from the FX803 MSB (Bit 7) first, LSB (Bit 0) last.
(2) Data is clocked into the FX803 and into the µController on the rising Serial Clock edge.
(3) Loaded data instructions are acted upon at the end of each individual, loaded byte.
(4) To allow for differing µController serial interface formats, the FX803 will work with either polarity Serial Clock pulses.

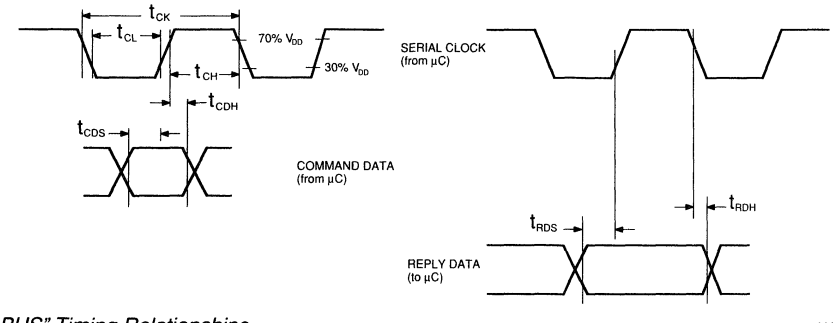


Fig.8 "C-BUS" Timing Relationships *NOT TO SCALE*

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX803J**	-40°C to +85°C (cerdip)
	FX803LG/LS	-40°C to +85°C (plastic)
Storage temperature range:	**FX803J**	-55°C to +125°C (cerdip)
	FX803LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock (f_{XTAL}) = 4.032MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz *(60% deviation, FM).*

Noise Bandwidth = 5.0kHz Band-Limited Gaussian.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
(Decoder + Both Timers)		–	2.0	–	mA
(Decoder + Both Timers + One Tx only)		–	4.0	–	mA
(All Functions Enabled)		–	5.0	–	mA
Analogue Impedances					
(Rx) Audio Input		–	20.0	–	MΩ
Summing Amp Input		–	20.0	–	MΩ
Switch		–	1.0	–	kΩ
Tones 1 and 2 Outputs		–	10.0	–	kΩ
CAL/CUES Output		–	5.0	–	kΩ
Summing Outputs		–	10.0	–	kΩ
Dynamic Values					
Digital Interface					
Input Logic "1"	1	3.5	–	–	V
Input Logic "0"	1	–	–	1.5	V
Output Logic "1" (IOH = -120µA)	2	4.6	–	–	V
Output Logic "0" (IOL = 360µA)	3	–	–	0.4	V
I_{OUT} Tristate (Logic "1" or "0")	3	–	–	4.0	µA
Input Capacitance	1	–	–	7.5	pF
IOX (V_{OUT} = 5.0V)	4	–	–	4.0	µA
Overall Performance					
Rx – Decoding					
High-Band					
Sensitivity		–	-20.0	–	dB
Tone Response Time					
Good Signal	5	–	–	30.0	ms
Tone-to-Noise Ratio = 0dB	5, 6	–	–	40.0	ms
Frequency					
Band		625		3000	Hz
Measurement Resolution		–	0.2	–	%
Measurement Accuracy	9	–	0.5	–	%

Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
Rx – Decoding					
Mid-Band					
Sensitivity		–	-20.0	–	dB
Tone Response Time					
Good Signal	7	–	–	60.0	ms
Tone-to-Noise Ratio = 0dB	6, 7	–	–	80.0	ms
Frequency					
Band		313		1500	Hz
Measurement Resolution		–	0.2	–	%
Measurement Accuracy	9	–	0.5	–	%
Extended-Band					
Sensitivity		–	-20.0	–	dB
Tone Response Time					
Good Signal	5	–	–	20.0	ms
Frequency					
Band		1250		6000	Hz
Measurement Resolution		–	0.2	–	%
Measurement Accuracy	9	–	0.5	–	%
Tx – Encoders 1 and 2					
Tone Frequency		208		3000	Hz
Period ($1/f_{TONE}$) Error		–	–	1.0	µs
Tone Amplitude		-1.5	–	1.5	dB
Total Harmonic Distortion		–	–	5.0	%
Rise Time to 90%		–	$3/f_{TONE}$	–	secs
Fall Time to 10%	8	–	–	5.0	ms
Frequency Change Time		–	$3/f_{TONE}$	–	secs
Timers					
General Purpose					
Timing Period Range					
High-Band		10.0		150	ms
Mid-Band		20.0		300	ms
Rx NOTONE					
Timing Period Range					
High-Band		20.0		300	ms
Mid-Band		40.0		600	ms
Xtal/Clock Frequency (f_{XTAL})	10	3.9	–	6.0	MHz

Notes

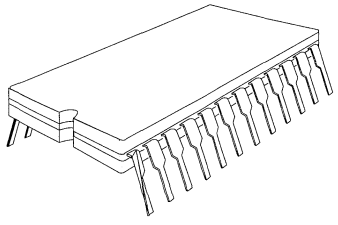
1. Device control pins; Serial Clock, Command Data, and $\overline{CS}$.
2. Reply Data output.
3. Reply Data and $\overline{IRQ}$ outputs.
4. Leakage current into the "Off" $\overline{IRQ}$ output.
5. Measurement Period = 9.125ms.
6. Decode Probability = 0.993.
7. Measurement Period = 18.250ms.
8. When set to Powersave.
9. For a good input signal.
10. The use of the FX803 at Xtal/clock frequencies above 4.0MHz will cause a shift in the overall performance parameters.

Package Outlines

The FX803 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX803J 24-pin cerdip DIL (J4)

NOT TO SCALE



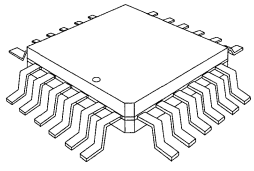
Max. Body Length 32.03mm
Max. Body Width 14.81mm

Handling Precautions

The FX803 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX803LG 24-pin quad plastic encapsulated bent and cropped (L1)

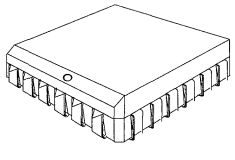
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX803LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX803J	24-pin cerdip DIL	(J4)
FX803LG	24-pin encapsulated bent and cropped	(L1)
FX803LS	24-lead plastic leaded chip carrier	(L2)

FX805 Sub-Audio Signalling Processor

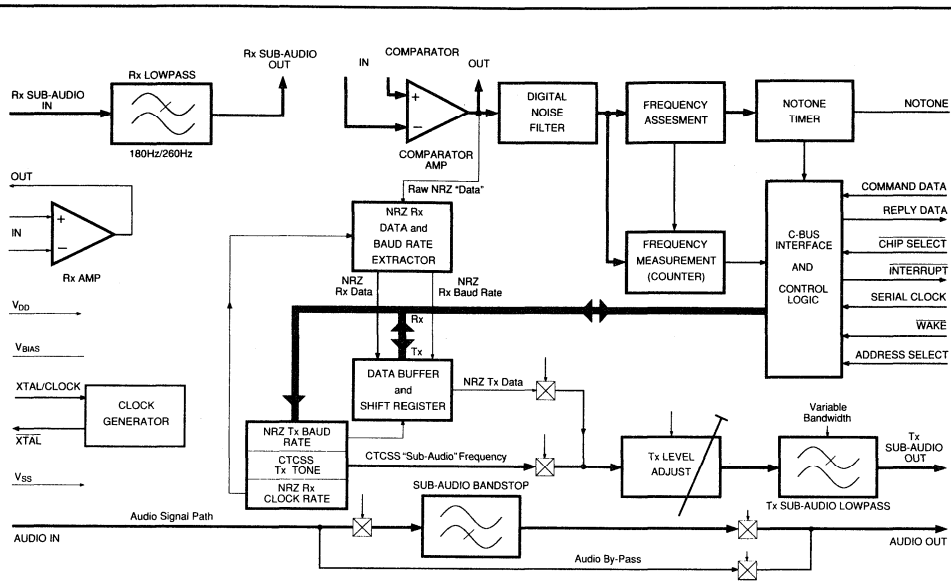


Fig.1 FX805 Sub-Audio Signalling Processor

FX805 Sub-Audio Signalling Processor

A µProcessor controlled, sub-audio frequency signalling processor to provide an outband audio and digital signalling facility for PMR radio systems.

This device caters for the transmission and non-predictive reception of:

- *Continuous Tone Controlled Squelch (CTCSS) tones and other non-standard sub-audio frequencies.*
- *Non-Return-to-Zero (NRZ) data to facilitate Continuous Digitally Coded Squelch (CDCS/DPL™) system operations.*

To achieve these functions, the FX805 has on-chip:

- *A non-predictive CTCSS Tone Decoder and CDCS sub-audio signal demodulator.*
- *A CTCSS/NRZ Encoder with Tx level adjustment and lowpass filter output stage with optional NRZ pre-emphasis.*
- *A selectable sub-audio bandstop filter.*
- *A Notone (CTCSS Rx) period timer.*

Setting of the FX805 functions and modes is by data loaded from the µController to the controlling registers within the device. Reply Data and Interrupt protocol keep the µController up to date on the operational status of the circuitry — all via the "C-BUS" interface.

CTCSS tone data for transmission is generated within the µController, loaded to CTCSS Tx Frequency Register, encoded and output as a tone via the Tx Sub-Audio Lowpass Filter.

Received non-predicted CTCSS tone frequencies are measured and the resulting data, in the form of a 2-byte data-word, is presented via the CTCSS Rx Frequency Register to the µController for matching against a 'look-up' table. Noise filtering is provided to improve the signal quality prior to measurement.

NRZ coded data streams for transmission, when generated within a µController, are loaded to the NRZ Tx Data Buffer and output, in 8-bit bytes, through the Lowpass Filter circuitry as sub-audio signals. CDCS turn-off tones can be added to the data signals by switching the FX805 to the CTCSS transmit mode at the appropriate time.

NRZ coding is produced by the µController and translated into sub-audio signals by the FX805.

Received NRZ data is filtered, detected and placed into the NRZ Rx Data Register which is then available for transfer one byte at a time, to the µController, for decoding by software. Clock extraction circuitry is provided on chip and Rx and Tx baud rates are selectable.

Provision is made in both hardware and system software allocations to address two FX805 Sub-Audio Signalling Processors consecutively to achieve multi-mode, duplex operation.

The FX805 has a powersaving function which may be controlled by software or a dedicated (Wake) input.

The FX805 is a low-power, 5-volt CMOS integrated circuit and is available in 24-pin DIL cerdip and 24-pin/lead plastic SMD packages.

Publication D/805/3 July 1994

Pin Number Function

FX805 J/LG/LS	
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this input when a Xtal (f_{XTAL}) input is used. See Figure 2.
2	**Xtal/Clock:** The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock (f_{XTAL}) should be connected here. See Figure 2.
3	**Address Select:** This pin enables two FX805 devices to be used on the same "C-BUS," providing full-duplex operation. See Tables 1 and 2.
4	**Interrupt Request ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, allowing the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low impedance pulldown to logic "0" when active and a high impedance when inactive. The System IRQ line requires 1 pullup resistor to V_{DD}. The conditions that cause interrupts are indicated in the Status Register (Table 4) and are shown below: *Rx CTCSS Tone Measurement Complete* *1 NRZ Rx Data Byte Received* *NRZ Tx Buffer Ready* *CTCSS NOTONE Timer Expired* *New NRZ Rx Data Received Before Last Byte Read* *NRZ Data Transmission Complete*
5	**Serial Clock:** The "C-BUS" serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the Sub-Audio Signalling Processor. See Timing Diagrams.
6	**Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams.
7	**Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the CS signal. See Timing Diagrams.
8	**Reply Data:** The "C-BUS" serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the µController. See Timing Diagrams.
9	**Tx Sub-Audio Out:** The sub-audio output (pure or NRZ derived). Signals are band-limited, the Tx Output Filter has a variable bandwidth, see Table 6. This output is at V_{BIAS} (a) when the NRZ Encoder is enabled but no data is being transmitted, (b) when the FX805 is placed in the Powersave All condition.
10	**Audio In:** The input to the switched sub-audio bandstop (highpass) filter. This input is internally biased and requires to be a.c. coupled by capacitor C_7.
11	**Audio Out:** The output of the 'audio signal path' (filter or by-pass). This output is controlled by the Control Register and when disabled is held at $V_{DD}/2$.
12	**V_{SS}:** Negative Supply (Signal Ground).

Pin Number Function

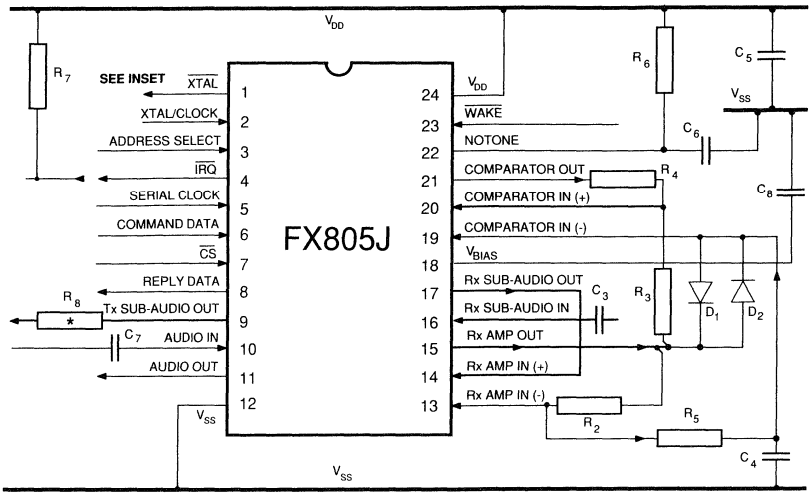
FX805 J/LG/LS	
13	**Rx Amp (-) In:** The inverting input to the on-chip Rx Input Amp. See Figures 2, 3 and 4.
14	**Rx Amp (+) In:** The non-inverting input to the on-chip Rx Input Amp.
15	**Rx Amp Out:** The output of the on-chip Rx Input Op-Amp. This circuit may be used, with external components, as a signal amplifier and an anti-aliasing filter prior to the Rx Lowpass Filter, or for other purposes. See Figure 2 for component details.
16	**Rx Sub-Audio In:** The received sub-audio (CTCSS/NRZ) input. This input is internally biased to $V_{DD}/2$ and requires to be a.c. coupled or biased. See Figure 2 for component details.
17	**Rx Sub-Audio Out:** The output of the Rx Lowpass Filter. This output may be coupled into the on-chip amplifier or comparator as required.
18	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS} by capacitor C_8 (see Figure 2).
19	**Comparator In (-):** The inverting input to the on-chip "comparator" amplifier. See Figures 2, 3 and 4.
20	**Comparator (+):** The non-inverting input to the on-chip "comparator" amplifier. See Figures 2, 3 and 4.
21	**Comparator Out:** The output of the "comparator" amplifier. This node is also internally connected to the input of the Digital Noise Filter (see Figure 1). When both decoders are Powersaved, this output is at a logic "0."
22	**NOTONE Timing:** External RC components connected to this pin form the timing mechanism of a NOTONE period timer. The external network determines the 'charge-rate' of the timer to $V_{DD}/2$. Expiry of the timer will cause an interrupt. This facility is only used in the CTCSS Rx mode. See Page 11.
23	**$\overline{\text{Wake}}$:** This 'real-time ' input can be used to reactivate the FX805 from the 'Powersave All' condition using an externally derived signal. The FX805 will be in a 'Powersave All' condition when both this pin and Bit 0 of the Control Register are set to a logic "1." Recovery from "Powersave All" is achieved by putting either the Wake pin or the 'Powersave All' bit to logic "0," thus allowing FX805 activation by the µController or an external signal, such as R.S.S.I. or Carrier Detect.
24	**V_{DD}:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within the Sub-Audio Signalling Processor are dependant upon this supply.

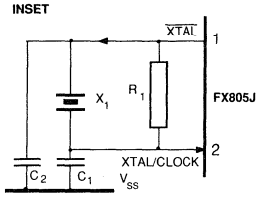
NOTE: (i) Further information on external components and DBS 800 system integration of this microcircuit are contained in the System Support Document, Document 2.
(ii) A glossary of abbreviations used in this document can be found on Page 9.
(iii) Guidance upon the generation and manipulation of NRZ Rx and Tx data is given in DBS 800 Application Support Document, Document 4.

***"C-BUS"** is CML's proprietry standard for the transmission of commands and data between a µController and DBS 800 microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined soley by the µController.*

Application Information

External Components





Component	Value	Component	Value	Component	Value
R_1 =	1.0MΩ	R_9 =	Fig.4	C_6 =	1.0µF
R_2	360kΩ	R_{10}	Fig.4	C_7	0.1µF
R_3	10.0kΩ	R_{11}	Fig.4	C_8	1.0µF
R_4	150kΩ	C_1	33.0pF	C_9	Fig.4
R_5	100kΩ	C_2	33.0pF	D_1	silicon small sig
R_6	150kΩ	C_3	1.5µF	D_2	silicon small sig
R_7	22.0kΩ	C_4	15.0µF	X_1	f_{XTAL} 4.00MHz
R_8	360kΩ	C_5	1.0µF		

Fig.2 Recommended External Components

Notes *on external components and connections*

1. Xtal/clock circuitry components shown INSET are recommended in accordance with CML Application Note D/XT/1 April 1986. The DBS 800 System Information Document contains additional notes on Xtal/clock distribution and frequencies.
2. R_8 is a System Component. Its value is chosen, for example, with the FX806 Modulation Summing Amplifier, to provide a sub-audio signal level of -11.0dB to the system modulator.
3. Components R_6 and C_6 are NOTONE timing components.
4. R_2 and R_5 are dependant upon the input signal level. Values given are for the specified composite signal (Page 16).
5. R_7 is used as the DBS 800 system common-pullup for the "C-BUS" Interrupt Request (IRQ) line, the optimum value of this component will depend upon the circuitry connected to the IRQ line.

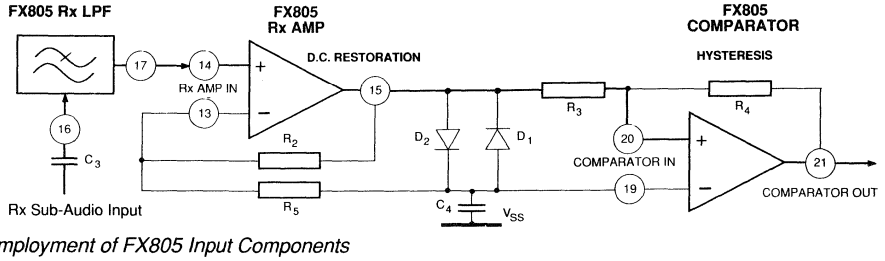


Fig.3 Employment of FX805 Input Components

With reference to Figure 2, Figures 3 and 4 show in detail recommended alternative component configurations for the FX805.

Application Information...

External Components .....

Figure 3 shows an input component configuration for use generally for CTCSS signal and NRZ data reception.

Input coupling capacitor C_3 is required because the Rx Sub-Audio Input is held at V_{BIAS} during all powered conditions of the FX805. Diodes D_1 and D_2 can be any silicon small-signal diode.

The output resistance (open loop) of the on-chip Rx Amp is ≈ 6kΩ. In the configuration shown in Figure 3, the (Rx Amp) RC time-constant is therefore 90ms. If this period is too long for some systems, ie. those employing half-duplex, short data bursts, an external amplifier should be considered in place of the FX805 on-chip Rx Amp.

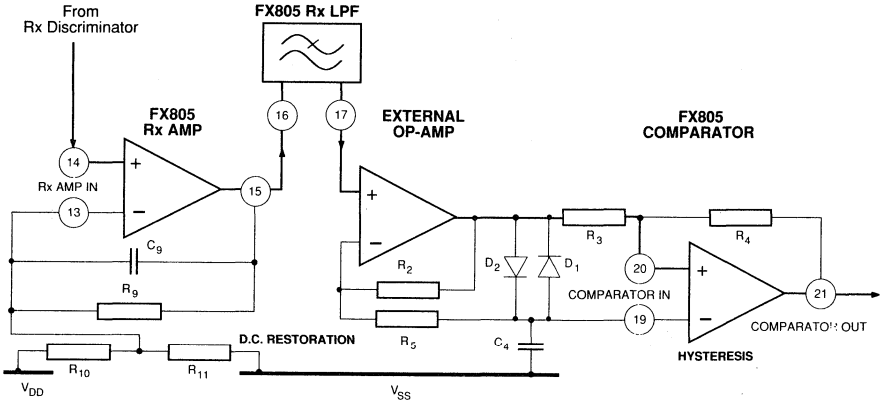


Fig.4 FX805 Input Components Using an External Op-Amp

Using an External Op-Amp

For d.c. coupling the FX805 to the receiver's discriminator output when using NRZ communication, it is recommended that an additional, external Op-Amp is employed as configured in Figure 4. This configuration will allow long sequences of logic "1s" or "0s" to be successfully decoded (eg. LTR™ trunking systems).

Components R_9, R_{10} and R_{11} should be calculated to provide an accurate potential of 2.5V d.c. (equal to V_{BIAS}) at pin-junction 15/16 when using a discriminator input. C_9 is an optional component which, if additional filtering is required, should be calculated, with R_9 to provide a lowpass cut-off frequency (f_{CO}) of 500Hz.

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FX805 Operational Modes

NRZ Tx (Encoding)

The NRZ Encoder is formed by a shift register and the Tx Sub-Audio Lowpass Filter. Data loaded from the Command Data line is output one 8-bit byte at a time from the NRZ Tx Data Register. The output data-signal level may be adjusted and filtered. Data may be pre-emphasized via a "C-BUS" command. The Tx baud rate is programmed as the NRZ Tx Baud Rate ($R_{NRZ\,Tx}$) (Table 5/Page 13).

CTCSS Tx (Encoding)

The CTCSS Tone Encoder comprises a clock-divider programmed by an 11-bit binary number (Q) loaded to the CTCSS Tx Frequency Register (Table 5) via the "C-BUS" Command Data line.

The square-wave output of the encoder is fed through the Tx Level Adjust variable gain block to the Tx Sub-Audio Lowpass Filter, a variable bandwidth circuit controlled by 4-bits (P) of the CTCSS Tx Frequency Register. The Tx Sub-Audio output is a sine-wave. Standard and non-standard sub-audio tones are available, a 'CDCS' turn-off tone may be generated.

NRZ Rx (Decoding)

Input (NRZ type) sub-audio signals are filtered and the data clock extracted. Decoded data is serially loaded into a shift register buffer. This data is output one 8-bit byte at a time as Reply Data from the NRZ Rx Data Register to the µController. The expected Rx baud rate is programmed as the NRZ Rx Baud Rate ($R_{NRZ\,Rx}$) (Table 5). Any codeword recognition can be carried out by software.

CTCSS Rx (Decoding)

Received CTCSS signals are filtered, coherence is increased by the digital noise filter. The quality of the signal is assessed by measurement of the cycle-to-cycle period variance and, provided it is sufficiently good, the frequency is measured over a period of 122.64 milliseconds.

If the average signal quality is consistently too low, NOTONE is indicated, if not, the input frequency is precisely indicated in the CTCSS Rx Frequency Register in a binary form as shown in Figure 6.

As any single sub-audio tone within the specified range may be selected, this would enable a 'CDCS' turn-off tone (of 134Hz) to be decoded whilst operating in the NRZ Rx mode.

Controlling Protocol

Control of the FX805 Sub-Audio Signalling Processor's operation is by communication between the µController and the FX805 internal registers on the "C-BUS," using Address/Commands (A/Cs) and appended instructions or data (see Figure 9). The use and content of these instructions is detailed in the following paragraphs and tables. The Address Select input enables the addressing of 2 separate FX805s on the "C-BUS" to provide full-duplex multi-mode signalling.

FX805 Internal Registers

FX805 internal registers are detailed below:

Control Register ($70_H/78_H$) – Write only, control and configuration of the FX805.

Status Register ($71_H/79_H$) – Read Only, reporting of device functions.

CTCSS Rx Frequency Register ($72_H/7A_H$) – Read Only, a 2-byte binary word indicating the frequency of the received sub-audio input.

CTCSS Tx Frequency / NRZ Tx or Rx Baud Rate Register ($73H/7B_H$) – Write Only, a 2-byte command to set the relevant parameters.

NRZ Rx Data Register ($74_H/7C_H$) – Read Only, a single-byte of received NRZ data.

NRZ Tx Data Register ($75_H/7D_H$) – Write Only, to load a single-byte of NRZ data for transmission one byte at a time.

Gain-Set Register ($76_H/7E_H$) – Write Only, a single byte to set the gain of the Tx Lowpass Filter.

Address/Commands

The first byte of a loaded data sequence is always recognized by the "C-BUS" as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an Address/Command byte followed by either:

(i) further instructions or data or,

(ii) a Status or data Reply.

Instructions and data are loaded and transferred, via "C-BUS," in accordance with the timing information given in Figures 9 and 10.

Placing the Address Select input at a logic "0" will address FX805 No.1, a logic "1" will address FX805 No.2.

Tables 1 and 2 show the list of A/C bytes relevant to the FX805. A complete list of DBS 800 "C-BUS" Address allocations is published in the System Support Document, Document 2.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB							LSB	+	Data Byte/s
General Reset	01	0	0	0	0	0	0	0	1		
Write to Control Reg.	70	0	1	1	1	0	0	0	0	+	1 byte Instruction to Control Reg.
Read Status Reg.	71	0	1	1	1	0	0	0	1	+	1 byte Reply from Status Reg.
Read CTCSS Rx Freq. Reg.	72	0	1	1	1	0	0	1	0	+	2 byte Reply of CTCSS Rx data
Write to CTCSS Tx Frequency/ NRZ Baud Rate Reg.	73	0	1	1	1	0	0	1	1	+	2 byte Instruction for Tx Frequency and NRZ Tx/Rx baud rates
Read NRZ Rx Data Reg.	74	0	1	1	1	0	1	0	0	+	1 byte binary data Reply
Write to NRZ Tx Data Reg.	75	0	1	1	1	0	1	0	1	+	1 byte binary data Command
Write to Gain-Set Reg.	76	0	1	1	1	0	1	1	0	+	1 byte Instruction for Tx Output

Table 1 – FX805 No.1 "C-BUS" Address/Commands — Address Select input at a logic "0"

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB							LSB	+	Data Byte/s
General Reset	01	0	0	0	0	0	0	0	1		
Write to Control Reg.	78	0	1	1	1	1	0	0	0	+	1 byte Instruction to Control Reg.
Read Status Reg.	79	0	1	1	1	1	0	0	1	+	1 byte Reply from Status Reg.
Read CTCSS Rx Frequency Reg.	7A	0	1	1	1	1	0	1	0	+	2 byte Reply of CTCSS Rx data
Write to CTCSS Tx Frequency/ NRZ Baud Rate Reg.	7B	0	1	1	1	1	0	1	1	+	2 byte Instruction for Tx Frequency and NRZ Tx/Rx baud rates
Read NRZ Rx Data Reg.	7C	0	1	1	1	1	1	0	0	+	1 byte binary data Reply
Write to NRZ Tx Data Reg.	7D	0	1	1	1	1	1	0	1	+	1 byte binary data Command
Write to Gain-Set Reg.	7E	0	1	1	1	1	1	1	0	+	1 byte Instruction for Tx Output

Table 2 – FX805 No.2 "C-BUS" Address/Commands — Address Select input at a logic "1"

Controlling Protocol...

"Write to Control Register" – A/C 70_H (78_H), followed by 1 byte of Command Data.

Table 3 (below) shows the configurations available to the FX805. Bits 5, 6 and 7 are used together to Enable and Powersave circuit sections as required.

Setting			*Control Bits*	
MSB			***Transmitted First***	
7	***6***	***5***	**Functions Enabled**	**Functions Powersaved**
0	0	0	CTCSS Decoder	NRZ Decoder and Both Encoders
0	0	1	NRZ Decoder	CTCSS Decoder and Both Encoders
0	1	0	CTCSS Encoder	All Decoders
0	1	1	NRZ Encoder	All Decoders
1	0	0	CTCSS Encoder and Decoder	NRZ Encoder and Decoder
1	0	1	NRZ Encoder and CTCSS Decoder	None
1	1	0	NRZ Decoder and CTCSS Decoder	All Encoders
1	1	1	NRZ Decoder	All Encoders (except Tx Sub-Audio LPF) and CTCSS Decoder

4	
1	Enable Audio Output – Used with Bit 3
0	Disable Audio Output – Output to V_{BIAS}
3	
1	Enable Sub-Audio Bandstop Filter (Audio Signal Path)
0	By-pass Sub-Audio Bandstop Filter
2	
1	Enable All FX805 Interrupts
0	Disable All FX805 Interrupts
1	
1	Set Rx Lowpass Filter bandwidth to 180Hz – For low CTCSS Tones or NRZ Data
0	Set Rx Lowpass Filter bandwidth to 260Hz
0	
1	All Encoders and Decoders Powersaved (Powersave All)
0	All Encoders and Decoders Enabled unless individually Powersaved

Table 3 Control Register

General Reset

Upon Power-Up the "bits" in the FX805 registers will be random (either "0" or "1"). A General Reset Command (01_H) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX805.

Control Register	*Set as 00_H*
Status Register	*Set as 00_H*
NOTONE Timer	*Discharged*

Warning – The following FX805 register configurations are not affected by a General Reset command:

CTCSS Rx Frequency
CTCSS Tx Frequency/NRZ Baud Rate Register
NRZ Rx Data Register
NRZ Tx Data Register
Gain-Set Register

Note that setting the Control Register in this way (General Reset) will set the FX805 to the CTCSS Decode mode and overwrite a "Powersave All" instruction.

It should also be considered that a General Reset command will reset ALL DBS 800 microcircuits operating on the "C-BUS."

Glossary of Abbreviations

Below is a list of abbreviations used within this Data Sheet.

CDCS	Continuous Digitally Coded Squelch
CTCSS	Continuous Tone Controlled Squelch
DPL™	Digital Private Line
LTR™	Logic Trunked Radio
NRZ	Non-Return-to-Zero data levels
f_{CO}	Filter cut-off frequency
$f_{CTCSS\ IN}$	Sub-Audio Rx frequency
$f_{CTCSS\ OUT}$	Sub-Audio Tx frequency
f_{TONE}	Tone frequency
f_{XTAL}	Xtal/clock frequency
$R_{NRZ\ Rx}$	NRZ Rx baud rate
$R_{NRZ\ Tx}$	NRZ Tx baud rate
S_{INPUT}	Audio input signal

"Read Status Register" – A/C 71_H (79_H), followed by 1 byte of Reply Data.

The Status Register indicates the operational condition of the FX805. Bits 0 to 5 are set individually to indicate specific actions within the device. When a Status Bit is set to a logic "1," an Interrupt Request (IRQ) output is generated. A read of the Status Register will reset the interrupt condition and ascertain the state of this register.

Table 4 (below) shows the conditions indicated by the Status Bits.

Status Bit	*Set By*	*Logic*	*Cleared By*	*Logic*
MSB *7, 6*	*Received First* Not used	"0"	Not used	"0"
5	NRZ data transmission complete. No new data loaded.	"1"	1. Write to NRZ Tx Data Reg. or, 2. General Reset or, 3. NRZ Encoder Powersave.	"0"
4	NRZ Tx Data Buffer ready for next data byte.	"1"	1. Write to NRZ Tx Data Reg. or, 2. General Reset or, 3. NRZ Tx Powersave.	"0"
3	New NRZ Rx data received **before** last byte was read.	"1"	1. Read NRZ Rx Data Reg. or, 2. General Reset or, 3. NRZ Decoder Powersave.	"0"
2	1 byte of NRZ Rx data received.	"1"	1. Read NRZ Rx Data Reg. or, 2. General Reset or, 3. NRZ Decoder Powersave.	"0"
1	NOTONE Timer period expired.	"1"	1. Read Status Register or, 2. General Reset or, 3. CTCSS Decoder Powersave.	"0"
0	Rx Tone Measurement complete.	"1"	1. Read Status Register or, 2. General Reset or, 3. CTCSS Decoder Powersave.	"0"

Table 4 Status Register

"Read CTCSS Rx Frequency Register" – A/C $72_H(7A_H)$, followed by 2 bytes of Reply Data.

Measurement of CTCSS Rx Frequency ($f_{CTCSS\ IN}$)

The input sub-audio signal ($f_{CTCSS\ IN}$), is filtered and measured in the Frequency Counter over the "measurement period" (122.64ms).

The measuring function counts the number of complete input cycles occurring within the measurement period and then the number of measuring-clock cycles necessary to make up the period.

When the measurement period of a successful decode is complete, the Rx Tone Measurement bit in the Status Register, and the Interrupt bit are set.

The CTCSS Rx Frequency Register will now indicate the sub-audio signal frequency ($f_{CTCSS\ IN}$) in the form of 2 data bytes (1 and 0) as illustrated in Figure 6.

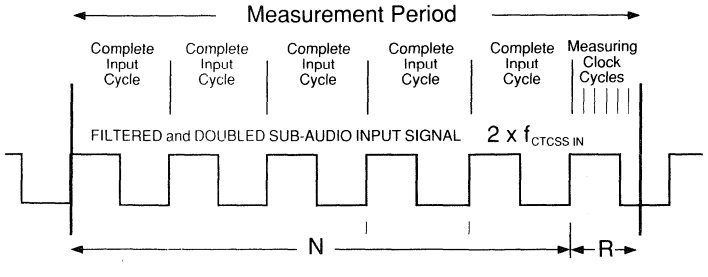


Fig.5 Measurement of a CTCSS Rx Frequency

"Read CTCSS Rx Frequency Register" .....

The Integer (N) – Byte 1

A binary number representing 'twice the number of complete input sub-audio cycle periods' counted during the measurement period of 122.64ms

The Remainder (R) – Byte 0

A binary number representing the remainder part, R, of 2 x Sub-Audio Input Frequency. 'R = number of specified measuring-clock cycles' required to complete the specified measurement period (See N). The clock-cycle frequency is 4166.6Hz

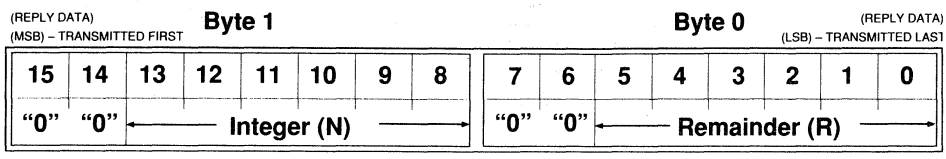


Fig. 6 Format of the CTCSS Rx Frequency Register

CTCSS Rx Frequency Register

Figure 6 (above) shows the format of the CTCSS Rx Frequency Register.

Bits 8 (LSB) to 13 (MSB) are used to represent the Integer (N). From Byte 1, valid values of $N = 16 \leq N \leq 61$.

ie. values of N less than 16 and greater than 61 are not within the specified frequency band.

Bits 0 (LSB) to 5 (MSB) (Byte 0) are used to represent the Remainder (R). From Byte 0, valid values of $R = \leq 31$.

This register is not affected by the General Reset command (01_H) and may adopt any random configuration at Power-Up.

CTCSS Rx Frequency Measurement Formulæ

To assist in the production of 'look-up' tables and limit-values in the µController and provide guidance upon the determination of N and R from a measured CTCSS frequency, the following formulæ show the derivation of the CTCSS Rx Frequency ($f_{CTCSS\ IN}$) from the measured data bytes (N and R).

$f_{CTCSS\ IN}$

In the measurement period of 122.64ms there are N cycles at 2 x $f_{CTCSS\ IN}$ and R clock-cycles at 4166.6Hz, for any input frequency.

So

$$f_{CTCSS\ IN} = \frac{N \times f_{XTAL}}{1920 \times (511 - R)}\ Hz \quad [1]$$

$$R = INT\left[511 - \left[\frac{N \times f_{XTAL}}{1920 \times f_{CT\ CSS\ IN}}\right] + 0.5\right] \quad [3]$$

$$N = INT\left[\frac{(1920 \times 511 \times f_{CTCSS\ IN})}{f_{XTAL}}\right] \quad [2]$$

Calculate N first

Examples (f_{XTAL} = 4.00MHz): $f_{CTCSS\ IN}$ = 100Hz N = 24 R = 11; $f_{CTCSS\ IN}$ = 250Hz N = 61 R = 3

NOTONE Timing

The input sub-audio signal is monitored by the Frequency Assessment circuitry. Before any NOTONE action is enabled, the FX805 must have achieved at least one successful "Tone Measurement Complete" action.

If there is no signal or the signal is of a consistently poor quality, the NOTONE Timer will start to charge via the timing components. When the timing period has expired (at $V_{DD}/2$), an Interrupt and a Status bit (NOTONE Timer Expired) are generated. This is a one-shot function and is reset by a "Tone Measurement Complete" interrupt.

"Write to CTCSS Tx Frequency/NRZ Baud Rate Register" – A/C 73_H ($7B_H$), followed by 2 bytes of Command Data.

The information loaded to this register will set either the:

(a) CTCSS Tx Tone Frequency $f_{CTCSS\ OUT}$

(b) NRZ Tx Baud Rate $R_{NRZ\ Tx}$

(c) NRZ Rx Baud Rate $R_{NRZ\ Rx}$

The chosen mode for this register (a, b or c) is determined by the FX805 operational mode enabled by the Control Register (Table 3), as shown in the table below.

Control Register Bits 7	6	5	FX805 Mode Enabled	CTCSS Tx/NRZ Baud Rate Register Function
0	0	0	CTCSS Decode	
0	0	1	NRZ Decode	NRZ Rx Baud Rate
0	1	0	CTCSS Encode	CTCSS Tx Frequency
0	1	1	NRZ Encode	NRZ Tx Baud Rate
1	0	0	CTCSS Encode and Decode	CTCSS Tx Frequency
1	0	1	NRZ Encode and CTCSS Decode	NRZ Tx Baud Rate
1	1	0	NRZ and CTCSS Decode	NRZ Rx Baud Rate
1	1	1	NRZ Decode	NRZ Rx Baud Rate

Table 5 CTCSS Frequency/NRZ Baud Rate Register Configurations

Data Format

Data is transmitted, via "C-BUS," to this register as 2 bytes of Command Data (1 and 2) distributed as command words P and Q, in the form illustrated in Figure 7. This register is not affected by the General Reset command (01_H) and may adopt any random configuration at Power-Up.

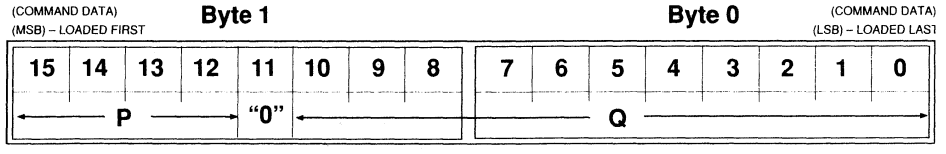


Fig.7 Format of the CTCSS Tx Frequency/NRZ Baud Rate Register

Command Words P and Q

With reference to Figure 7, the two data words, P and Q, loaded to this register are interpreted as:

P = a binary number to set the Tx Sub-Audio Lowpass Filter bandwidth (applicable to NRZ Encode and CTCSS Encode modes).

Q = a binary number to set the frequency or baud rate of the selected function (see Table 5).

Command Word 'P'

Bits 15	14	13	LSB 12	'P'	LPF Bandwidth
0	0	1	0	2	300Hz
0	0	1	1	3	200Hz
0	1	0	0	4	150Hz
0	1	0	1	5	120Hz
0	1	1	0	6	100Hz
0	1	1	1	7	85.7Hz
1	0	0	0	8	75Hz

Table 6 Valid Values of 'P'

Bits 12 to 15 are used to produce the data word '**P**' as shown in Table 6 (left). The cut-off frequency f_{CO} (0.5dB point) of the Tx Sub-Audio Lowpass Filter is calculated as:

$$f_{CO} = \frac{f_{XTAL}}{32 \times 208.33 \times \text{'P'}}$$

$$\text{so 'P'} = \frac{f_{XTAL}}{32 \times 208.33 \times f_{CO}}$$

Table 6 is given as an example and calculated using a Xtal/clock (f_{XTAL}) frequency of 4.00MHz. As illustrated, only values of '**P**' of *2 to 8* are usable.

Controlling Protocol...

"Write to CTCSS Tx Frequency/NRZ Baud Rate Register" .....

Command Word 'Q'

With reference to Figure 7, Bits 0 to 10 are used to produce the data word '**Q**' which sets one of the parameters described below. As can be seen, command word '**Q**' could be used to produce a word whose value would produce a parameter outside that specified (Pages 16 and 17), care should be taken not to do this. Examples for limits of '**Q**' in each operational configuration are included. '**Q**' = 0 is not valid in the following calculations. Bit 11 is not used and must be set to logic "0"

(a) CTCSS Tx Tone Frequency ($f_{CTCSS\ OUT}$)

$$f_{CTCSS\ OUT} = \frac{f_{XTAL}}{32 \times \text{'Q'}} \text{ Hz}$$

$$\text{so 'Q'} = \frac{f_{XTAL}}{32 \times f_{CTCSS\ OUT}} \text{ Hz}$$

Example Limits

$f_{CTCSS\ OUT}$	=	67Hz	
so 'Q'	=	1866	"11101001010"
$f_{CTCSS\ OUT}$	=	250Hz	
so 'Q'	=	500	"00111110100"

(b) NRZ Tx Baud Rate ($R_{NRZ\ Tx}$)

$$R_{NRZ\ Tx} = \frac{f_{XTAL}}{32 \times \text{'Q'}} \text{ bits/sec}$$

$$\text{so 'Q'} = \frac{f_{XTAL}}{32 \times R_{NRZ\ Tx}}$$

$R_{NRZ\ Tx}$	=	67 bits/sec	
so 'Q'	=	1866	"11101001010"
$R_{NRZ\ Tx}$	=	300 bits/sec	
so 'Q'	=	417	"00110100001"

(c) NRZ Rx Baud Rate ($R_{NRZ\ Rx}$)

$$R_{NRZ\ Rx} = \frac{f_{XTAL}}{32 \times 11 \times \text{'Q'}} \text{ bits/sec}$$

$$\text{so 'Q'} = \frac{f_{XTAL}}{352 \times R_{NRZ\ Rx}}$$

$R_{NRZ\ Rx}$	=	100 bits/sec	
so 'Q'	=	114	"00001110010"
$R_{NRZ\ Rx}$	=	300 bits/sec	
so 'Q'	=	38	"00000100110"

"Read NRZ Rx Data Register" – A/C 74_H ($7C_H$), followed by 1 byte of Reply Data.

Received NRZ data bits are organized into bytes and made available to the µController via the Reply Data line. As 8 bits are received into this register an interrupt is generated to indicate that a complete byte has been received, this byte must be read before the arrival of the last (8th) bit of the next incoming byte, if this is not done, an interrupt to indicate this condition will be generated and the previous Rx data is discarded (See Table 4, Status Register, Bits 2 and 3).

Word synchronization is not provided. Byte synchronization and any codeword recognition will be performed by the host µController. The Rx baud rate is set by writing to the CTCSS Tx Frequency/NRZ Baud Rate Register (73_H/$7B_H$). The first bit received is the first bit sent to the µController.

This register is not affected by the General Reset command (01_H) and may adopt any random configuration at Power-Up.

"Write to NRZ Tx Data Register" – A/C 75_H ($7D_H$), followed by 1 byte of Command Data.

A byte for transmission is loaded from the "C-BUS" Command Data line with this A/C. The first data-bit received via the "C-BUS" is transmitted first. This transmitter operation is **non-inverting**.

The first data-byte loaded after the NRZ Encoder is enabled (Control Register) initiates the transmission sequence and an interrupt will be generated when the NRZ Tx Data Buffer is ready for the next data-byte. Subsequently, interrupts occur for every 8 bits transmitted.

Transmission is terminated, the Tx Sub-Audio Output placed at V_{BIAS}, and an interrupt generated if the next byte is not loaded within 7 bit periods. (See Table 4, Status Register, Bits 4 and 5).

This register is not affected by the General Reset command (01_H) and may adopt any random configuration at Power-Up.

"Write to Gain-Set Register" – A/C 76_H ($7E_H$), followed by 1 byte of Command Data.

Setting				Gain Setting	
MSB					
7	6	5	4	*Transmitted Bit 7 First*	
0	0	0	0	These 4 Bits Must be "0"	
		3		**Pre-Emphasis Setting**	
		1		1.72dB Gain Enabled	
		0		1.72dB Gain Disabled	
2		1	0	**Tx Level Adjust Gain Setting**	
0		0	0	-2.58	dB
0		0	1	-1.72	dB
0		1	0	-0.86	dB
0		1	1	0	dB
1		0	0	+0.86	dB
1		0	1	+1.72	dB
1		1	0	+2.58	dB
1		1	1	Not Used	

Table 7 Gain-Set Register Settings

The Gain-Set Register Settings

The settings of this register control the CTCSS and NRZ signal level that is presented at the Tx Sub-Audio Output.

Bit 3, when enabled, is used to produce a pre-emphasis effect on the NRZ Tx Data by increasing the gain of the data bit **before** a level change (Figure 8 below), by 1.72dB to make that data pulse level slightly more positive (or negative). The signal level will be 1.72dB greater than that set by Bits 0 to 2. If the Tx Sub-Audio Output level is set to +2.58dB, the pre-emphasized level will be +4.3dB.

The pre-emphasis function, will remain enabled until disabled by setting Bit 3 to a logic "0." If this function remains enabled when using the CTCSS Encoder the output signal level may be adversely affected, therefore this function should only be enabled when in the NRZ Encode mode.

This register is not affected by the General Reset command (01_H) and may adopt any random configuration at Power-Up.

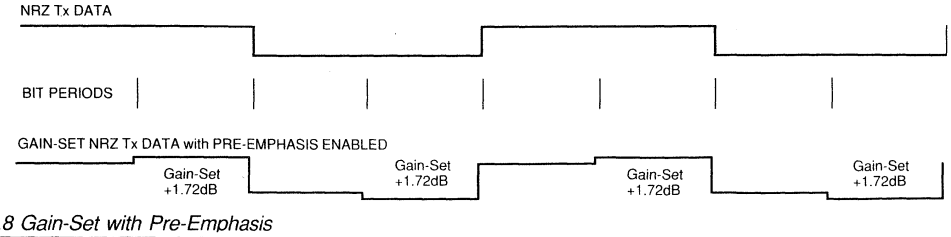


Fig.8 Gain-Set with Pre-Emphasis

Timing Information

Timing Diagrams

Figure 9 shows the timing parameters for two-way communication between the µController and the FX805 on the "C-BUS." Figure 10 shows, in detail, the timing relationships for "C-BUS" information transfer.

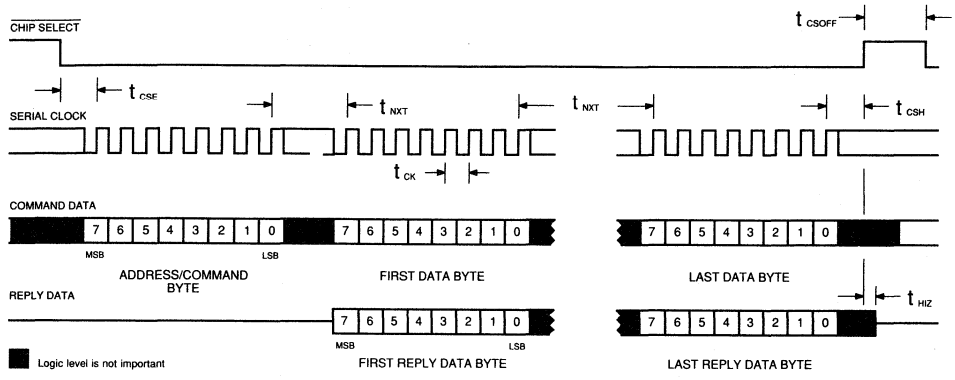


Fig.9 "C-BUS" Timing Information

NOT TO SCALE

Parameter	Min.	Typ.	Max.	Unit
t_{CSE}	2.0	–	–	µs
t_{CSH}	4.0	–	–	µs
t_{CSOFF}	2.0	–	–	µs
t_{NXT}	4.0	–	–	µs
t_{CK}	2.0	–	–	µs
t_{CH}	500	–	–	ns
t_{CL}	500	–	–	ns
t_{CDS}	250	–	–	ns
t_{CDH}	0	–	–	ns
t_{RDS}	250	–	–	ns
t_{RDH}	50.0	–	–	ns
t_{HIZ}	–	–	2.0	µs

Notes

(1) Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the FX805 MSB (bit 7) first, LSB (bit 0) last.
(2) Data is clocked into the FX805 and into the µController on the rising Serial Clock edge.
(3) Loaded data instructions are acted upon at the end of each individual, loaded byte.
(4) To allow for differing µController serial interface formats, the FX805 will work with either polarity Serial Clock pulses.

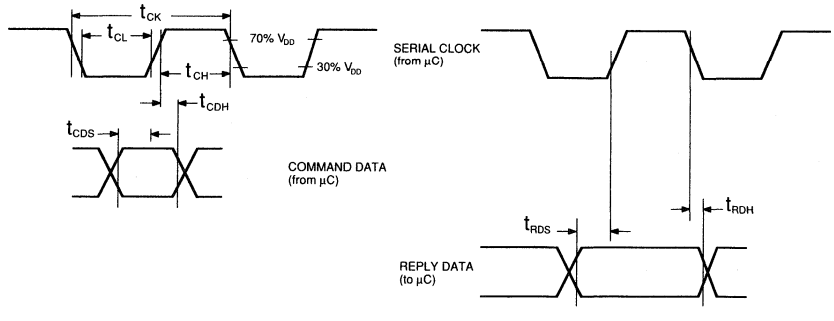


Fig.10 "C-BUS" Timing Relationships

NOT TO SCALE

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX805J**	-40°C to +85°C (cerdip)
	FX805LG/LS	-40°C to +85°C (plastic)
Storage temperature range:	**FX805J**	-55°C to +125°C (cerdip)
	FX805LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:
V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_{XTAL} = 4.0MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz.
Composite Signal = 308mVrms @ 1kHz + 75mVrms Noise + 31mVrms Sub-Audio Signal.
Noise Bandwidth = 5kHz Band Limited Gaussian.

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage			4.5	5.0	5.5	V
Supply Current	(All Functions Enabled)		–	5.0	–	mA
	(Decoders Only Enabled)		–	1.9	–	mA
	(Powersave All)		–	0.9	–	mA
Analogue Impedances						
Rx Sub-Audio Input			350	–	–	kΩ
Audio Input			350	–	–	kΩ
Audio By-Pass Switch 'On'		5	–	2.0	–	kΩ
Audio By-Pass Switch 'Off'		5	1.0	10.0	–	MΩ
Rx Amp Input (+ and -)			1.0	10.0	–	MΩ
Comparator Input (+ and -)			1. 0	10.0	–	MΩ
Rx Sub-Audio Output			–	2.0	–	kΩ
Tx Sub-Audio Output	(Encoder Enabled)	5	–	2.0	–	kΩ
	(Encoder Disabled)	5	–	500	–	kΩ
Audio Output	(Enabled)	5	–	2.0	–	kΩ
	(Disabled)	5	–	500	–	kΩ
Rx Amp and Comparator Outputs						
Large Signal			–	6.0	–	kΩ
Small Signal			–	600	–	Ω
Dynamic Values						
Digital Interface						
Input Logic "1"		1	3.5	–	–	V
Input Logic "0"		1	–	–	1.5	V
Output Logic "1"	(IOH = -120µA)	2	4.6	–	–	V
Output Logic "0"	(IOL = 360µA)	3	–	–	0.4	V
I_{OUT} Tristate (Logic "1" or "0")		3	–	–	4.0	µA
Input Capacitance		1	–	–	7.5	pF
Logic Input Current	(V_{IN} = 0 to 5.0V)	1	–	–	1.0	µA
IOX	(V_{OUT} = 5.0V)	4	–	–	4.0	µA
Overall Performance						
CTCSS – Decode						
Sensitivity	(Pure CTCSS Tone)	6	–	-26.0	–	dB
Response Time	(Composite Signal)					
100Hz to 257Hz Tone			–	–	250	ms
65Hz Tone		9	–	–	375	ms
Tone Measurement Resolution			–	0.2	–	%
Tone Measurement Accuracy			–	0.5	–	%
NOTONE Response Time	(Composite Signal)	7	–	–	250	ms
False Tone Interrupts	(Noise input only)	10	–	20.0	–	/Hr

Specification...

Characteristics	See Note	Min.	Typ.	Max.	Unit
CTCSS – Encode					
Frequency Range		65.0		257	Hz
Tone Frequency Resolution		–	–	0.2	%
Tone Amplitude Tolerance		-1.0	–	+1.0	dB
Rise Time (to 90%)		–	–	30.0	ms
Fall Time (to 10%)		–	–	50.0	ms
Total Harmonic Distortion		–	–	5.0	%
NRZ – Decode					
Rx Bit-Rate Sync Time		–	2	–	edges
Rx Bit Error Rate	11	–	1×10^{-3}	–	$P_{(error)}$
NRZ – Tx					
Tx Bit Rate		67.0	–	300	bits/s
Tx LPF (3dB) Bandwidth		75	–	300	Hz
Sub-Audio Tx Output Level					
CTCSS		–	0	–	dB
NRZ		–	0.871	–	V p-p
Amplitude Adjustment Range		-2.58		2.58	dB
Adjustment Step Size (7 steps)	8	–	0.86	–	dB
Sub-Audio Bandstop Filter					
Passband		297		3000	Hz
Passband Gain		–	0	–	dB
Passband Gain (w.r.t. gain at 1.0kHz)		-1.5	–	+0.5	dB
Stopband Attenuation					
at 250 Hz		–	36.0	–	dB
at 150 Hz		–	24.0	–	dB
at 100 Hz		–	18.0	–	dB
Residual Hum and Noise		–	-50.0	-46.0	dBp
Alias Frequency		–	–	62.5	kHz
Xtal/Clock Frequency (f_{XTAL})		3.9	–	4.1	MHz

Notes

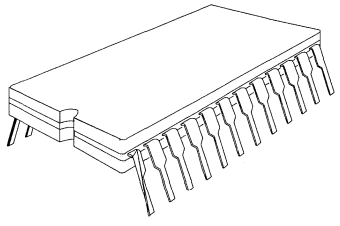
1. Device control pins; Serial Clock, Command Data, $\overline{\text{Wake}}$ and $\overline{\text{CS}}$.
2. Reply Data output.
3. Reply Data and $\overline{\text{IRQ}}$ outputs.
4. Leakage current into the "Off" $\overline{\text{IRQ}}$ output.
5. See Control Register.
6. With Input gain components set as recommended in Figure 2.
7. Probability 0.97
8. See Gain-Set Register, Table 7 - Bits 0, 1, 2 and 3.
9. For $f_{CTCSS\ IN}$ of 65Hz to 100Hz, Response Time $t_R = (100/f_{TONE}) \times 250$ ms.
10. Distributed across the Rx frequency band.
11. With 10dB signal-to-noise ratio in a bit-rate bandwidth.

Package Outlines

The FX805 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX805J 24-pin cerdip DIL (J4)

NOT TO SCALE



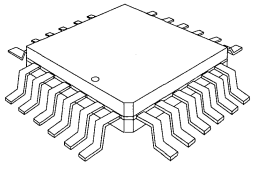
Max. Body Length 32.03mm
Max. Body Width 14.81mm

Handling Precautions

The FX805 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX805LG 24-pin quad plastic encapsulated bent and cropped (L1)

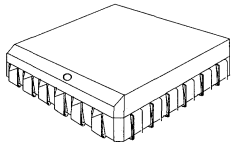
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX805LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX805J	24-pin cerdip DIL	(J4)
FX805LG	24-pin encapsulated bent and cropped	(L1)
FX805LS	24-lead plastic leaded chip carrier	(L2)

FX806A
AUDIO PROCESSOR

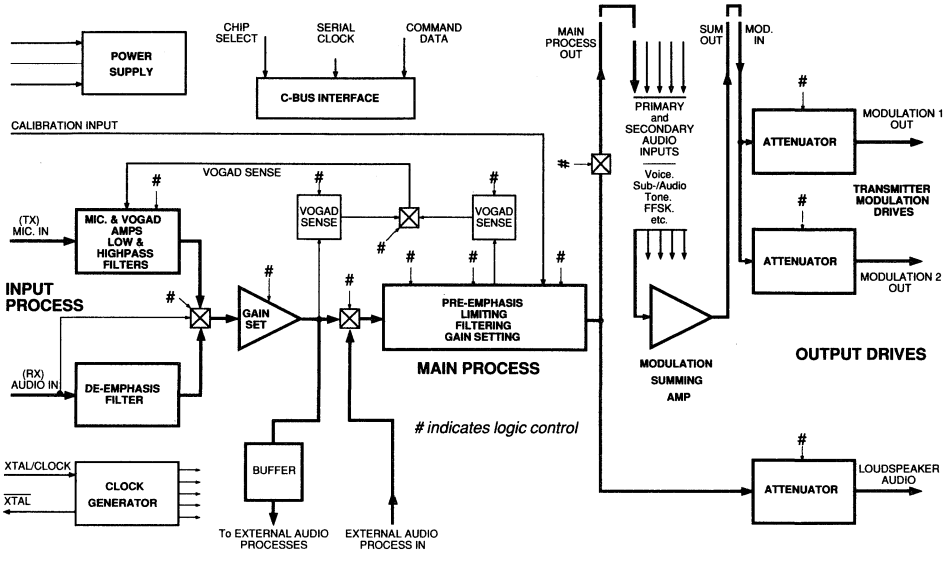


Fig.1 FX806A Audio Processor

Brief Description

Intended primarily to operate as the "Audio Terminal" of Radio Systems using the DBS 800 Digitally-integrated Baseband System, the FX806A is a PMR Audio Processor which meets EIA and CEPT audio specifications.
Using a unique filter line-up, the FX806A offers lower distortion versus modulation level figures than conventional filter/limiter configurations.

The FX806A is a half-duplex device whose signal paths and level-setting elements are dynamically configured and adjusted by digital information sent from the Radio µController using "C-BUS" hardware and software protocol.

Figure 5 shows a complete functional block diagram of the FX806A signal paths which can be viewed as 3 sections:

- **Input Process**

Selectable transmit or receive input paths.

The transmit path with low-noise input and VOGAD amplifiers and bandpass filtered stages provides good signal-to-noise performance at low input levels and minimum distortion for high-drive modulation signals.

De-emphasis is software selectable at the Rx Audio Input for FM or PM radio configurations.

This initial audio, after in-line gain adjustment, is available for switching to either external audio processes (such as scrambling) or internally to the Main Process stages.

- **Main Process**

Conditioning for Input or External Process signals with gain/pre-emphasis, high and lowpass switched capacitor filters and a transmitter deviation limiter. The Main Process Output may be switched to V_{BIAS}.

- **Summation and Output Drives**

Main "voice audio" from the Main Process is combined with signalling and data from other DBS 800 facilities, to provide the composite (in and outband) signal for the digitally adjustable Transmitter Modulation Drives.
Received audio is level (volume) adjusted for output to loudspeaker circuitry.

Signal-level stability and therefore output accuracy, of the FX806A is maintained by a voltage-controlled gain system (VOGAD) with specific gain sensors that are selected automatically by the Internal/External Mode Command. The VOGAD system permits high deviation with low distortion. This is achieved by reducing the path gain (and so reducing the distortion introduced by the Peak Deviation limiter) when the input signal is large.

Signal levels can be controlled to provide 'dynamic-compensation' for such factors as temperature drift, VCO non-linearity, etc.

FX806A audio output stages can be completely disabled or the whole microcircuit placed into a "Powersave" mode, leaving only clock and "C-BUS" circuitry active.

The FX806A is a low-power, 5-volt CMOS integrated circuit and is available in 24-pin DIL cerdip and 24-pin/lead plastic SMD packages.

Publication D/806A/3 July 1994

Pin Number Function

FX806A J/LG/LS	
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this output when a Xtal circuit is employed. See Figure 2, INSET 2.
2	**Xtal/clock**: The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2, INSET 2. This clock provides timing for on-chip elements, filters etc.
3	**Serial Clock:** The "C-BUS," serial data loading clock input. This clock, produced by the µController, is used for transfer timing of Command Data to the Audio Processor. See Timing diagrams and System Support Document.
4	**Command Data:** The "C-BUS," serial data input from the µController. Command Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. The Command/Data instruction is acted upon at the end of loading the whole instruction. Command information is detailed in Tables 1, 2, 3, 4 and 5. See Timing diagrams and System Support Document.
5	**$\overline{\text{Chip Select}}$ ($\overline{\text{CS}}$):** The "C-BUS," data loading control function. This input is provided by the µController. Command Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing diagrams and System Support Document.
6	**VOGAD Out:** The output of the relevant VOGAD sensor. This output, with external attack and decay setting components, should be connected as in Figures 2 and 3, to the VOGAD In pin.
7	**Rx Audio In:** The audio input to the FX806A from the radio receiver's demodulator circuits. This input, which requires to be a.c. coupled with capacitor C_{12}, is selected by a Control Command bit.
8	**VOGAD In:** The gain control signal from the selected VOGAD sensor (VOGAD Out) to the "Input Process" Voltage Controlled Amplifier. VOGAD operation is enabled via a Mode Command (Bit5). Individual sensors, automatically selected, permit gain control from either the Input Process or an external process. External attack and decay setting components should be applied as recommended in Figures 2 and 3.
9	**V_{BIAS}:** The output of the on-chip analogue circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by a capacitor C_{10}, See Figure 2.
10	**Mic In (+):** The non-inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2, INSET 1.
11	**Mic In (–):** The inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2, INSET 1.
12	**V_{SS}:** Negative supply rail (GND).

Pin Number Function

FX806A J/LG/LS	
13	**Mic Out:** The output of the microphone Op-Amp, used with the Mic In (–) input to provide the required gain/attenuation using external components as shown in Figure 2. The external components shown are to assist in the use of this amplifier with either inverting or non-inverting inputs. During Powersave (Volume Command) this output is placed at V_{SS}.
14	**Processed Audio In:** The input to the device from such external audio processes as Voice Store and Retrieve or Frequency Domain Scrambling. This input, which requires to be a.c. coupled with a capacitor, C_{13}, is selected by a Mode Command bit.
15	**External Audio Process:** The buffered output of the Input Processing stage. For further external audio processing prior to re-introduction at the Processed Audio In pin.
16	**CALibration Input:** A unique input, intended to be used for dynamic balancing of the modulator drives and for measuring Deviation Limiter levels. A CUE (beep) input from the FX803 Audio Tone Processor can be entered on this line. This input is selected via a Mode Command bit (11_H) and is self-biased.
17	**Main Process Out:** The output of the Main Process stage. This output is summed with additional system inputs as required (Audio, Sub-Audio Signalling, FFSK – See System Overview) in the on-chip Modulation Summing Amplifier. External components as shown in Figure 2 should be used as required.
18	**Sum In:** The input and output terminals of the on-chip Modulation Summing Amplifier. External components are required for input signals, with gain/attenuation setting as shown in Figure 2. For single-signal, no-gain requirements, Main Process Out may be linked directly to Modulation In.
19	**Sum Out:**
20	**Modulation In:** The final, composite modulating signal to VCO (Mod 1) and Reference (Mod 2) Output Drives.
21	**Audio Output:** The processed audio signal output intended as a received audio (volume) output. Though normally used in the Rx mode, operation in Tx is permitted. The output level of this attenuator is controlled via a Volume Set command. During Powersave this output is placed at V_{SS}.
22	**Modulation 1 Drive:** The drive to the radio modulator Voltage Controlled Oscillator (VCO), from the composite audio summing stage.
23	**Modulation 2 Drive:** The drive to the radio modulator Reference Oscillator, from the composite audio summing stage. **NOTE:** These VCO output attenuators are individually adjustable using the Modulator Levels command. During Powersave these outputs are placed at V_{SS}.
24	V_{DD}: Positive supply rail. A single, stable +5 volt supply is required. Levels and voltages within the Audio Processor are dependant upon this supply.

Analogue Application Information

External Components

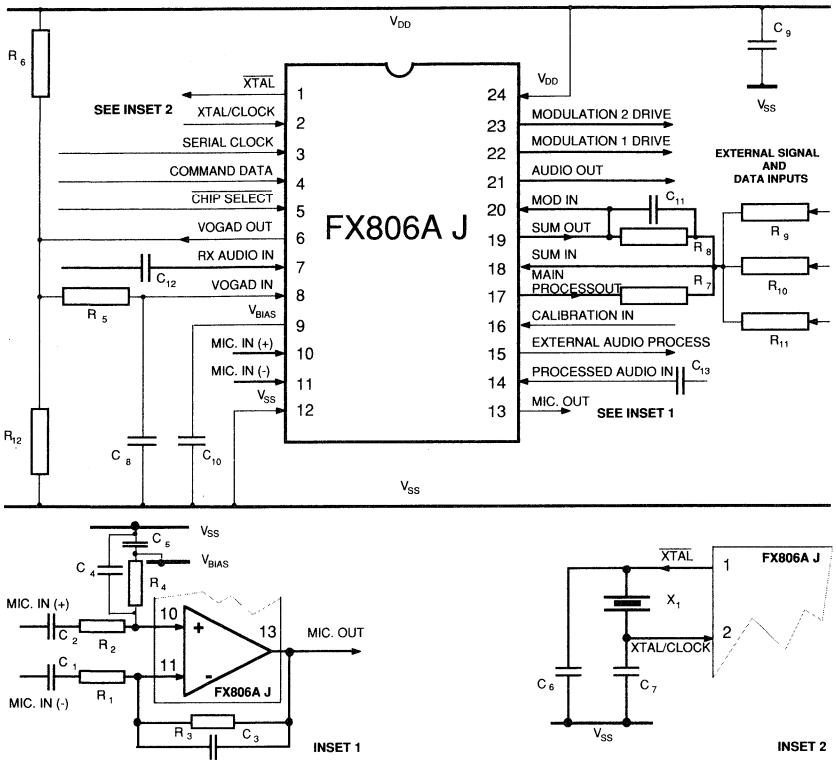


Fig.2 Recommended External Components

Component		Value						
R_1	=	10.0kΩ	R_{10}	=	100kΩ	C_7	=	5 – 65pF
R_2		10.0kΩ	R_{11}		100kΩ	C_8		1.0µF
R_3		20.0kΩ	R_{12}		2.2MΩ	C_9		1.0µF
R_4		20.0kΩ	C_1		470nF	C_{10}		1.0µF
R_5		10.0kΩ	C_2		470nF	C_{11}		22pF
R_6		2.2MΩ	C_3		270pF	C_{12}		100nF
R_7		100kΩ	C_4		270pF	C_{13}		10.0nF
R_8		100kΩ	C_5		0.1µF	X_{13}		4.0MHz
R_9		100kΩ	C_6		33pF	Tolerance: R = ±10%. C = ± 20%		

Notes

To demonstrate the versatility of the Mic. inputs, Input Op-Amp gain/attenuation components for a voltage gain of 6.0dB are shown (INSET 1) in a differential configuration. Components for a single (+ or -) input may be employed.

Resistor values R_7 to R_{11} (summation components) are dependant upon application and configuration requirements.

Xtal circuit capacitors C_6 (C_D) and C_7 (C_G) shown (INSET 2) are recommended in accordance with *CML Application Note D/XT/1 April 1986*. Circuit drive and drain resistors are incorporated on-chip.

Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail (V_{DD}) is fitted with a current limiting device (resistor or fast reaction fuse).

VOGAD Components Calculations – Figures 2 and 3

Provided R_5 >>1.0kΩ and $R_6 = R_{12}$ >>R_5

Then:

Attack Time (T_A) = $R_5 \times C_8$

Decay Time (T_D) = $\frac{R_6 \times C_8}{2}$

Analogue Application Information .....

The Gain Control System

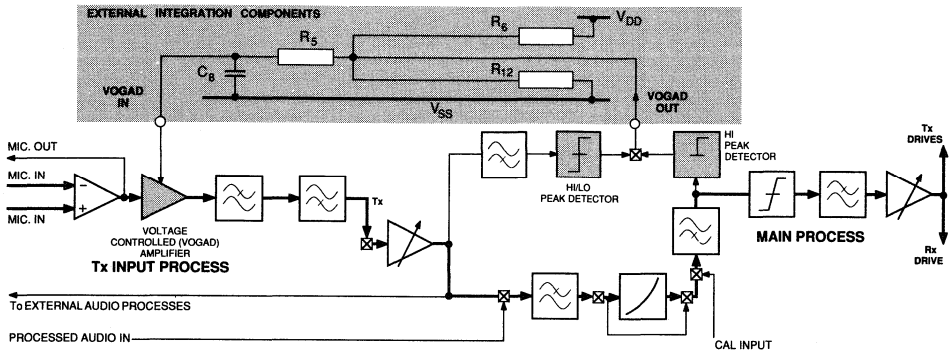


Fig.3 "VOGAD" Sensors and Timing Components – (part of Fig.4)

Tx gain control of the FX806A is by 1 of 2 selectable signal peak detectors whose output is fed via external integrating components to the Voltage Controlled Amplifier positioned in the Tx Input Process Path.

The integrated level to the VOGAD In pin causes the Voltage Controlled Amplifier gain to be reduced. VOGAD attack and decay calculations are described at the foot of the proceeding page.

The FX806A automatically chooses the appropriate peak detector when the signal path is set by a Mode Command. The Hi/Lo Peak Detector is employed when external audio processes are used.

The Hi Peak Detector is employed when external audio processes are not used.

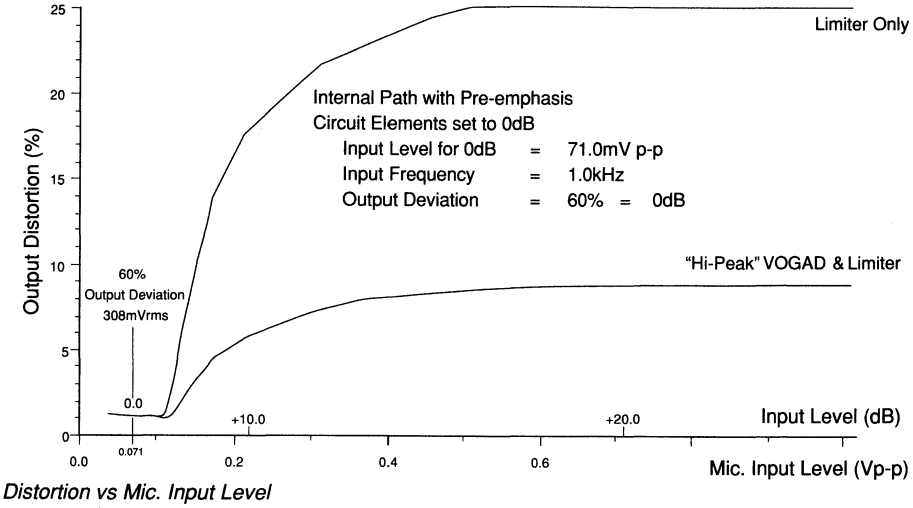


Fig.4 Distortion vs Mic. Input Level

Suggested Calibration Methods

To effectively null all internal microcircuit tolerances, the following initial calibration routine is suggested:

Tx Calibration : *From Mic. In to Modulator Drives Out*

Disable Peak Detectors (Mode Command).
Set Transmitter Drives to 0dB (Mod Levels Set).
Pre-emphasis may be employed as required (Control Command).
Set Input Level Amp to 0dB (Control Command).

(1) Mic. In = 250mVrms at 1kHz; Set Process Gain Amp for output of 1440mV p - p (100% deviation).

(2) With Process Gain Amp set as (1); Mic In = 25mVrms at 1kHz, set Input Level Amp for output level of 308 mVrms (60% deviation).

Rx Calibration: *From Rx Audio In to Audio Output*

Set Audio Output Drive to 0dB (Volume Set).
Leave Process Gain Amp set as In (1) (above).

(3) With Rx Audio In level of between 154mVrms and 308mVrms (see Specification page), at 1kHz, set the Input Level Amp for an output level of 308mVrms.

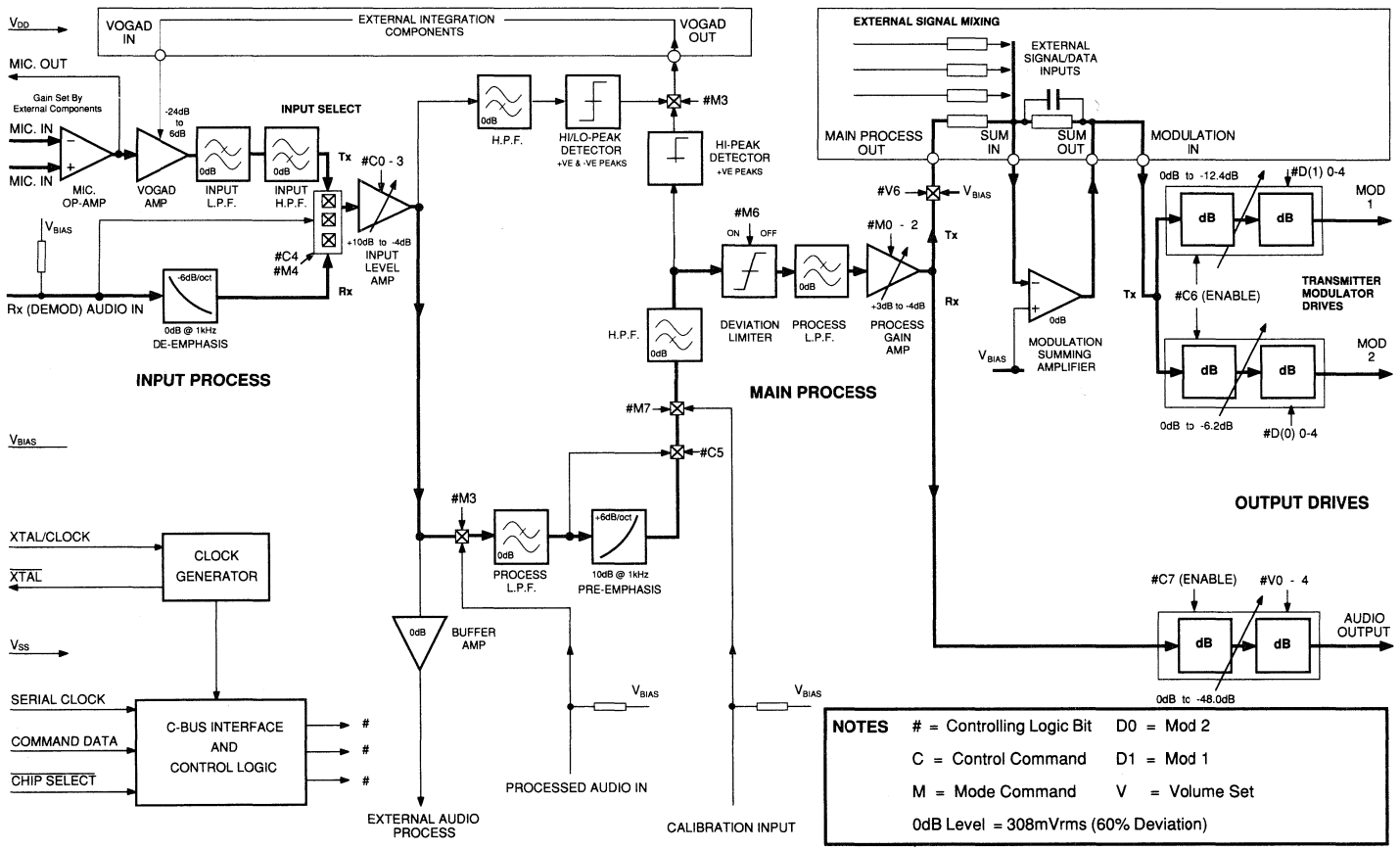


Fig.5 PLMR Audio Processor – Facilities

Controlling Protocol

Control of the functions and levels within the FX806A PLMR Audio Processor is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the FX806A. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex	Binary MSB LSB		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Control Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
Mode Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
Mod. Levels Set	12	0 0 0 1 0 0 1 0	+	2 bytes	4
Volume Set	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 "C-Bus" Address/Commands

In "C-BUS" protocol the FX806A is allocated Address/Command (A/C) values 10_H to 13_H. "C-BUS" Command, Mode, Modulation and Volume assignments and data requirements are given in Table 1 and illustrated in Figure 5 (Main Block Diagram). Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the "C-BUS" interface recognises the first byte after $\overline{\text{Chip Select}}$ (logic "0") as an Address/Command.

Function or Level control data, which is detailed in Tables 2, 3, 4 and 5, is acted upon at the end of the loaded instruction.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). A General Reset Command (01_H) will be required. This command is provided to "reset" all devices on the "C-BUS" and has the following effect on the FX806A.

Control Address Command	Loaded as 00_H
Mode Address Command	Loaded as 00_H
Volume Set	Loaded as 00_H

Control Command

(Preceded by A/C 10_H)

Setting				*Control Bits*
				Transmitted First
				MSB
				Bit 7
				Audio Output (Rx)
				0 Disabled
				1 Enabled
				6
				Modulation Drives
				0 Disabled
				1 Enabled
				5
				Pre-Emphasis
				0 By-Pass
				1 Enabled
				4
				Input Select
				0 Rx Audio In
				1 Mic. In
3	***2***	***1***	***0***	**Input Level Set**
0	0	0	0	Input Amp Disabled
0	0	0	1	-4.0dB
0	0	1	0	-3.0dB
0	0	1	1	-2.0dB
0	1	0	0	-1.0dB
0	1	0	1	0dB
0	1	1	0	1.0dB
0	1	1	1	2.0dB
1	0	0	0	3.0dB
1	0	0	1	4.0dB
1	0	1	0	5.0dB
1	0	1	1	6.0dB
1	1	0	0	7.0dB
1	1	0	1	8.0dB
1	1	1	0	9.0dB
1	1	1	1	10.0dB

Table 2 Control Commands

Mode Command

(Preceded by A/C 11_H)

Setting			*Mode Bits*
			Transmitted First
			MSB
			Bit 7
			Drive Source
			0 Signals
			1 Calibration
			6
			Deviation Limiter
			0 Disabled
			1 Enabled
			5
			VOGAD
			0 Disabled
			1 Enabled
			4
			De-Emphasis
			0 Enabled
			1 By-Passed
			3
			Signal Select
			0 Internal
			1 External
2	***1***	***0***	**Process Gain Set**
0	0	0	-4.0dB
0	0	1	-3.0dB
0	1	0	-2.0dB
0	1	1	1.0dB
1	0	0	0dB
1	0	1	1.0dB
1	1	0	2.0dB
1	1	1	3.0dB

Table 3 Mode Commands

Modulator Levels

(Preceded by A/C12$_H$)

Setting	Modulator Drives
Byte 1	***First byte for transmission***
MSB	
7 0	***6*** 0 — ***5*** 0 — Must be "0"
4 ***3*** ***2*** ***1*** ***0***	**Mod. 1** Attenuation
0 0 0 0 0	12.4dB
0 0 0 0 1	12.0dB
0 0 0 1 0	11.6dB
0 0 0 1 1	11.2dB
0 0 1 0 0	10.8dB
0 0 1 0 1	10.4dB
0 0 1 1 0	10.0dB
0 0 1 1 1	9.6dB
0 1 0 0 0	9.2dB
0 1 0 0 1	8.8dB
0 1 0 1 0	8.4dB
0 1 0 1 1	8.0dB
0 1 1 0 0	7.6dB
0 1 1 0 1	7.2dB
0 1 1 1 0	6.8dB
0 1 1 1 1	6.4dB
1 0 0 0 0	6.0dB
1 0 0 0 1	5.6dB
1 0 0 1 0	5.2dB
1 0 0 1 1	4.8dB
1 0 1 0 0	4.4dB
1 0 1 0 1	4.0dB
1 0 1 1 0	3.6dB
1 0 1 1 1	3.2dB
1 1 0 0 0	2.8dB
1 1 0 0 1	2.4dB
1 1 0 1 0	2.0dB
1 1 0 1 1	1.6dB
1 1 1 0 0	1.2dB
1 1 1 0 1	0.8dB
1 1 1 1 0	0.4dB
1 1 1 1 1	0dB
Byte 0	***Last byte for transmission***
MSB	
7 0	***6*** 0 — ***5*** 0 — Must be "0"
4 ***3*** ***2*** ***1*** ***0***	**Mod. 2** Attenuation
0 0 0 0 0	6.2dB
0 0 0 0 1	6.0dB
0 0 0 1 0	5.8dB
0 0 0 1 1	5.6dB
0 0 1 0 0	5.4dB
0 0 1 0 1	5.2dB
0 0 1 1 0	5.0dB
0 0 1 1 1	4.8dB
0 1 0 0 0	4.6dB
0 1 0 0 1	4.4dB
0 1 0 1 0	4.2dB
0 1 0 1 1	4.0dB
0 1 1 0 0	3.8dB
0 1 1 0 1	3.6dB
0 1 1 1 0	3.4dB
0 1 1 1 1	3.2dB
1 0 0 0 0	3.0dB
1 0 0 0 1	2.8dB
1 0 0 1 0	2.6dB
1 0 0 1 1	2.4dB
1 0 1 0 0	2.2dB
1 0 1 0 1	2.0dB
1 0 1 1 0	1.8dB
1 0 1 1 1	1.6dB
1 1 0 0 0	1.4dB
1 1 0 0 1	1.2dB
1 1 0 1 0	1.0dB
1 1 0 1 1	0.8dB
1 1 1 0 0	0.6dB
1 1 1 0 1	0.4dB
1 1 1 1 0	0.2dB
1 1 1 1 1	0dB

Table 4 Modulator Drive Levels

Volume Set

(Preceded by A/C13$_H$)

Setting	Volume Set
MSB	
7 0	***6*** 0 — ***5*** 0 — ***Transmitted First***
0	1 — **Main Process Out**
	Enabled
	Biased
	Powersave
	Chip Enabled
	Powersaved
4 ***3*** ***2*** ***1*** ***0***	**Volume Set** Attenuation
0 0 0 0 0	Off
0 0 0 0 1	48.0dB
0 0 0 1 0	46.4dB
0 0 0 1 1	44.8dB
0 0 1 0 0	43.2dB
0 0 1 0 1	41.6dB
0 0 1 1 0	40.0dB
0 0 1 1 1	38.4dB
0 1 0 0 0	36.8dB
0 1 0 0 1	35.2dB
0 1 0 1 0	33.6dB
0 1 0 1 1	32.0dB
0 1 1 0 0	30.4dB
0 1 1 0 1	28.8dB
0 1 1 1 0	27.2dB
0 1 1 1 1	25.6dB
1 0 0 0 0	24.0dB
1 0 0 0 1	22.4dB
1 0 0 1 0	20.8dB
1 0 0 1 1	19.2dB
1 0 1 0 0	17.6dB
1 0 1 0 1	16.0dB
1 0 1 1 0	14.4dB
1 0 1 1 1	12.8dB
1 1 0 0 0	11.2dB
1 1 0 0 1	9.6dB
1 1 0 1 0	8.0dB
1 1 0 1 1	6.4dB
1 1 1 0 0	4.8dB
1 1 1 0 1	3.2dB
1 1 1 1 0	1.6dB
1 1 1 1 1	0dB

Table 5 Volume Set

Command Loading Address/Commands and data bytes must be loaded in accordance with the information given in Figure 6 (Timing).

The **Powersave** function is instigated by bit 5 of the Volume Set Command (Table 5).

During Powersave, all internal elements except the Clock Generator and "C-BUS" Interface are off, with the Mic Op-Amp and Output Drive stage outputs connected to V_{SS}.

Modulator Drives are controlled separately, but the whole two-byte Modulator Drive command must be loaded for each required adjustment.

$\overline{\text{Chip Select}}$ must be held at a logic "1" for the period "t_{CSOFF}" between transactions.

Command Loading and Timing

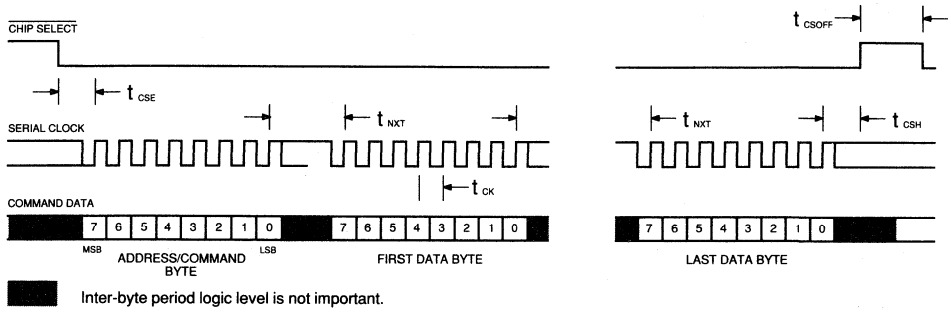


Fig.6 "C-BUS" Timing Information

Parameter	Min.	Typ.	Max.	Unit
t_{CSE}	2.0	–	–	µs
t_{CSH}	4.0	–	–	µs
t_{CSOFF}	2.0	–	–	µs
t_{NXT}	4.0	–	–	µs
t_{CK}	2.0	–	–	µs

Notes

(1) Command Data is transmitted to the peripheral MSB (bit7) first, LSB (bit0) last.
(2) Data is clocked into the peripheral on the rising clock edge.
(3) Loaded data instructions are acted upon at the end of each individual, loaded byte.
(4) To allow for differing µController serial interface formats, the FX806A will work with either polarity Serial Clock pulses.

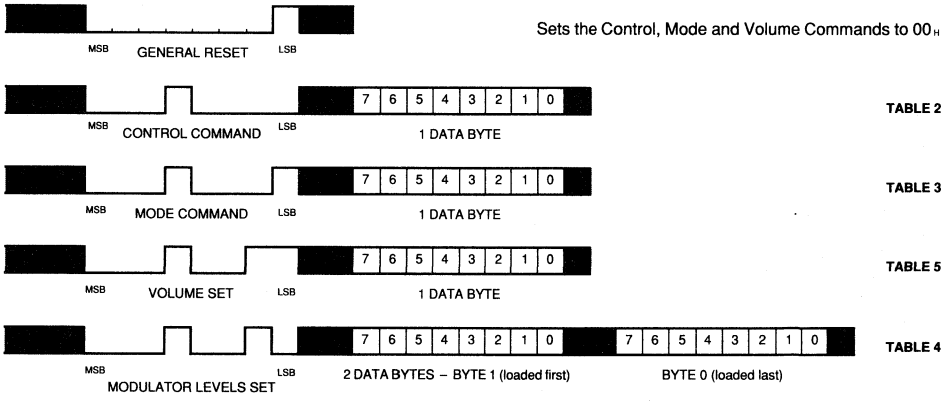


Fig.7 Examples of "Command Data" Configurations

To assist in rapid setting, the "quick-reference" guide below should be used together with Figure 5.

Control	**A/C = 10_H**
Bit 7	Audio Out (Rx) Enable
6	Modulator Drive Enable
5	Pre-Emphasis Enable
4	Input Select (Rx/Tx)
3 – 0	Input Level Set (-4dB to 10dB)
Mode	**A/C = 11_H**
Bit 7	Drive Source
6	Deviation Limiter Enable
5	VOGAD Enable
4	De-Emphasis Enable
3	Signal Select
2 – 0	Process Gain Set (-4dB to 3dB)

Modulator Levels	**A/C = 12_H**
Byte 1	
Bit 7 – 5	"0"
4 – 0	Mod 1 Attenuation (0 to 12.4dB)
Byte 2	
7 – 5	"0"
4 – 0	Mod 2 Attenuation (0 to 6.2dB)
Volume Set	**A/C = 13_H**
Bit 7 – 6	"0"
5	Powersave
4 – 0	Volume Set Attenuation (0 to 48dB)

Table 6 "Quick-Reference" to Command Allocations

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX806A J**	-40°C to +85°C (cerdip)
	FX806A LG/LS	-40°C to +85°C (plastic)
Storage temperature range:	**FX806A J**	-55°C to +125°C (cerdip)
	FX806A LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.0MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz *(60% deviation, FM).*

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (All Elements Enabled)		–	8.0	–	mA
(Maximum Powersave)		–	0.7	–	mA
"C-BUS" Interface					
Input Logic "1"		3.5	–	–	V
Input Logic "0"		–	–	1.5	V
Input Leakage Current (logic "1 or 0")		-1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
Dynamic Values					
Overall Performance					
Microphone Input	4, 5	–	25.0	–	mVrms
Rx Audio In	6, 5	154	–	308	mVrms
Output Drive Levels					
For 60% Deviation	5, 7	291	308	326	mVrms
For 100% Deviation	5, 7, 8	–	1,440	–	mV p - p
Passband Frequencies	1	297	–	3000	Hz
Passband Ripple	2	-2.0		0.5	dB
Stopband Attenuation	1, 3				
f = 150Hz		10.0	12.0	–	dB
f = 3400Hz		–	2.0	–	dB
f = 6000Hz		30.0	36.0	–	dB
f = 8000Hz to 20,000Hz		–	60.0	–	dB
Signal Path Noise					
Rx	11	–	-60.0	–	dBp
Rx	10	–	-55.0	–	dB
Tx	11	–	-50.0	–	dBp
Tx	10	–	-45.0	–	dB
Distortion		–	1.0	–	%
Circuit Elements – Figure 5					
Mic Amp or Mod Summation Amp					
Open Loop Gain		–	50.0	–	dB
Bandwidth		20.0	–	–	kHz
Input Impedance		10.0	–	–	MΩ
Output Impedance (Open Loop)		–	6.0	–	kΩ
(Closed Loop)		–	600	–	Ω
De-emphasis					
Slope		–	-6.0	–	dB/oct.
Gain (at 1.0kHz)		–	0	–	dB
Input Impedance		–	500	–	kΩ
Voltage Controlled Gain Amp					
Gain (Non-Compressing)	5	–	6.0	–	dB
(Full Compression)		–	-24.0	–	dB
VOGAD In Input Impedance		–	10.0	–	MΩ

Specification.....

Characteristics	See Note	Min.	Typ.	Max.	Unit
VOGAD Peak Detectors					
Output Impedance - Logic "1" (Compress)		–	1.0	–	kΩ
- Logic "0"		–	10.0	–	MΩ
Hi/Lo Peak Detector Thresholds		–	1,300	–	mV p - p
Hi Peak Detector Threshold		–	650	–	mV +ve pk
Input (Low + Highpass) Filter					
Gain (at 1.0kHz)		-1.0	0	1.0	dB
Input Level Amp					
Nominal Adjustment Range		-4.0		10.0	dB
Error of any Setting		-1.0	–	1.0	dB
Step Size		0.75	1.0	1.25	dB
External Audio Buffer					
Gain		-0.1	0	0.1	dB
Pre-emphasis (Main Process and VOGAD)					
Slope		–	6.0	–	dB/oct.
Gain (at 1.0kHz)		–	10.0	–	dB
Process Highpass Filter					
Gain (at 1.0kHz)		-1.0	0	1.0	dB
Deviation Limiter					
Threshold		–	1,300	–	mV p - p
Gain		-0.5	–	0.5	dB
Process Lowpass Filter					
Gain (at 1.0kHz)		-1.0	0	1.0	dB
Process Gain Amp					
Nominal Adjustment Range		-4.0		3.0	dB
Error of any Setting		-0.5	–	0.5	dB
Step Size		0.75	1.0	1.25	dB
Output Impedance		–	600	–	Ω
Transmitter Modulator Drives					
Input Impedance		–	15.0	–	kΩ
Mod.1 Attenuator					
Nominal Adjustment Range		0		12.4	dB
Error of any Setting		-1.0	–	1.0	dB
Step Size		0.2	0.4	0.6	dB
Output Impedance		–	600	–	Ω
Mod.2 Attenuator					
Nominal Adjustment Range		0		6.2	dB
Error of any Setting		-0.6	–	0.6	dB
Step Size		0.1	0.2	0.3	dB
Output Impedance		–	600	–	Ω
Audio Output Attenuator					
Nominal Adjustment Range		0		48.0	dB
Error of any Setting		-1.5	–	1.5	dB
Step Size		–	1.6	–	dB
Output Impedance		–	600	–	Ω
Miscellaneous Impedances					
Processed Audio Input		–	500	–	kΩ
Calibration Input		–	500	–	kΩ
External Process Out		–	100	–	Ω
Rx with De-Emphasis By-Pass		–	25.0	–	kΩ

Notes

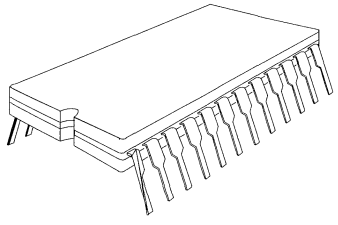
1. Between Mic. or Rx inputs to Modulator or Audio outputs.
2. The deviation from the ideal overall response that includes the pre- or de-emphasis slope.
3. Excluding the effect of the pre- or de-emphasis slope.
4. Producing an output of 0dB with the Mic. Op-Amp set to 6dB (as shown in Figure 2) and the Modulator Drives set to 0dB.
5. With Output Drives set to 0dB and the system calibrated, as described in the Application pages.
6. Input level range for 0dB output, by adjustment of the Input Level Amp.
7. It is recommended that these output levels will produce 60% or 100% deviation in the transmitter.
8. With the microphone input level 20dB above the level required to produce 0dB at the Output Drives.
9. Using external components recommended in Figure 2.
10. In a 30kHz bandwidth.
11. dBp = Psophometrically weighted measurement.

Package Outlines

The FX806A is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX806A J 24-pin cerdip DIL (J4)

NOT TO SCALE



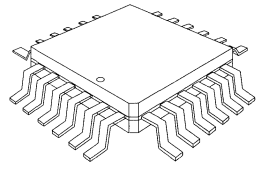
Max. Body Length 32.03mm
Max. Body Width 14.81mm

Handling Precautions

The FX806A is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX806A LG 24-pin quad plastic encapsulated bent and cropped (L1)

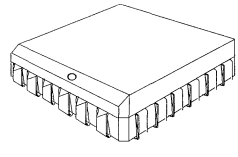
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX806A LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX806A J 24-pin cerdip DIL (J4)

FX806A LG 24-pin encapsulated bent and cropped (L1)

FX806A LS

FX809
FFSK Modem

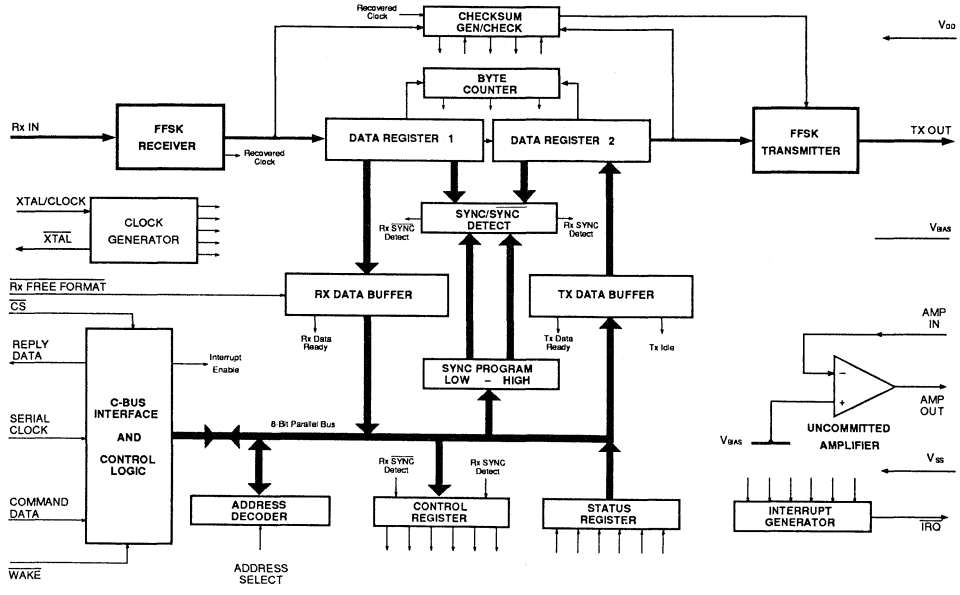


Fig 1. FX809 FFSK Modem

Brief Description

An intelligent, half-duplex, FFSK/MSK modem which operates under "C-BUS" control. In addition this modem provides software selectable checksum generation and error checking, in accordance with MPT1327.

The FX809, using Interrupt and Status Register procedures, performs the functions described below:

In Tx mode the FX809 will:

1. (a) Accept from the host and transmit, 8-bit bytes of data as instructed (Preamble, Sync, Address and data).

   (b) internally calculate and insert a 2 byte checksum based upon the preceeding 6 bytes of data, or

   (c) disable the internal checksum generator and continuously transmit the data supplied.
2. Transmit 1 hang-bit and go to Tx Idle when all loaded data bytes have been transmitted.

In Rx mode the FX809 will:

1. Detect and achieve bit synchronization within 16 bits.
2. (a) Search and detect the user-programmed Sync (or its opposite logic sense) Word and achieve frame sychronization. Data will then be output in 8-bit bytes via the Rx Data Buffer.

   (b) Use the received checksum to calculate the presence of any errors, setting the Status Register accordingly.
3. Make the incoming data directly available, via the Rx Data Buffer (Rx Freeformat), overriding synchronization requirements.

The FX809 achieves Rx input timing by recovering an Rx clock from the incoming data stream. Output tones are timed to the internally generated transmit clock. Filter, register clocks and transmit FFSK tone frequencies are derived internally from the external Xtal or clock pulse input.

For compliance with the MPT 1327 Signalling Specification a 4.032MHz Xtal or clock input will be required.

NOTE: All information contained in this data sheet is specified using a 4.032 MHz Xtal, 1200 bps baud rate, Mark and Space frequencies 1200 Hz and 1800 Hz.

The FX809 is a low-power 5-volt integrated circuit, incorporating "Powersave" modes to further reduce power requirements.

An uncommitted amplifier is provided on chip for general purpose applications within DBS 800.

The FX809 is available in 24-pin cerdip DIL and 24-pin/lead plastic SMD packages.

Publication D/809/3 July 1994
Provisional Issue

Pin Number FX809 J/LG/LS	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this input when a Xtal input is used. See Figure 2, INSET.
2	**Xtal/Clock:** The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2, INSET.
3	**$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low-impedance pulldown to logic "0" when active and a high-impedance when inactive. The conditions that cause interrupts are indicated in the Status Register and are shown below: Tx Idle — Rx Data Ready — Tx Data Ready Rx SYNC Detect — Rx $\overline{\text{SYNC}}$ Detect Interrupt outputs can be disabled by bit 3 of the Control Register.
4	No Internal connection.
5	No Internal connection.
6	**$\overline{\text{Rx Freeformat}}$:** Used in the Rx mode, this input, when a logic "0," allows received data to be read from the Rx Data Buffer via the Reply Data line without having to acheive byte synchronization (SYNC/$\overline{\text{SYNC}}$) first. Data will continue to be available after this input goes to a logic "1" until either a SYNC or $\overline{\text{SYNC}}$ Prime bit is set or the modem set to Tx mode. When held at a logic "1" the modem operates normally. This pin has an internal 1MΩ pullup resistor. **NOTE:** If this input is held at a logic "0" in the Tx mode, the Rx Data Ready bit in the Status Register may occasionally be set, but not cause an interrupt. If this input is a logic "0" when going into the Rx mode, an Rx Data Ready interrupt may be generated immediately, in this case the first byte of Rx data should be ignored.
7	**V_{BIAS} :** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS} by capacitor C_3, see Figure 2.
8	**Amp In:** The inverting input to the on-chip uncommitted amplifier .
9	**Amp Out:** The output of the on-chip uncommitted amplifier.
10	**Rx In:** The 1200 baud, 1200Hz/1800Hz, received FFSK signal input. The input signal to this pin must be a.c. coupled via capacitor C_4, see Figure 2.
11	No Internal connection.
12	**V_{SS}:** Negative Supply (GND).

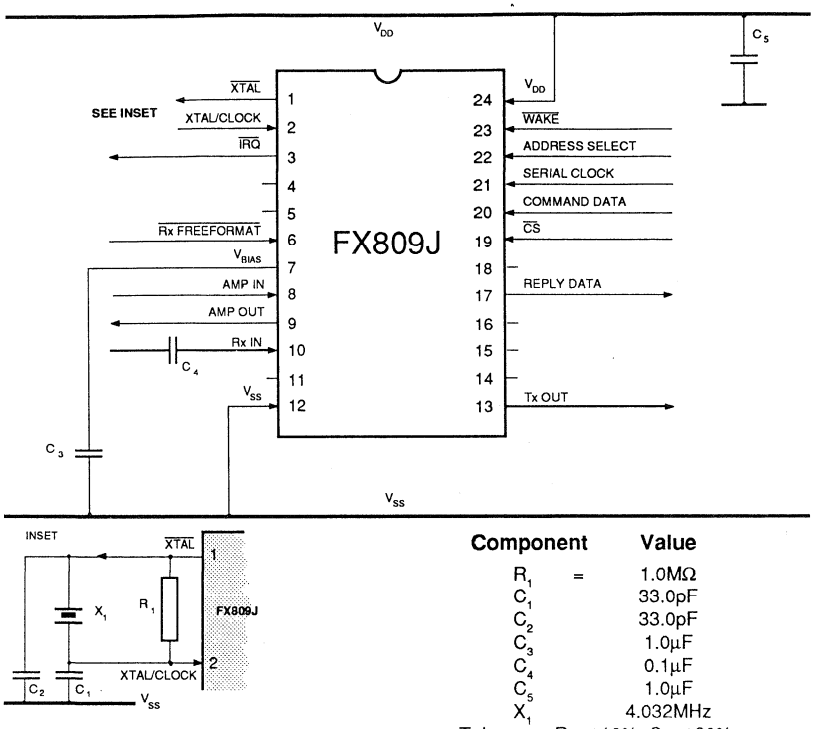
Pin Number Function

FX809 J/LG/LS	Function
13	**Tx Out:** The 1200 baud, 1200Hz/1800Hz FFSK Tx output. When not transmitting data the output impedance of this pin is high. On power-up, this output can be any level, a General Reset command is required to ensure that this output attains V_{BIAS} initially.
14	No Internal connection.
15	No Internal connection.
16	No Internal connection.
17	**Reply Data:** The "C-BUS", serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the µController. See Timing Diagrams and System Support Document, Document 2.
18	No Internal connection.
19	**Chip Select ($\overline{CS}$):** The "C-BUS" data loading control function, this input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Timing Diagrams and System Support Document, Document 2.
20	**Command Data:** The "C-BUS," serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams and System Support Document, Document 2.
21	**Serial Clock:** The "C-BUS," serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the FFSK Modem. See Timing Diagrams and System Support Document, Document 2.
22	**Address Select:** This pin enables two FX809 devices to be used on the same "C-BUS," providing full-duplex operation. When at a logic "1" Address/Command bytes (with the exception of a General Reset) must have bit 3 set to a logic "1" to address this device. See Tables 1 and 2.
23	**$\overline{Wake}$:** This input can be used to reactivate the FX809 from the 'Powersave' condition. The device will be in a 'Powersave' condition when both this pin and bit 2 of the Control Register are set to a logic "1." Recovery from Powersave is achieved by putting either the $\overline{Wake}$ pin or the Powersave bit in the Control Register to a logic "0." This allows FX809 activation by the µController or an external signal, such as R.S.S.I. or Carrier Detect.
24	**V_{DD}:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within the FFSK Modem are dependant upon this supply.

Powersave (CR bit 2)	$\overline{Wake}$	FX809 Condition
1	1	Powersave
0	1	Enabled
1	0	Enabled
0	0	Enabled

NOTE: Pins 4, 5, 11, 14, 15, 16 and 18 may be connected to V_{SS} to improve screening.

External Components



Component		Value
R_1	=	1.0MΩ
C_1		33.0pF
C_2		33.0pF
C_3		1.0µF
C_4		0.1µF
C_5		1.0µF
X_1		4.032MHz

Tolerance: R = ±10% C = ±20%

Fig.2 External Components

Modem Performance

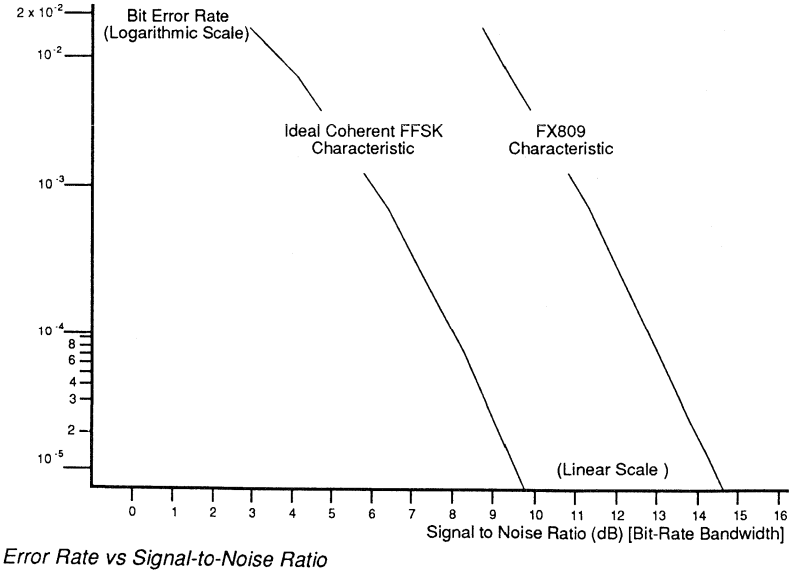


Fig.3 Bit Error Rate vs Signal-to-Noise Ratio

Controlling Protocol

Control of the functions within the FX809 FFSK Modem is by a group of Address/Commands (A/Cs) and appended data to and from the system µController via "C-BUS." Provision is made to address 2 separate FFSK Modems. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex	Binary MSB LSB		Notes
General Reset	01	0 0 0 0 0 0 0 1		Control Register bits set to logic "0"
Write to Control Register	40	0 1 0 0 0 0 0 0	+	1 byte instruction to Control Reg.
Read Status Register	41	0 1 0 0 0 0 0 1	+	1 byte reply from Status Reg.
Read Rx Data Buffer	42	0 1 0 0 0 0 1 0	+	1 byte of data from Rx Data Buffer
Write to Tx Data Buffer	43	0 1 0 0 0 0 1 1	+	1 byte of data to Tx Data Buffer
Write to SYNC Program	44	0 1 0 0 0 1 0 0	+	2 bytes of SYNC Word to SYNC Prog. Reg.

Table 1 Modem No.1 "C-Bus" Address/Commands – (Address Select input at a logic "0")

Address/Commands

Instruction and data transactions to and from the FX809 consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data, or
(ii) a Status or Rx data Reply.

Control and configuration is by writing instructions from the µController to the Control Register [40_H, (48_H)].

Reporting of FX809 configurations is by reading the Status Register [(41_H, (49_H)]. Instructions and data are transferred, via "C-BUS," in accordance with the timing information given in Figure 4.

Data for transmission as FFSK is sent to the Tx Data Buffer via the Command Data line. Received data is read from the Rx Data Buffer via the Reply Data line.

Instruction and data transactions to and from this device are preceded by the relevant Address/Command (A/C).

"C-BUS" allocations for the FX809 are shown in Tables 1 and 2.

A complete list of DBS 800 "C-BUS" Address/Command allocations is published in the System Support Document, Document 2.

Command Assignment	Address/Command (A/C) Byte Hex	Binary MSB LSB		Notes
General Reset	01	0 0 0 0 0 0 0 1		Control Register bits set to logic "0"
Write to Control Register	48	0 1 0 0 1 0 0 0	+	1 byte instruction to Control Reg.
Read Status Register	49	0 1 0 0 1 0 0 1	+	1 byte reply from Status Reg.
Read Rx Data Buffer	4A	0 1 0 0 1 0 1 0	+	1 byte of data from Rx Data Buffer
Write to Tx Data Buffer	4B	0 1 0 0 1 0 1 1	+	1 byte of data to Tx Data Buffer
Write to SYNC Program	4C	0 1 0 0 1 1 0 0	+	2 bytes of SYNC Word to SYNC Prog. Reg.

Table 2 Modem No.2 "C-Bus" Address/Commands – (Address Select input at a logic "1")

Address Select

This input allows, using the correct addressing, 2 FFSK Modems on the same BUS.

When operating in a system employing 2 FFSK Modems, 1 FFSK Modem is designated No.1 and requires its Address Select input to be held at a logic "0", and the second FFSK Modem (No. 2) requires its Address Select input to be held at logic "1."

All "C-BUS" transactions with Modem 1 will use Address/Command allocations 40_H to 44_H (Table 1) and transactions with Modem 2 will use 48_H to $4C_H$ (Table 2).

For explanation purposes further descriptions in this publication of FX809 FFSK Modem internal register functions will deal primarily with FFSK Modem No. 1 (Address Select at logic "0").

Controlling Protocol...

"Write to Control Register" This 'Write Only' register directs the modem's operation.

Setting	*Control Bits*
MSB Bit 7	***Transmitted First*** Not used Set to "0"
6	Not used Set to "0"
5	**$\overline{\text{SYNC}}$ Prime**
0	
1	Primed
4	**SYNC Prime**
0	
1	Primed
3	**Interrupt Enable**
0	Disable
1	Enable
2	**Powersave**
0	Normal Operation
1	Powersave
1	**Checksum Enable**
0	Disable
1	Enable
0	**Rx/Tx Mode**
0	Rx
1	Tx

Table 3 Control Register

$\overline{\text{SYNC}}$ Prime When set, this bit enables $\overline{\text{SYNC}}$ Word detection.
Cleared on a successful $\overline{\text{SYNC}}$ Word detection.

SYNC Prime When set, this bit enables SYNC Word detection.
Cleared on a successful SYNC Word detection.

Interrupt Enable When set, this bit allows interrupts to be output by the FX809 on the IRQ line.

Powersave Used in conjunction with the $\overline{\text{Wake}}$ input (see Pin Functions) to control the Powersave state of the FX809.

Checksum Enable When set:
In Tx: a 2-byte checksum is generated and transmitted after every 6 bytes transmitted.
In Rx: After every 8 received bytes (6 information + 2 checksum) the checksum word is checked. If the checksum is correct, the Rx Checksum True bit in the Status Register is set to a logic "1."
When this bit is a logic "0" no checksums are generated or checked.
NOTE: Checksum operation is inhibited during the SYNC/$\overline{\text{SYNC}}$ search period.

"Read Rx Data Buffer"

MSB							LSB
7	6	5	4	3	2	1	0
Rx Data Buffer							

Rx Data Buffer

This "Read Only' register contains the last byte of data received from the Data Register. Received Bit 7 (MSB) first.

"Write to Tx Data Buffer"

MSB							LSB
7	6	5	4	3	2	1	0
Tx Data Buffer							

Tx Data Buffer

This "Write Only" register contains the next byte of data to be transmitted. Bit 7 (MSB) will be transmitted first.

"Write to Sync Program"

MSB Byte 1								Byte 0							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC High								**SYNC Low**							

SYNC Program

This "Write Only" register is loaded with the required Sync Word. This word (or its opposite logic sense, $\overline{\text{SYNC}}$) is compared with the received synchronization word. If the required SYNC Word is less than 16 bits, the remaining bits must be programmed as preamble (10101010..etc.) bit 15 (MSB) is loaded first.

Controlling Protocol...

"Read Status Register" This 'Read Only' register will indicate the source of FX809 interrupts ($\overline{IRQ}$'s).

Reading	*Status Bits*
MSB	***Received First***
Bit 7	Undefined
0	"0" or,
1	"1"
6	Undefined
0	"0" or,
1	"1"
5	**Rx $\overline{SYNC}$ Detect**
0	
1	$\overline{SYNC}$
4	**Rx SYNC Detect**
0	
1	SYNC
3	**Tx Idle**
0	
1	Idle
2	**Tx Data Ready**
0	
1	Tx Data Ready
1	**Rx ChecksumTrue**
0	
1	True
0	**Rx Data Ready**
0	
1	Rx Data Ready

Table 4 Status Register

Rx $\overline{SYNC}$ Detect
Set and an Interrupt generated when the correct $\overline{SYNC}$ Word is detected (if $\overline{SYNC}$ Prime is set).

Cleared by (i) reading the Status Register,
(ii) Setting $\overline{Rx}$/Tx to logic "1."

Rx SYNC Detect
Set and an Interrupt generated when the correct SYNC Word is detected (if SYNC Prime is set).

Cleared by (i) reading the Status Register,
(ii) Setting $\overline{Rx}$/Tx to logic "1."

Tx Idle
Set and an Interrupt generated when all loaded Tx data and 1 'hang-bit' have been transmitted.

Cleared by (i) writing to the Tx Data Buffer,
(ii) Setting $\overline{Rx}$/Tx to logic "0."

Tx Data Ready
Set and an Interrupt generated indicating that a byte of data should be written to the Tx Data Buffer.

Cleared by (i) reading the Status Register and writing a byte of data to the TX Data Buffer,
(ii) Setting $\overline{Rx}$/Tx to logic "0."

Rx Checksum True
Set and an Interrupt generated by successful comparison of the received and self generated checksums.

Cleared by (i) reading the Status Register and the Rx Data Buffer,
(ii) $\overline{Rx}$/Tx being taken to logic "1."

Rx Data Ready
Set and an Interrupt generated, indicating that the Rx Data Buffer is full, a byte of data is to be read from the Rx Data Buffer, this must be read within 8 bit periods.

Cleared by (i) reading the Status Register and the Rx Data Buffer,
(ii) Setting $\overline{Rx}$/Tx to logic "1."

Interrupt Requests ($\overline{IRQ}$)

The conditions that cause interrupts to be output (if enabled by the Control Register) from the FX809 are:

Tx Idle
Tx Data Ready
Rx $\overline{SYNC}$ Detect
Rx Data Ready
Rx SYNC Detect

To ascertain the cause of the interrupt the Status Register should be read.

Interrupts are cleared:

(i) by a read of the Status Register, or

(ii) by changing the state of the $\overline{Rx}$/Tx bit.

General Reset

Upon Power-Up, the bits in the FX809 Modem registers and buffers will be random (either "0" or "1"). The General Reset command (01_H) will "reset" all microcircuits on the "C-BUS" and has the following effect on the FX809:

All bits in the Control Register will be set to logic "0." The Tx Out output will be set to V_{BIAS}.

NOTE: That the Status Register, Rx Data Buffer, Tx Data Buffer and Sync Program register are not affected by the General Reset command.

"C-BUS" Timing Information

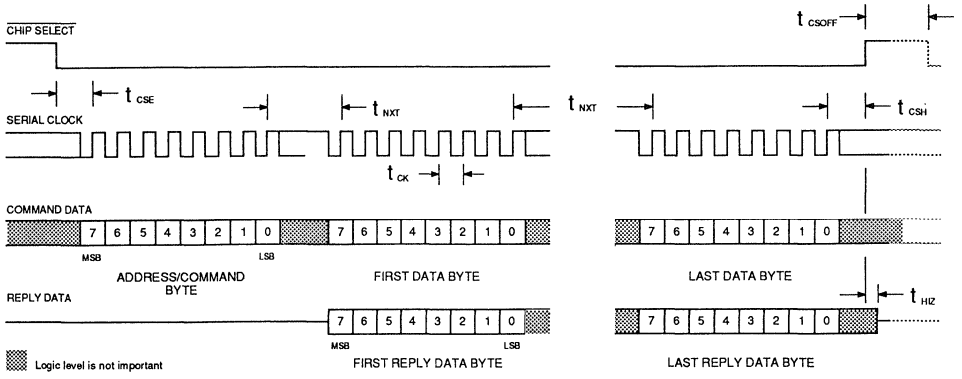


Fig.4 "C-BUS" Timing

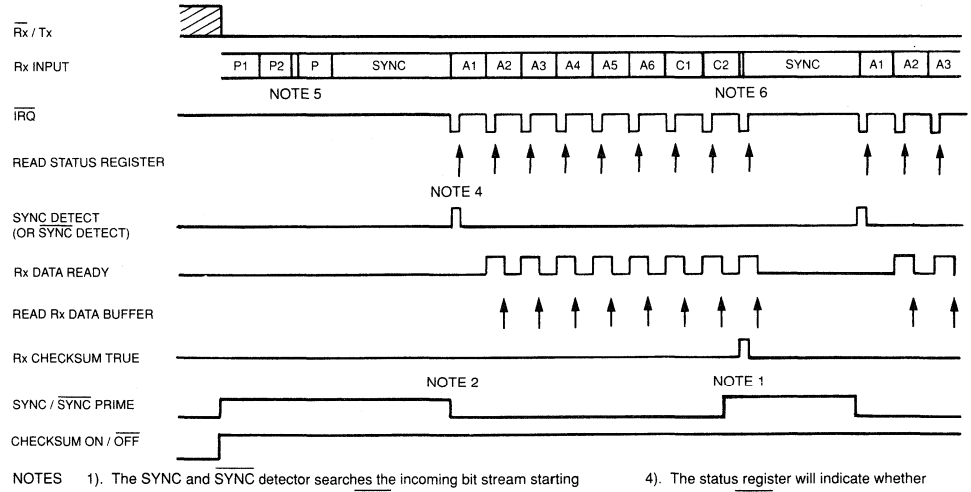
"C-BUS" Timing – Figure 4

Parameter	Min.	Max.	Unit
t_{CSE}	2.0	–	µs
t_{CSH}	4.0	–	µs
t_{HIZ}	–	2.0	µs
t_{CSOFF}	2.0	–	µs
t_{NXT}	4.0	–	µs
t_{CK}	2.0	–	µs

Notes

(1) Depending on the command, 1 or 2 bytes of Command Data is transmitted to the peripheral MSB (bit7) first, LSB (bit0) last. Reply Data is read from the peripheral MSB (bit7) first, LSB (bit0) last.
(2) Data is clocked into and out of the peripheral on the rising Serial Clock edge.
(3) Loaded commands are acted upon at the end of each command.
(4) To allow for differing µController serial interface formats "C-BUS" compatible ICs are able to work with either polarity Serial Clock pulses.

Modem Timing Information

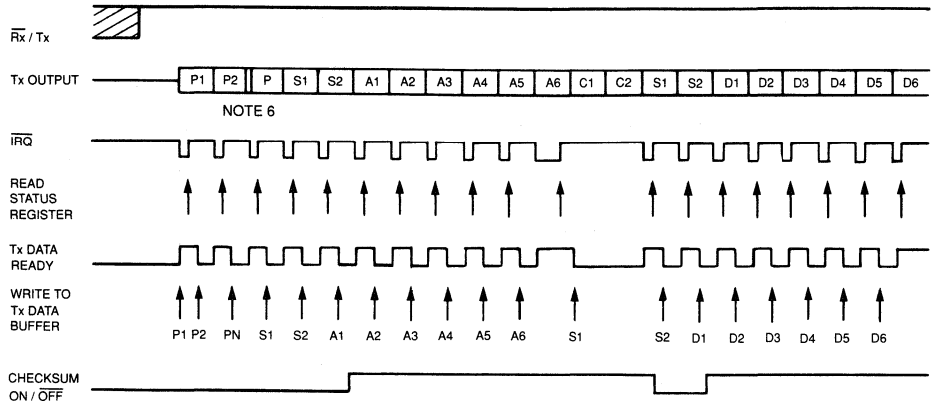


NOTES
1). The SYNC and SYNC detector searches the incoming bit stream starting at the end of the byte in which SYNC/SYNC prime was set.
2). After detection of a SYNC/SYNC word the SYNC/SYNC prime bits automatically go low (control bits 5 and 6: detector off).
3). The checksum checker is inhibited during the time SYNC/SYNC search is operating.
4). The status register will indicate whether SYNC or SYNC was detected here.
5). Any number of preamble bits can occur here.
6). Any number of bits can occur here.
7). Rx Freeformat set high.

Fig.5 Rx 1

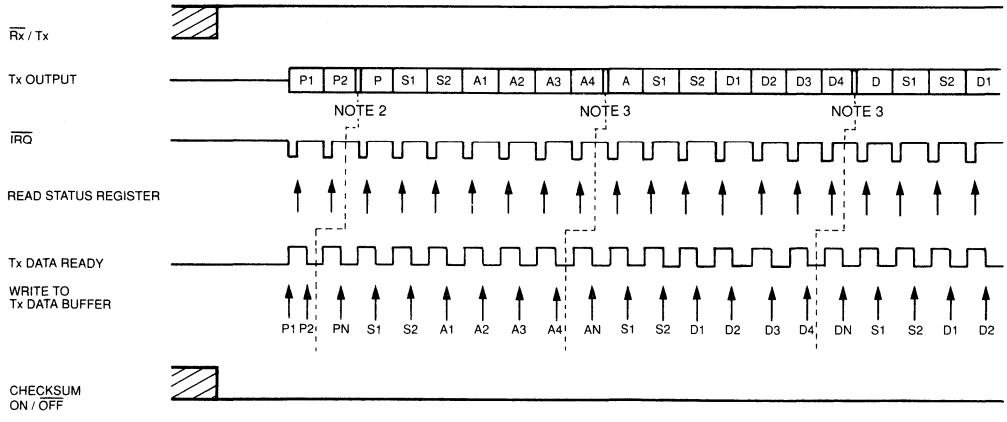
Tx Timing Information

(a) Tx MORE THAN ONE MESSAGE, SYNC BEFORE EVERY MESSAGE, Tx CHECKSUM ENABLED.



NOTES
1). Preamble and SYNC bytes are loaded as data from the µC.
2). The Tx output will be held at bias level when no data is being transmitted.
3). Tx byte synchronisation is established by the loading of the first preamble byte from the µC.
4). Checksum must be turned off during preamble and SYNC words.
5). When Rx/Tx is low Tx output is at bias.
6). Any number of preamble bytes can occur here.

(b) Tx MORE THAN ONE MESSAGE, Tx CHECKSUM NOT ENABLED.

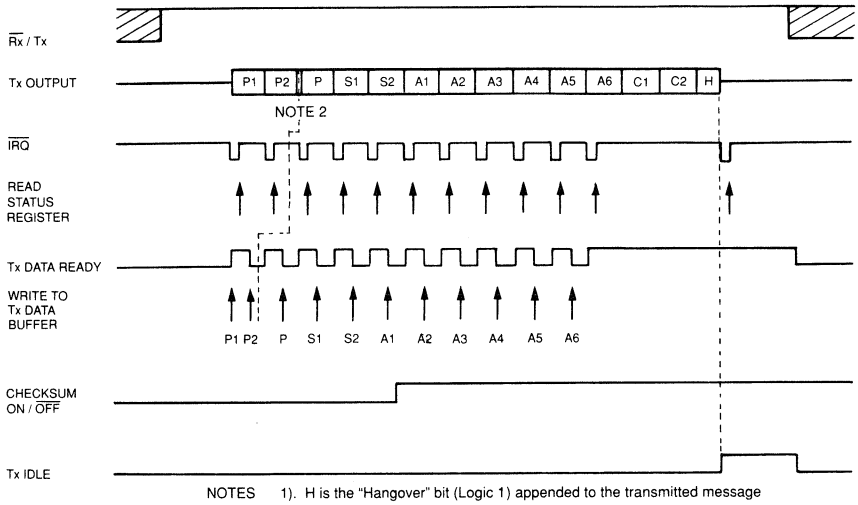


NOTES
1). Preamble, SYNC words and checksums are supplied by the µC in this format as data bytes.
2). Any number of preamble bytes can occur here.
3). Any number of address/data bytes can occur here.

Fig.6 Tx Timing

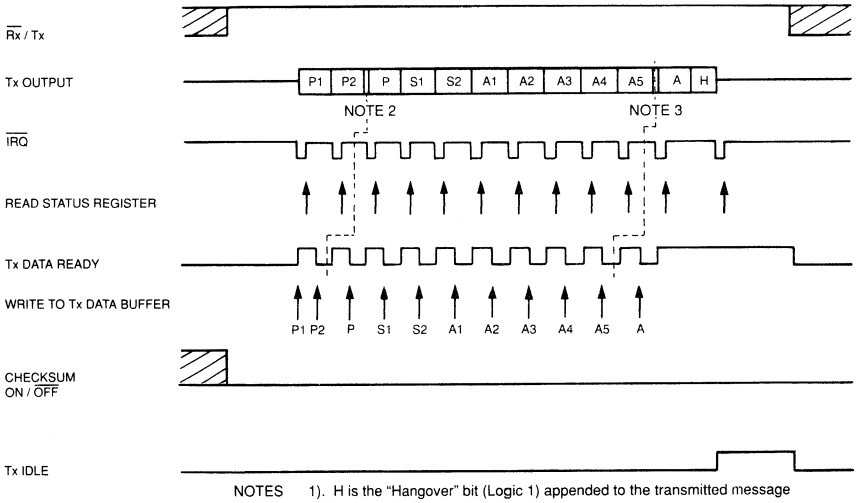
Tx Timing Information...

(a) Tx ONE MESSAGE, Tx CHECKSUM ENABLED.



NOTES
1). H is the "Hangover" bit (Logic 1) appended to the transmitted message before transmission is terminated.
2). Any number of preamble bytes can occur here.
3). Transmission terminates after C1, C2 and H. Termination occurs when no further data bytes are written to the Tx data buffer.

(b) Tx ONE MESSAGE, Tx CHECKSUM NOT ENABLED.



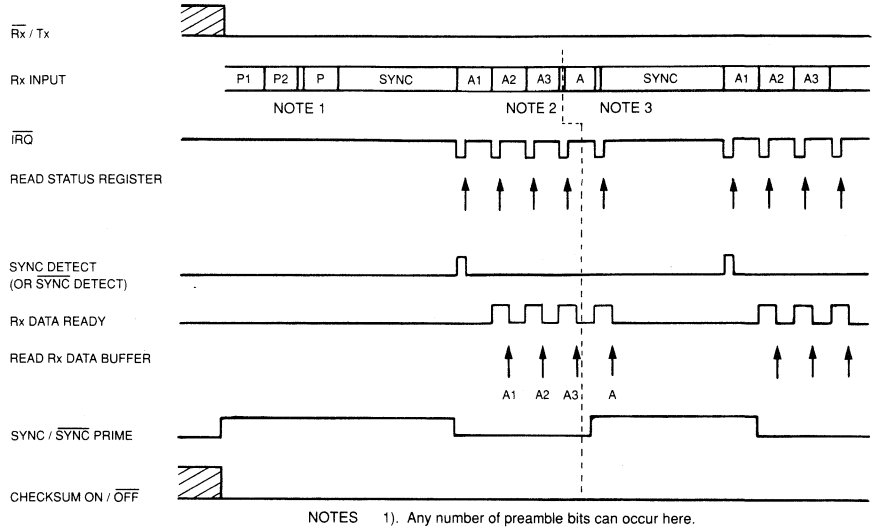
NOTES
1). H is the "Hangover" bit (Logic 1) appended to the transmitted message before transmission is terminated.
2). Any number of preamble bytes can occur here.
3). Any number of address/data bytes can occur here.
4). Transmission terminates when no more data bytes are loaded into the Tx data buffer.

NOTES
i). A – Address bytes.
ii). C – Checksum bytes.
iii). D – Data bytes.
iv). H – Hang bit.
v). P – Preamble bytes.
vi). Z – Don't care state.
vii). Tx only – In Tx, Preamble and SYNC are loaded as data from the microcontroller.

Fig.7 Tx Timing

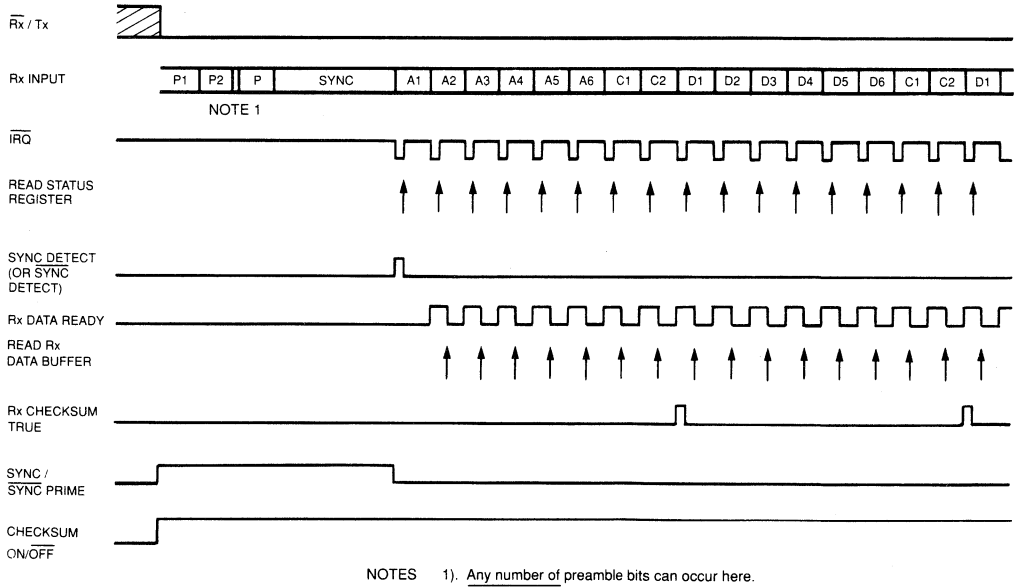
Rx Timing Information

(a) Rx SYNC/ $\overline{\text{SYNC}}$ REQUIRED BEFORE EVERY MESSAGE, Rx CHECKSUM NOT ENABLED.



NOTES
1). Any number of preamble bits can occur here.
2). Any number of address/data bytes can occur here.
3). Any number of bits can occur here.
4). Rx Freeformat set high.

(b) RX ADDITIONAL DATA FOLLOWS INITIAL ADDRESS (6 DATA & 2 CHECKSUM BYTES) DATA, RX CHECKSUM ENABLED.



NOTES
1). Any number of preamble bits can occur here.
2). Rx Freeformat set high.

NOTES
i). A – Address bytes.
ii). C – Checksum bytes.
iii). D – Data bytes.
iv). H – Hang bit.
v). P – Preamble bytes.
vi). Z – Don't care state.
vii). Tx only – In Tx, Preamble and SYNC are loaded as data from the microcontroller.

Fig.8 Rx Timing

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX809J**	-40°C to +85°C (cerdip)
	FX809LG/LS	-40°C to +85°C (plastic)
Storage temperature range:	**FX809J**	-55°C to +125°C (cerdip)
	FX809LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.032MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz.

Bit Rate = 1200bp/s.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Enabled		–	5.0	–	mA
Powersave		–	2.0	–	mA
Dynamic Values					
Digital Interface					
Input Logic "1"	1	3.5	–	–	V
Input Logic "0"	1	–	–	1.5	V
Output Logic "1" (IOH = -120µA)	2	4.6	–	–	V
Output Logic "0" (IOL = 360µA)	2, 3	–	–	0.4	V
Digital Input Current					
V_{IN} = Logic "1" or "0"	1	–	–	1.0	µA
Digital Input Capacitance	1	–	–	7.5	pF
Tri-state "Off" Leakage Current	8	-4.0	–	4.0	µA
Analogue Impedances					
Rx Input		100	–	–	kΩ
Tx Output					
Transmitting Data		–	6.0	10.0	kΩ
Not Transmitting Data		–	1.0	–	MΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}		5.0	–	15.0	kΩ
Gain		–	15.0	–	dB
Frequency	4	–	4.032	–	MHz
Receiver					
Signal Input Levels	5	-9.0	-2.0	10.5	dB
Bit Error Rate					
at 12dB SNR		–	7.0	–	10^{-4}
at 20dB SNR		–	1.0	–	10^{-8}
Synchronization at 12dB SNR	6				
Probability of Bit 8 being correct		–	99.0	–	%
Probability of Bit 16 beng correct		–	99.5	–	%

Specification...

Characteristics	See Note	Min.	Typ.	Max.	Unit
Dynamic Values					
Transmitter					
Output Level		–	0	–	dB
Output Level Variation		-1.0	–	1.0	dB
Output Distortion		–	3.0	5.0	%
3rd Harmonic Distortion		–	2.0	3.0	%
Logic "1" Frequency	7	–	1200	–	Hz
Logic "0" Frequency	7	–	1800	–	Hz
Isochronous Distortion					
1200Hz – 1800Hz		–	25.0	40.0	µs
1800Hz – 1200Hz		–	20.0	40.0	µs
Uncommitted Amplifier					
Bandwidth		–	200	–	kHz
Gain		–	50.0	–	dB
Input Impedance		1.0	–	–	MΩ
Output Impedance		–	–	10.0	kΩ

Notes

1. Device control pins; Serial Clock, Command Data, $\overline{\text{Wake}}$ and $\overline{\text{CS}}$.
2. $\overline{\text{Reply}}$ Data output.
3. $\overline{\text{IRQ}}$ output.
4. For baud rate specified (1200 baud).
5. Signal-to-Noise Ratio = 50dB.
6. The response time is measured using a 10101010.....101 signal input pattern at 230mVrms (-2.5dB) with no noise.
7. $\overline{\text{Dependant}}$ upon Xtal tolerance.
8. $\overline{\text{IRQ}}$ and Reply Data outputs, for $V_{SS} < V_{OUT} < V_{DD}$.

Generation

The checksum generator takes the 48 bits from the 6 bytes loaded into the Tx Data Buffer and divides them modulo–2, by the generating polynomial;-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted).
This 16–bit word is used as the "Checksum."

Checking

The checksum checker does two things:
It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo–2, by the generating polynomial;-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

The 15 bits remaining in the polynomial divider are checked for all zero.
Secondly, it generates an EVEN parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64).
If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the Rx Checksum True bit (Status Register bit-1) is set.

Package Outlines

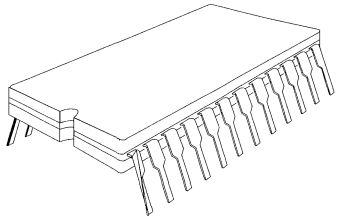
The FX809 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX809 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX809J 24-pin cerdip DIL (J4)

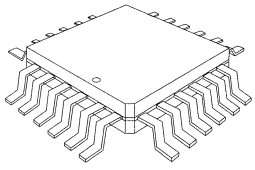
NOT TO SCALE



Max. Body Length 32.03mm
Max. Body Width 14.81mm

FX809LG 24-pin quad plastic encapsulated bent and cropped (L1)

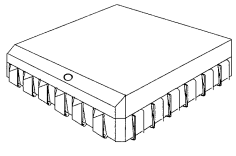
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX809LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX809J	24-pin cerdip DIL	(J4)
FX809LG	24-pin encapsulated bent and cropped	(L1)
FX809LS	24-lead plastic leaded chip carrier	(L2)

CML Semiconductor Products

PRODUCT INFORMATION

CM10 Base Station Signalling Controller -*Computer Card*

Publication D/10/1 July 1994
Provisional Issue

Features

- PC Expansion Card -Total Base Station Control by PC
- PMR Base Station Applications
- 5/6-Tone Selcall Encode/Decode - All Recognised Tonesets
- 2-Tone Encode
- 1200 Baud FFSK Encode/Decode
- Morse Station ID Output
- Separate Rx/Tx Tone, Data and Voice Paths
- Data and Signalling Loaded From Host Computer
- Received Data and Signalling Loaded To Host Computer
- On-Board PTT Control

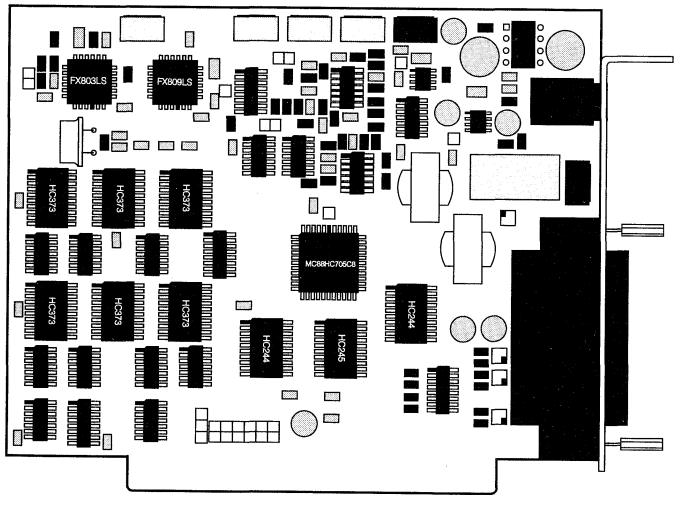


Fig.1 The CM10 Computer Card

CM10

The CM10

Computer-aided PMR signalling requires specialized applications software, a CM10 'N'-Tone Encoder/Decoder and Selcall equipped 2-way radios.

No two systems are ever alike, but hardware like the CM10 remains a common denominator. Most systems are uniquely configurable according user requirements. PMR systems may "oversee" large fleets comprising hundreds of remote units or the smaller "Base + 5" installation for a modern office or in-plant talk-back paging system.

The CM10's role in a communications signalling system is to handle all the non-verbal signals used to call or address radio units selectively, and to decode status reports from fleet units or other remote stations. Data generated by the host PC commands the CM10, which in turn controls a base station radio. Conversely, remotely (mobile/portable) originated data collected by the CM10 is downloaded to the PC for processing, storage and display.

For Example:

ANI equipped radios key-up a digital stream of data to:

a. Identify each unit with a discrete address-code,
b. Add a suffix indicative of a unit's status: "out of service," "on-site" etc.,
c. Report "man-down" alarms or general operating problems.

Selcall equipped radios can be addressed even unattended, and the HORN sounded to get attention. Voice Storage/Retrieval systems may be added to extract verbal reports and dispatch new tasks without interference to productive activity.

CM1481 equipped fleets can be called, controlled, reprogrammed, stunned or enabled as according to current tactical and strategic requirements. Calls can be logged and alarms output to the relevant authority.

The CM10 is supplied as a convenient PC "half-card" for insertion directly into the host's expansion slot.

Description

The CM10 plugs-in to an IBM PC's (or clone's) expansion slot. External connections control an associated 2-way radio, keying the transmitter and monitoring receive audio for signal traffic. For optimum operation both microphone and receive audio may be routed through the CM10, assuring that speech and tones don't collide or interfere with each other. Alternatively the CM10 may be used to control the audio section of a local base station. Morse code station callsigns are transmitted automatically. A Transmitter Time-Out timer, independent of any computer control, times-out the PTT key to prevent inadvertent lock-up of the RF system. Four programmable function I/O ports allow local sensing and control of external devices; i.e. "man-down", claxon drive, door-ajar or Tower Lamp failure. Two CM10 units can share the same host computer, each controlling separate base station radio systems.

Tone Signalling Formats

The CM10 may be programmed for the following tone signalling formats using the supplied PC software:

HSC-CCIR	**GE Type 99***
HSC-EEA	**Motorola Quick Call II****
HSC-USA	

A custom tone set may be created using the CM10's Tone Pallette feature.

**GE Type 99 is a trademark of General Electric Corp.*
***Quick Call II is a trademark of Motorola, Inc.*

System Set-Up

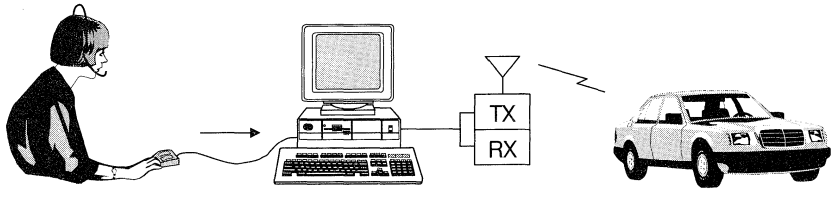


Fig.2 Typical System Set-Up of the CM10

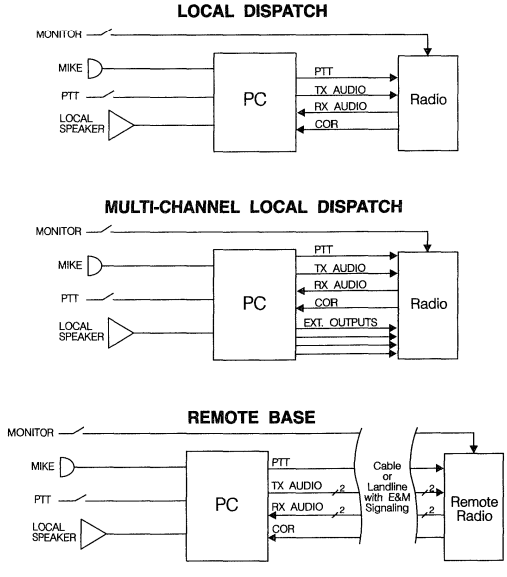


Fig.3 Set-Up Options for Remote, Multi-Channel and Local Dispatch

Operation

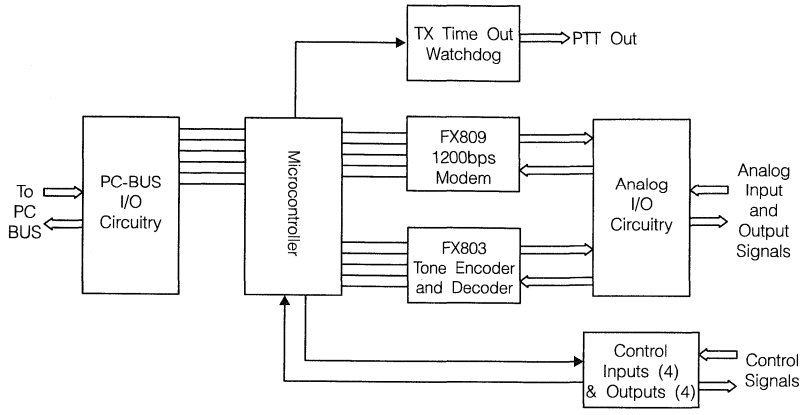


Fig.4 Functional Block Diagram

HSC Decode Mode

To decode, the CM10 monitors the receive audio input for tones. Upon detection of a valid tone of the correct duration and frequency (in the programmed toneset), data is placed in a receive buffer. An interrupt is set, flagging the PC according to the configuration requirements.

The flag or interrupt is cleared by the application software reading the buffer. The CM10 will continue decoding tone sequences and placing them into the receive buffer up to its capacity of forty digits. If the forty-digit limit is reached without the host computer reading the digits, a receive buffer overflow flag is set, and decoding will be discontinued until the buffer has space again. Once the buffer has available storage, the overflow flag is cleared and decoding will resume.

HSC Encode Mode

To transmit a Selcall burst, the application software assembles the required string of address and command digits and transfers this string to the CM10's Tx buffer. Depending on the CM10's configuration, one of the following will then take place:

If there is an RF carrier present, i.e. the channel is busy, and the carrier lock out has been enabled, the CM10 will "standby" until the RF channel is available.

Detect an of 'Idle' state keys PTT and transmits the buffer.

If the application software has enabled the "Auto-Send on PTT" bit, the information in the transmit buffer will be transmitted when the PTT button is pressed.

This will happen each time PTT is pressed.

2-Tone Encode Mode

To transmit a 2-Tone burst, the application software puts together the required address digits and, using the CM10 software driver, transfers them to the CM10's Tx buffer. Depending on the CM10's configuration, one of the following processes will then take place:

If there is an RF carrier present and the carrier lock out has been enabled, the CM10 goes into "standby" until the RF channel is available.

If the application software has enabled the "Auto Send on PTT" bit, the information in the transmit buffer will be transmitted when the PTT button is pressed.

This will occur only the first time PTT is pressed after loading the information to the CM10.

Telemote Operation

Telemote operation allows a remote transmitter to be controlled over radio or multiplexed (non-metalliic) links. It is enabled by installing a jumper on E8, and by the configuration software.

The CM10 provides a software choice of dc (logic) or tone (Telemote) transmitter control.

Tone control, popularly known as Telemote operation, employs a momentary "select" tone and continuous PTT "maintenance" tone of 2175Hz attenuated by a notch filter in the associated base station.

After set-up, Telemote operation will occur every time PTT is pressed. Telemote operation is disabled via software.

See the CM10 Installation Guide for details.

Operation...

MSK Operation

The CM10 sends and receives synchronous Medium Shift Keying (MSK) 1200 baud data, and provides checksum generation and error checking in accordance with the MPT1327 standard.

The CM10 uses the MPT1327 protocol's proven packet data format. This format provides for selective calling and for transmitting alphanumeric messages of limited length over conventional, half-duplex 2-way radio channels. Trunking operation is not within the scope of the sotware provided.

The CM10 has separate Rx and Tx buffers or registers, each able to store twenty bytes of data (160 bits). Switching from Rx to Tx in MSK mode is accomplished using the CM10's Rx and Tx Enable commands. The transmitter is automatically disabled when the receiver is enabled and vice versa. This differs from the HSC mode, in which the Rx and Tx operations are full-duplex.

"MPT1327, A Signalling Standard for Trunked Private Land Mobile Radio Systems" is published in the UK by the Department of Trade and Industry.

Hardware

Level Controls

The CM10 has seven level controls, six of which are on the top edge of the card. This placement of the controls allows simple adjustments to be made after the CM10 has been installed in the computer. The speaker level (volume control) is on the rear of the card just above the radio interface connector. It is accessible when the computer cover is installed.

Control	Description
Tone Deviation	Sets the tone level to the transmit audio output port.
MSK Deviation	Sets the MSK deviation level to the transmit audio output port.
Tx Time Out Timer	This control allows the user to set the timer between 10 seconds and 180 seconds. It is independent of the PC and microprocessor on the card as serves as a safeguard against the transmitter being keyed for long periods.
Microphone Mix	Sets the microphone level to the tape output.
Microphone Deviation	Sets the level of the microphone audio at the CM10's transmitter audio output pins (Tx mic. input).
Microphone Gain	Sets the gain between the microphone input and output pins.
Speaker Level	Sets the level at the external speaker. It is adjustable from the rear edge of the card just above the radio interface connector (max. rating: 500 mW into 8Ω).

Jumper Table

The following table shows effects on signals by the CM10's jumpers.

Jumper	Description
E1	This two-position jumper selects PC Port I/O Address of $200 or $300. This jumper is factory-installed to select address $200. To change it, remove the jumper on positions 1-2 and install a jumper on positions 2-3.
E2	Enables PC Interrupt IRQ2 when installed.
E3	Enables PC Interrupt IRQ3 when installed.
E4	Enables PC Interrupt IRQ4 when installed.
E5	Enables PC Interrupt IRQ5 when installed.
E6	Enables PC Interrupt IRQ6 when installed.
E7	Enables PC Interrupt IRQ7 when installed.
	Supplied for use with custom software Not used with the CM10 Software provided
E8	Factory-installed. Tonemote Jumper - *Remove for Tonemote operation only*
E9	Enables microphone audio to the tape output. This jumper is factory-installed.
E10	Enables the transmitter timeout timer. This jumper is factory-installed.
E11	Selects Rx and Tx audio in half-duplex mode when installed (operation is full duplex when E11 is open).

Hardware...

Radio/Microphone Interface

The CM10 will accept PTT control and a microphone audio input at the local dispatching area. Working with application software, it will provide a simple dispatch system for both the small and the large fleet user.

Pin	Function	Description
1,14	Rx Audio In	Balanced receiver audio input.
2	Rx Audio In	Unbalanced receiver audio input.
3	Tx Audio In	Microphone input.
4	Tape	Low-level receiver and transmitter audio output to tape.
5,18	Tx Audio Out	Balanced transmitter audio output. With jumper E11, half duplex Tx and Rx audio can be directly coupled to this connection.
6,7,19	PTT Out	Keying relay, pin 6 common, pin 7 (normally closed), pin 19 (normally open).
8	PTT Input	This is the PTT signal originated by the operator.
9	Mic. Audio	Buffered and amplified microphone output.
10,11, 12,13	AuxiliaryOutputs	These are auxiliary open collector outputs to allow control of external devices such as radio channel selection, power level, recorder enable, etc. The minimum active low voltage is 0.7Vd.c., as this is a cascade driver (if an application requires a lower minimum, an external transistor switch circuit may be added -- see the CM10 User Manual for details).
15,16,17	GND	Audio signal ground.
20	Mic Mute	This signal is an indication that the microphone is being muted for a tone data burst.
21	COR	This signal, supplied by the radio's busy or noise squelch signal, indicates to the CM10 the presence of an RF carrier.
22,23 24,25	Auxiliary Inputs	These inputs allow external devices to have signalling inputs to the PC.

PC Interface

The PC uses I/O base address $200 or $300 to pass HSC characters (representing tones) to and from the CM10. The TX Buffer holds one HSC character from the PC until the CM10's microprocessor stores it in its internal data buffer. The RX Buffer Latch holds one character from the CM10's microprocessor internal RX buffer until the PC reads it.

The following I/O addresses and card registers are used to exchange information between the CM10 and the computer bus:

Address	R/W	Description
$300	WRITE	Tx LATCH (one tone character is buffered for sending to the CM10's μP).
$300	READ	Rx LATCH (one tone character is buffered for sending to the PC).
$301	WRITE	CM10 COMMAND DATA LATCH (buffers a configuration byte to the CM10).
$301	READ	PC COMMAND DATA LATCH (latched buffer which provides status on CM10 configuration as requested by the PC).
$302	WRITE	CM10 COMMAND REGISTER (buffers a command information byte to the CM10).
$302	READ	CM10 STATUS BUFFER (provides real time status of CM10 buffers).

Software

The following software is supplied with the CM10:

1) A configuration program that allows you to setup, confirm operation and initialize the personality settings of the CM10.

2) An autoload program that allows the configuration settings to be loaded into the CM10 when the computer is booted up.

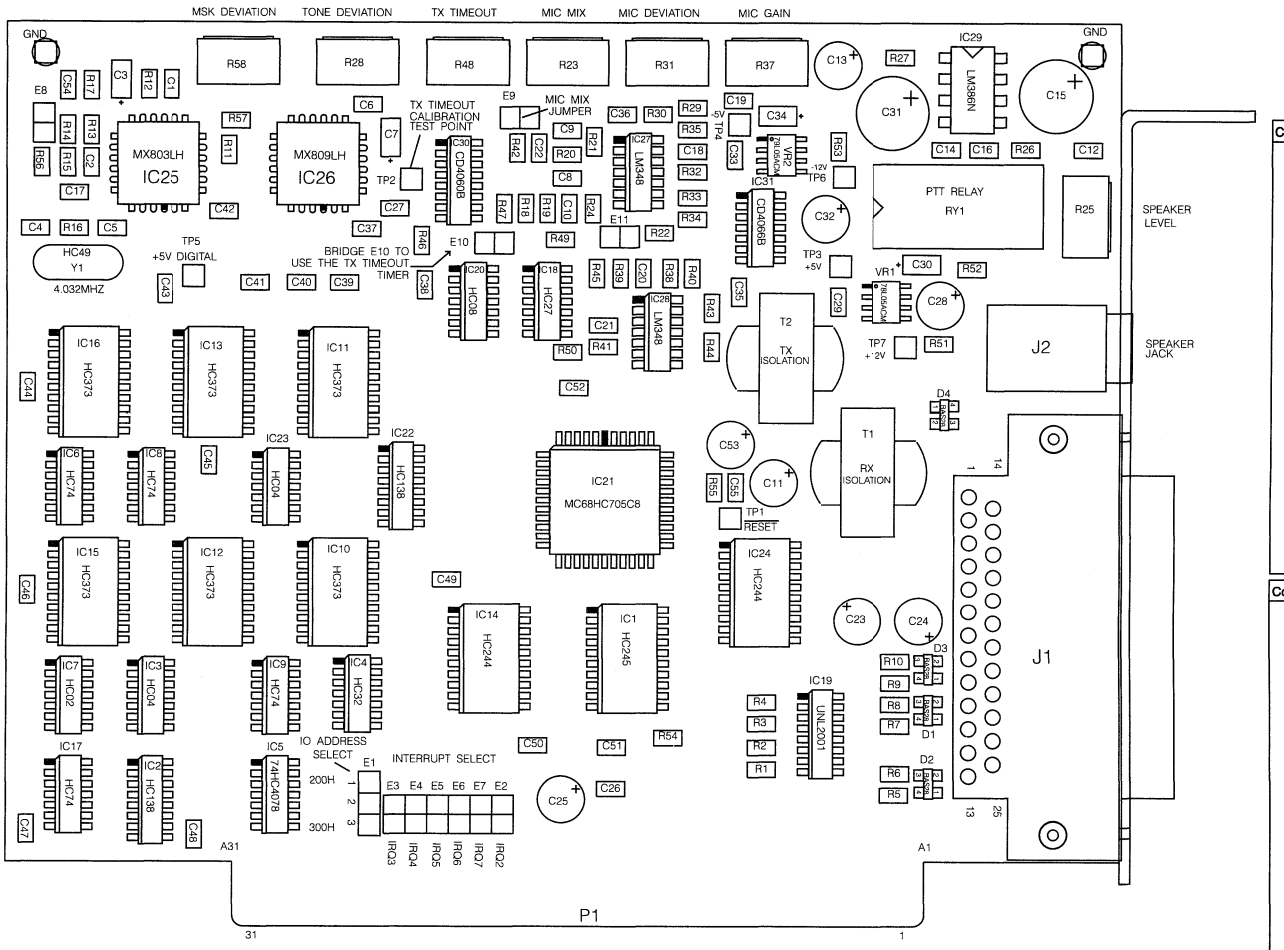
3) A software driver that provides an CM10 interface similar to that of a printer.

4) Examples of CM10 control using Pascal.

Set-up Options

The following commands and parameters are used to establish the operating parameters of the card. These same configuration options may be accessed by user defined software. (See the CM10 User Manual for more information.)

Enable/Disable Tx Buffer	Buffers up to 40 digits of HSC signalling (20 bytes of MSK).
Enable/Disable Rx Buffer	Buffers up to 40 digits of HSC information for the transmitter (20 bytes of MSK).
Clear Rx or Tx Buffers	Clears entire Rx or Tx Buffer.
Send Morse Code ID	Causes the information in the morse code buffer to be transmitted.
Clear ID Buffer	Clears the information stored in the card's morse code ID buffer.
Warm Start the Card	Allows a card reset without destroying the information in any of the registers.
Halt/Resume Operation	Halts or resumes tone signalling processing.
Enable/Disable PTT	Controls the effect of the PTT input.
Test Tone On/Off	Enable/disable a user frequency programmable tone test generator.
Set Pre/Post Tx Delay	Allows the pre-transmission and post transmission delays to be set.
Morse Code ID	Reads or loads the eight ID characters.
ID Time Period	Reads or loads the transmit time interval for station ID.
ID Tone Frequency	Reads or sets the frequency of the tone generator for the Morse Code ID function.
Tone Signalling Format	Reads or sets the tone signalling format.
Custom Tone Duration	Reads or writes the tone duration for the custom tone set. If in a standard tone set, read the duration specified.
Custom Tone Table	Reads and writes to the custom tone table over a frequency range of 448Hz to 3000 Hz.
Auxilliary I/O	Reads the four auxilliary inputs or set the four auxilliary outputs.
PC Interrupt Handling	Reads or sets the two PC interrupt masks, one mask for external I/O functions and the other, miscellaneous functions for tone, MSK and I/O functions. The interrupt must then be hardware programmed to the selected point (IRQ2 through IRQ7), using the hardware jumpers on the CM10.
I/O Definitions	Reads and writes to the I/O sense register. This is the register which determines if the input or output is active high or low.
Auxilliary Status Register	Read the Auxilliary Status register.



Component	Value
R1-11	10K
R12	1M
R13	62K
R14	620K
R15	62K
R16	1M
R17	20K
R18	560
R19-21	100K
R22	68K
R23	500K
R24	68K
R25	10K
R26	10
R27	620
R28	500K
R29	16K
R30	120K
R31	100K
R32	120K
R33-34	10K
R35	620
R37	200K
R38	16K
R39	180K
R40-41	20K
R42	13K
R43-44	10K
R45	100K
R46-47	10K
R48	500K
R49-50	10K
R51	100
R52	10
R53	100
R54	10K
R55	100K
R56	68K
R57	20K
R58	500K

Component	Value
C1	.1UF
C2	330PF
C3	1UF
C4-5	33PF
C6	.1UF
C7	1UF
C8	.1UF
C9	100PF
C10	330UF
C11	4.7UF
C12	.1UF
C13	10UF
C14	.1UF
C15	100UF
C16	.047UF
C17	.1UF
C18	100PF
C19	.1UF
C20-21	100PF
C22	.1UF
C23-24	4.7UF
C25	10UF
C26	.1UF
C27	.047UF
C28	10UF
C29	.1UF
C30	1UF
C31	100UF
C32	10UF
C33	.1UF
C34	1UF
C35-52	.1UF
C53	4.7UF
C54-55	.1UF

Fig.5 Component Location Guide

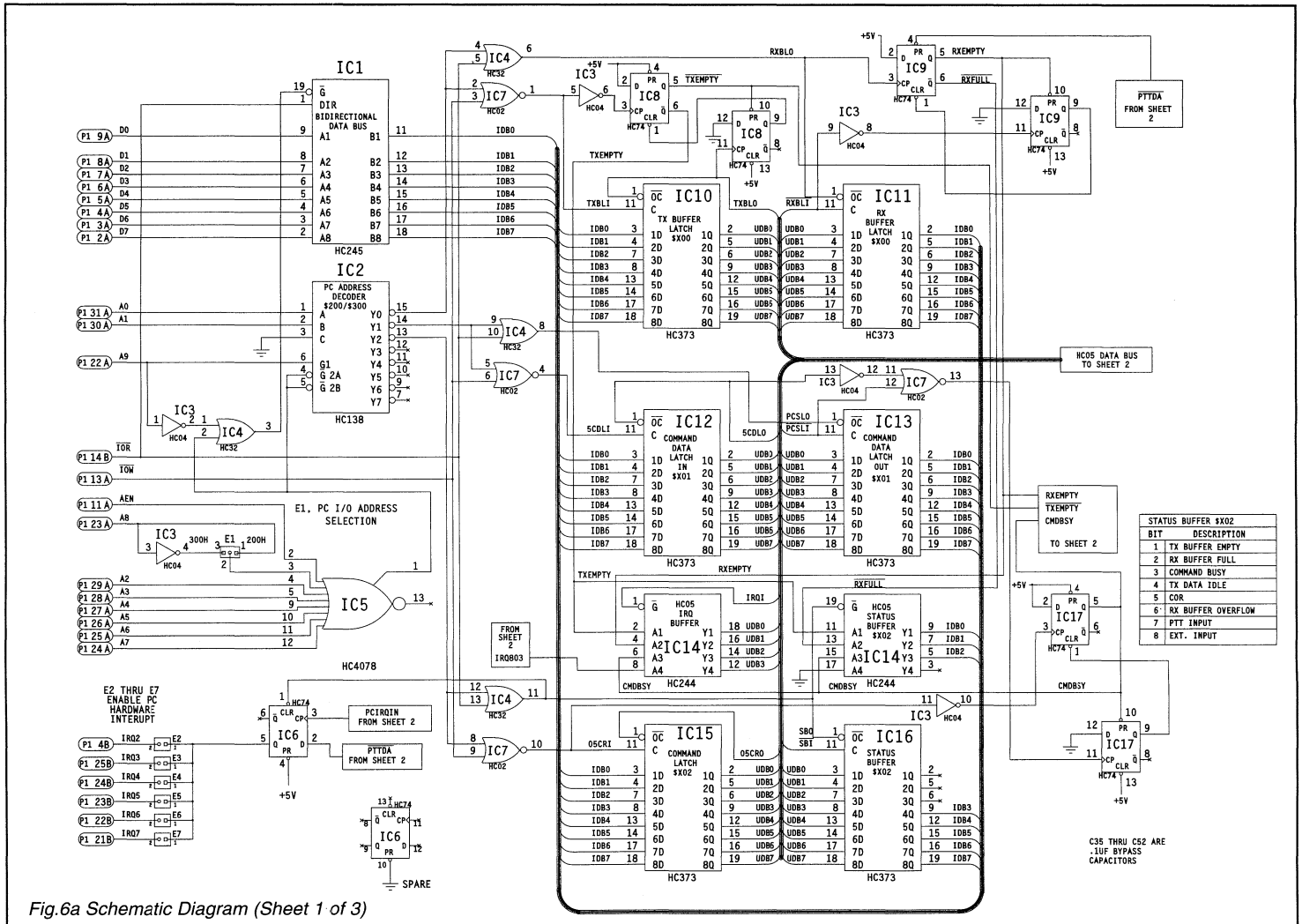


Fig.6a Schematic Diagram (Sheet 1 of 3)

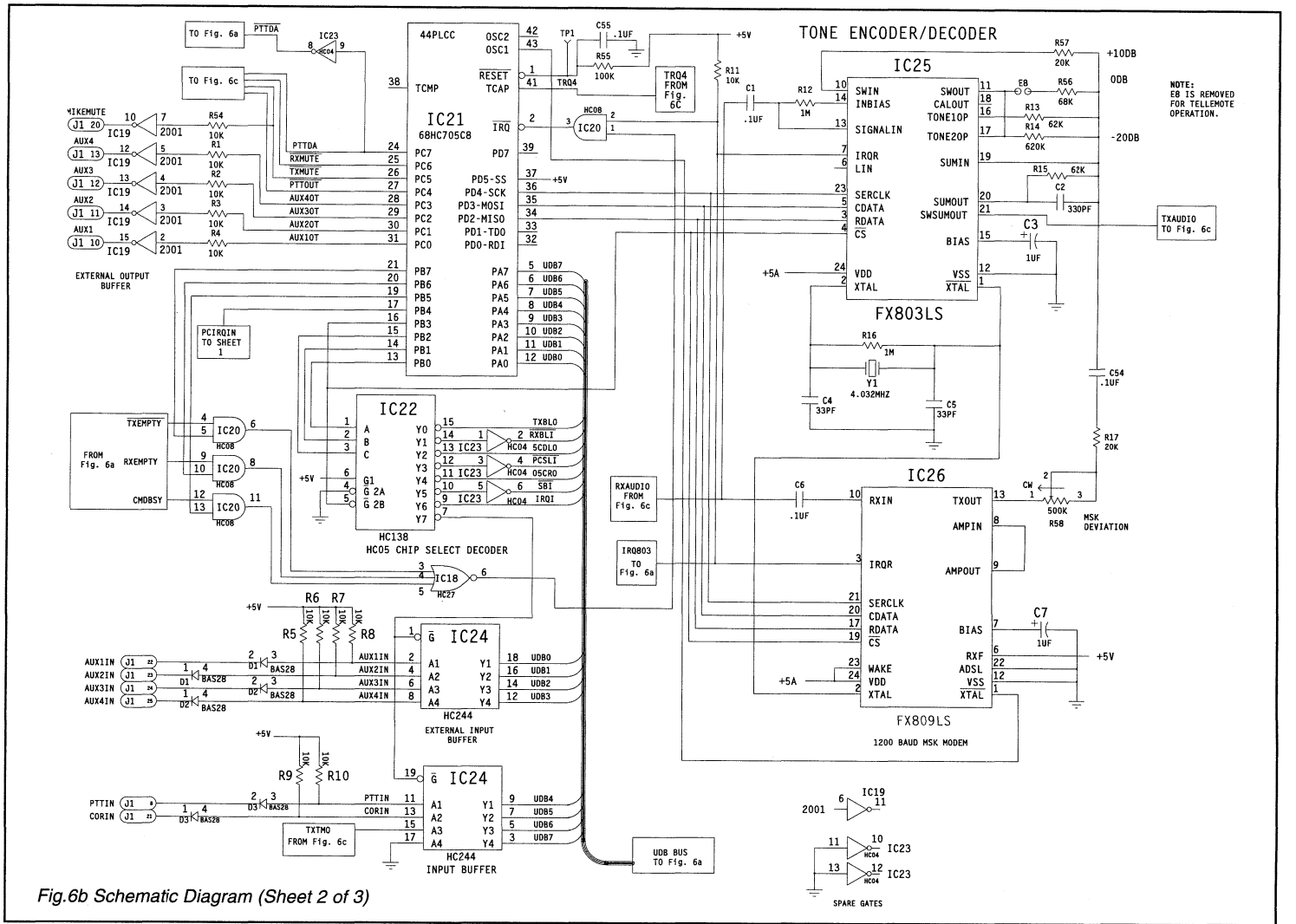


Fig.6b Schematic Diagram (Sheet 2 of 3)

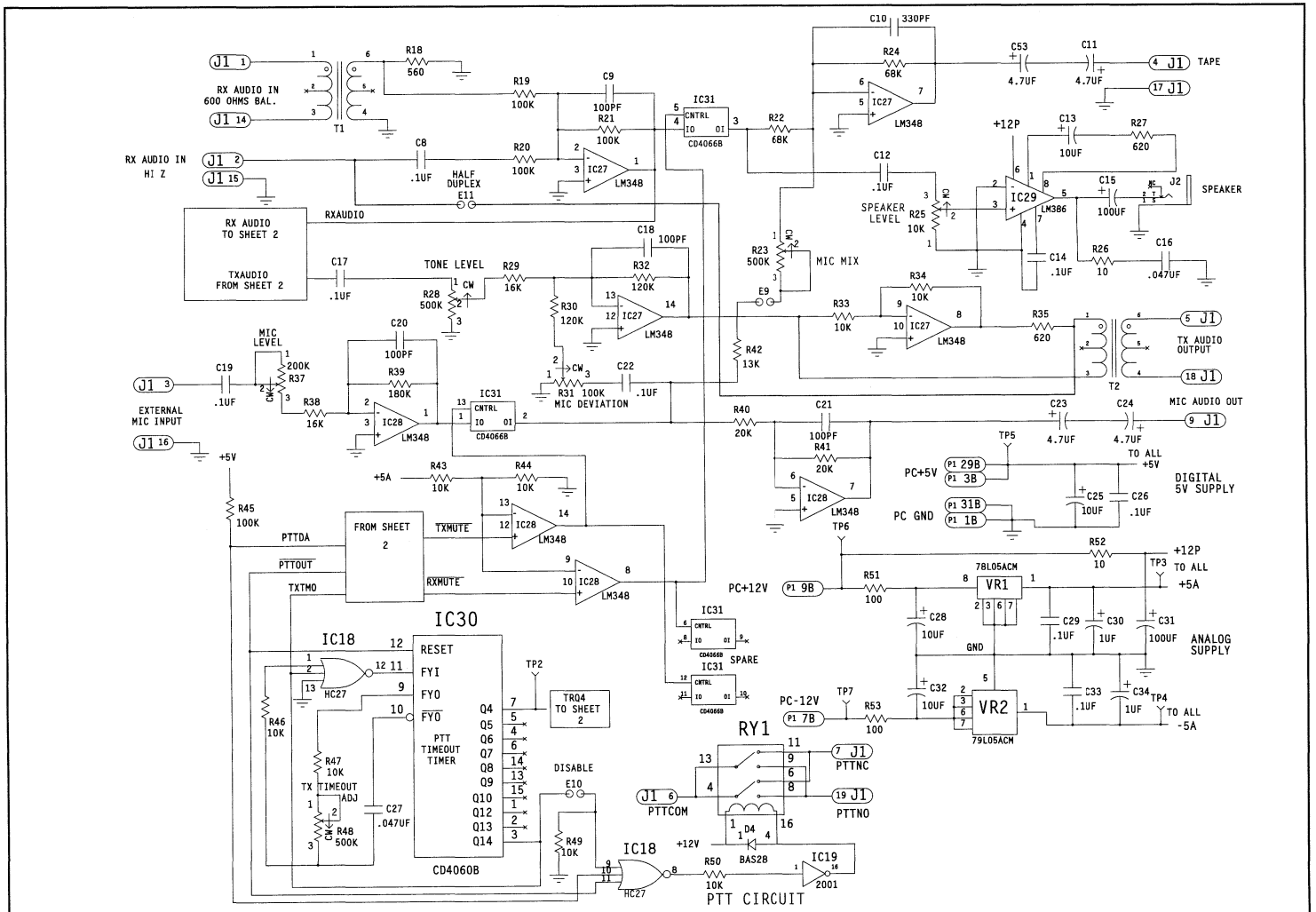


Fig.6c - Schematic Diagram (Sheet 3 of 3)

Specifications

Absolute Maximum Ratings:

		Min	Max	Units
PC Supply Voltages	+12	8.0	14.0	V
	-12	-8.0	-14.0	V
	+5	4.8	5.2	V
Voltage on COR, PTT, and Aux inputs		-0.3	50.0	V
Voltage on External Digital Outputs			50.0	V
Voltage on unbal. Analog Input		-25	+25	V
Storage Temperature		0	+85	°C
Operating Temperature		0	+50	°C

Measurement Conditions:

All characteristics were measured under the following conditions unless otherwise indicated:

T_{AMB} = 25°C

DC voltages +12,-12, and +5 V_{DC} (derived from the PC Bus)

0dBm = 774.6 mVrms, 600 Ω

Characteristics

PC Current Loading

Supply Current at 12 V_{DC} is typically 200mA.
At -12 V_{DC} it is typically 20mA.
At +5 V_{DC} it is typically 100mA.
Current is measured at the PC bus connector by inserting a current meter in line with the pins from the PC bus supplying voltage to the CM10.
Max. Switching Capacity of PTTOUT is typically 1000mA (Floating Dry form C contact), 200 V_{DC}.
Sink Current at Mic Enable and the Auxiliary Outputs is typically 100mA.

Logic Voltages

Input Low Voltage at COR, PTTIN & Aux Inputs is 1.8V max. (with a 10kΩ pullup resistor).

Input High Voltage at COR, PTTIN & Aux Inputs is 4.1V min. (with a 10kΩ pullup resistor).

Maximum Input Voltage to COR, PTTIN and Aux Inputs is 50 V.

TX Time Out Timer range is 10 to 180sec. [clockwise to increase].

Audio Levels

Rx Audio Input Level range is 0.05 to 1.0 Vrms.

Speaker Audio Output Level is from 0.0 to 2.0 Vrms (Under 8Ω resistive load.)

Audio Output Level (Tx Out) to Radio Transmitter is from 0.0 to 1.0Vrms with a 600 Ω load.

The Rx/Tx Monitor is adjustable, usually set at 0dB gain with respect to Tx Out.

Microphone Audio Out ranges from -1.5dB to 18dB of gain to Tx Out with a 600Ω load.

Impedances

Rx Input, Balanced, is 600Ω (typ). Unbalanced, it is 10kΩ (min). Microphone Input is 15kΩ (min).

Tx Output, Balanced, is 600Ω (typ).

Mic. Output is 200Ω (max). Rx/Tx Monitor Output is 200Ω (max).

Tone Encoder

Distortion is 5% max. (600Ω load at Tx Out).
Duration is ±0.5ms.
Period Error is 1µs max.

Decode Sensitivity SNR

Sensitivity measurement is based on decode of a 5-tone set with Signal Level = 45mV, Noise bandwidth = 5.0kHz Band-Limited Gaussian.
Probability of detection = 96%.

HSC/CCIR: 0dB min.

HSC/EEA: 0dB min.

HSC/USA: 6dB min.

MSK Modem

MSK Decoder Bit Error Rate (12dB Sinad) is 7 x 10^{-4} max.

MSK Encoder Tone Distortion is 3% max. Encoder "0" Frequency is 1200Hz max. Encoder "1" Frequency is 1800Hz max.

Isochronous Distortion 0 to 1 is 40µs max.
Isochronous Distortion 1 to 0 is 40µs max.

Ordering Information

CM10 **Base Station Signalling Controller**

[Computer Card + Operating Software]

CML Semiconductor Products

PRODUCT INFORMATION

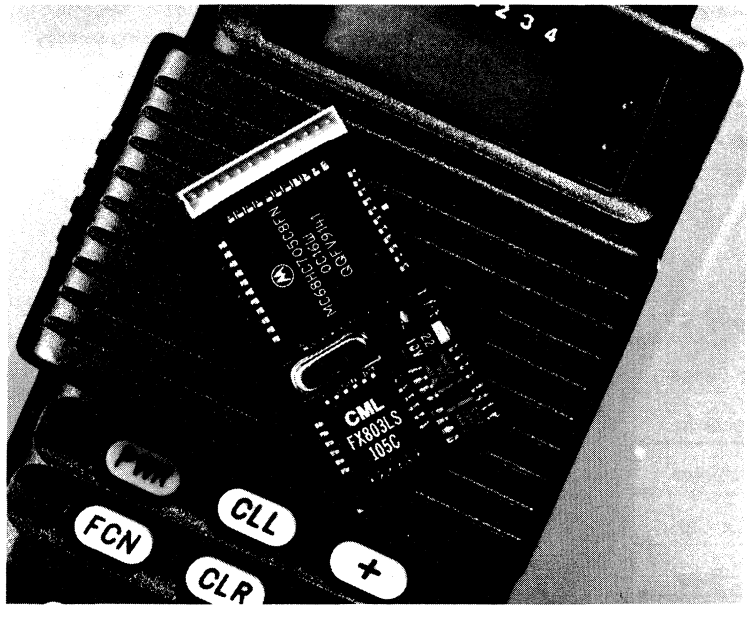
CM1481 Non-Predictive Selcall Module

Publication Adv/1481/2 February 1993
Advance Information

Applications

- Selcall in Two-Way Radio
- Alarm Systems
- Remote Control/Switching
- 'SECURE' Control and Switching
- Industrial Control
- Automatic User Identification

★ *'N'-TONE SELCALL ENCODING & NON-PREDICTIVE DECODING + GROUP CALLING* ★



CM1481

Module actual size is
45mm x 22mm x 8mm

Features

★ **Encoding and Non-Predictive All-Tone Decoding**

★ **All-System Group-Call**

★ **Transponding and ANI**

★ **Over-Air *"Stun" and "Release", "Re-Configuration" and "Reset"***

★ **PTT Lockout**

★ **Low-Power Requirement (4.0mA @ 6V to 26V D.C.** [typ])

★ **CCIR, EEA and ZVEI Tonesets**

★ **Simple, Serial Configuration**

★ **PTT Time-Out Timer**

★ **Multiple Coded Audio Alerts**

'Typical' power is specified with reference to operating periods of: 10% Tx, 10% Rx and 80% standby; No loading.

CM1481 - An Introduction

CM1481

A compact 5- or 6-Tone CCIR, EEA and ZVEI Selcall module with individual address encoding, non-predictive all-tone decoding, transponding and full, all-system group-call and ANI capabilities.

In addition to normal Selective Call facilities, the CM1481 offers, ***As Standard .....***

Over-Air — "Stun" and "Release" - Allowing base control in respect of disabling an addressed unit remotely due to theft, unpaid fees or air misuse/abuse!

Over-Air — "Address/Mode Re-Configuration" - Rapid, remote address and mode re-configuration - allowing unit participation in an alternative working group.

Over-Air — "Reset" - The base will call, and on completion of the transaction, may reset the unit, remotely, without operator intervention.

The CM1481 has a low-power requirement of 4.0mA (typ) at supply inputs between 6 and 26 volts d.c.

Typical' power is specified with reference to operating periods of: 10% Tx, 10% Rx and 80% standby. No loading.

The CM1481 is completely software configured, and as such, requires no internal links or switches.

Initial configuration of all module parameters is via a simple serial link to the on-board µController from the printer port of a "PC" or compatible computer employing the menu-driven software provided.
Parameter variations available are described in the table on the Back Page of this document.

Major inputs and outputs can be software configured to active "high" or "low" levels.

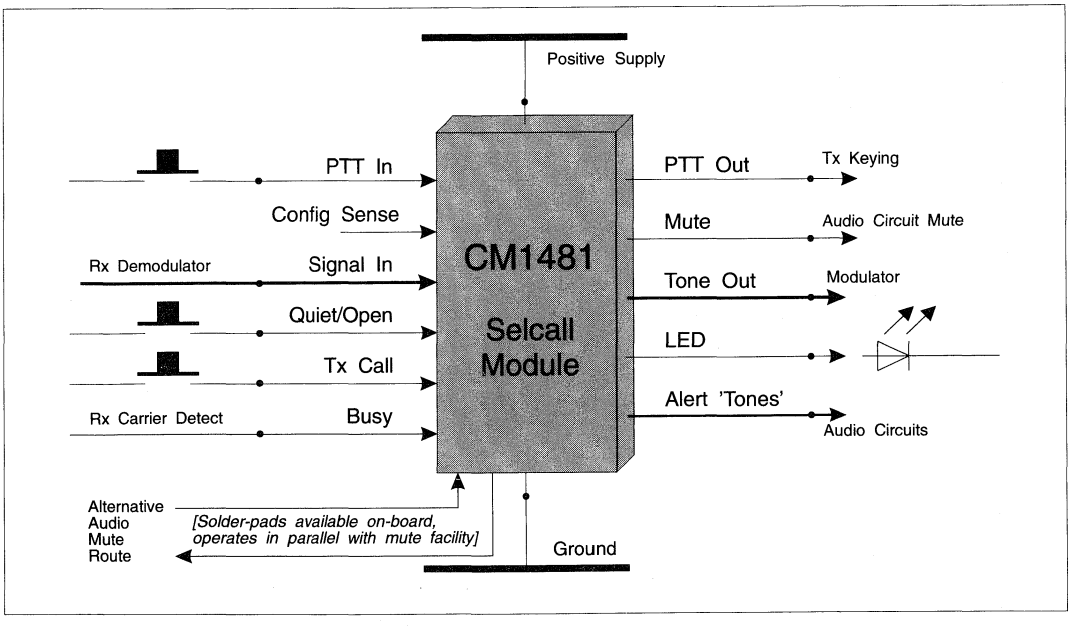
The supplied Configuration software and the CM1481 have the added ability, with a radio Tx/Rx, to originate and progress Over-Air operations from a PC terminal; this includes supplying security checks

Selective Call activity is indicated by multiple coded audio alerts; an LED drive output is available.

Applications Include

Selcall in Two-Way Radio systems
Alarms
Remote Control via radio or wire requiring security and noise immunity.

CM1481 - The Radio Interface - connection of the CM1481 to a radio unit is via a simple 13-pin radio interface.

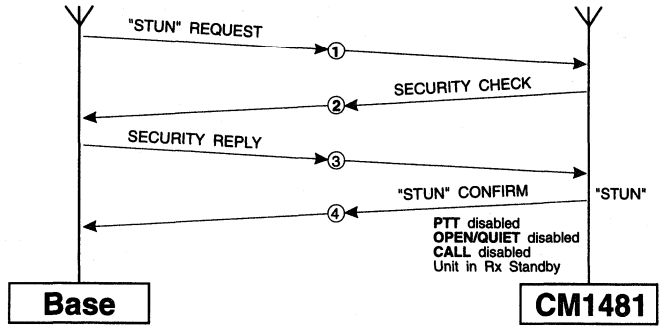


CM1481 - A Summary of Standard Functions and Features

- **Configuration by Menu-Driven Serial 'PC' Link**
- **CCIR, EEA and ZVEI Toneset/Length Capabilities**
- **HSC Signalling Control Features**
- **Over-Air "Stun" & "Release"**
- **Rapid Over-Air "Re-Configuration"**
- **Remote Reset**
- **Individual Addressing**
- **Extended Group & Data Tone Facilities**
- **Simple Radio Interface**
- **Low-Power Requirement (4.0mA typ)**
- **"Muted" Call Initiation**
- **Programmable I/O Polarities**
- **Lead/Trail Automatic Number Identification (ANI)**
- **Programmable Lead-In Tone/Delay**
- **Transponding Facility**
- **Single or Dual Button Operation**
- **Timed Mute Reset**
- **Tx (PTT) Time Out + Warning**
- **Operators Audio Alerts**
- **PTT (Busy) Lockout**
- **CMOS Compatible Logic**
- **Coded Call-Alert Capability**

CM1481 - Special Over-Air Functions

Over-Air Stun and Release - To completely disable (or enable) any unit by a simple, but secure authentication command. To prevent mistaken or accidental operations, CM1481 over-air transactions, "Stun", "Release" and "Re-Configure", are carried out using a secure authentication protocol based upon the synchronization of two pseudo-random number generators. The system is similar to that used in the over-air synchronization of rolling-code speech scramblers. The diagram below describes, basically, a "Stun" transaction sequence.



Once a unit has been "STUNned", it can only be "Released" by a base conducted Re-Configuration or by performing an over-air "Release".

Operation

1. Base initiates "STUN" Request.
2. CM1481 transmits 'SEED' for security-check pseudo-random number generation and an address check. Both units generate a 'number.'
3. Base replies with its 'number.'
4. CM1481 compares 'numbers', a valid comparison places unit into the "STUN" mode and confirms this action to base.

Over-Air Re-Configuration

An over-air function which allows the base station to remotely change the following CM1481 parameters:

Tx Address	Rx Address
Transpond Address	Transpond Mode
ANI Address	ANI Mode

Employs the same secure type authentication sequence as described above.

Remote Reset

An over-air function which allows the base station to remotely reset a CM1481 unit.

The base sends the unit's Selcall address with the Remote Reset tone 'C' or 'D' appended.

Secure authentication is not used in this transaction.

Selective Calling - Message Composition and Coding

a1	a2	a3	a4	a5	(a6)	(C/D)	(B)		
5 Tone Hexadecimal Sequential Code (HSC) Address					Optional 6th 'Address' Tone	Optional Remote Reset Tone	Optional Data Prefix (B) Tone	Additional (HSC) Function Tones	

All calls, commands and interrogations to, and calls and replies from, the CM1481 are prefixed with a 5 (or 6) tone HSC format address. Full international group-calling is possible to more than one user group via GROUP (A) and REPEAT (E) tones. Data function tones appended after the data-prefix tone (B) to the control the operation of all CM1481 transactions.

HSC Tone Signalling

'0' thro' '9'	Decimal digit value.
'A'	Address GROUP character or character 'A' in the data-field.
'B'	Data prefix character.
'C' & 'D'	Address code suffixes - to signal Remote Reset (Mute).
'E'	REPEAT character.
'F'	Available as a Lead-In Tone and used as the transpond 'BEEP' character.

CM1481 Function Tones

'0'	*Reserved for future functions.*
'1'	"STUN" Request.
'2'	"SECURITY" Check.
'3'	"SECURITY" Reply.
'4'	"CONFIGURE" Request.
'5'	"RELEASE" Request.
'6'	"STUN" Confirm.
'7'	"RELEASE" Confirm.
'8'	"CONFIGURE" Confirm.
'9'	*Reserved for future functions.*

CM1481 - Specifications

Technical Details

Temperature Range	0°C to +70°C	
Supply Voltage	6 to 26 volts d.c.	
Operating Current	4.6mA -duty cycle (no LED)	
	10% Tx, 10% Rx, 80% standby	
Standby Current	2.5mA	typ
Logic "1" In	3.5 to 26 volts d.c.	typ
Logic "0" In	0 to 1 volt d.c.	typ
PTT & Mute Out	Open Collector	50mA max
LED Drive Current	25mA	max
Tone Out Accuracy	±0.1%	max
Level	308mV rms	typ
Decode Sensitivity	31mV rms	min

Alert Signals -

Unit Muted	- short duration high-pitch beep
Unit Unmuted	- short duration low-pitch beep
Call Received	- continuous rapid mid-pitch beeps
Group Call Received	- 3 short duration mid-pitch beeps
Call Transmitted	- short duration mid-pitch beep
Tx Time-Out Warning	- short duration high-pitch beep
PTT Action Disabled	- continuous low-pitch tone
Call Action Disabled	- continuous low-pitch tone

PCB Size	45mm x 22mm x 8mm
Interface Connector	13-pin SIL male

Toneset Details - the table below details the relevant system tone frequencies available within the CM1481. All tones are available; Configuration will allocate the active set.

Tone	EEA	CCIR	ZVEI 1	PZVEI	ZVEI 2	ZVEI 3\DZVEI
0	1981 Hz	1981 Hz	2400 Hz	2400 Hz	2400 Hz	2200 Hz
1	1124	1124	1060	1060	1060	970
2	1197	1197	1160	1160	1160	1060
3	1275	1275	1270	1270	1270	1160
4	1358	1358	1400	1400	1400	1270
5	1446	1446	1530	1530	1530	1400
6	1540	1540	1670	1670	1670	1530
7	1640	1640	1830	1830	1830	1670
8	1747	1747	2000	2000	2000	1830
9	1860	1860	2200	2200	2200	2000
A	1055	2400	2800	970	885	825
B	930	930	810	810	810	740
C	2247	2247	970	2800	740	2600
D	991	991	885	885	680	885
E	2110	2110	2600	2600	970	2400
F	2400	1055	680	680	2600	680

CM1481 - Configuration Menu - the diagram shown below indicates the functions of the CM1481 and the options that may be achieved via software configuration.

Toneset	**EEA** CCIR ZVEI1 ZVEI2 ZVEI3 PZVEI		
Tone Length	**30ms** to 150ms in 10ms steps		
Lead-In Delay	**0** to 2550ms in 10ms steps		
Lead-In Tone Length	**0** to 2550ms in 10ms steps		
Lead-In Tone Digit	**0** 1 2 3 4 5 6 7 8 9 A B C D E F		
NoTone Timer	**20ms** to 300ms in 20ms steps		
PTT Time-Out	**0** to 248sec in 1sec steps		
Pseudo Iterations	**1** to 255 in steps of 1		
Timed Mute Reset	**0** to 255secs in 1sec steps		
PTT In:	Active	**LOW**	HIGH
PTT Out:	Active	**LOW**	HIGH
Busy:	Active	**LOW**	HIGH
Mute:	Active	**HIGH**	LOW
LED:	Active	**HIGH**	LOW
Quiet/Open:	Active	**LOW**	HIGH
Call:	Active	**LOW**	HIGH

Transmit Address	**5** or *6* Tones
Receive Address	**5** or *6* Tones
ANI Address	**5** or *6* Tones
Transpond Address	**5** or *6* Tones
Extended Group Tone (Tx)	**No** Yes
Number of Called Alerts	**4** to 60 in steps of 4
Extended Data Tone Tx)	**No** Yes
Call When Muted	**No** Yes
Radio "Stunned"	**No** Yes
Operation	**Single** Dual -Button
Start-Up State	**Muted** Unmuted
ANI Mode	**OFF** Lead Trail Lead & Trail
Transpond Mode	**OFF** Address Beep
Tones per Address	**5** *6*
Lead-In Gap	**No** Yes
Over-Air Functions	**No** Yes

** A comprehensive Operating and Programming Manual is supplied with the CM1481 module **

CML Semiconductor Products

PRODUCT INFORMATION

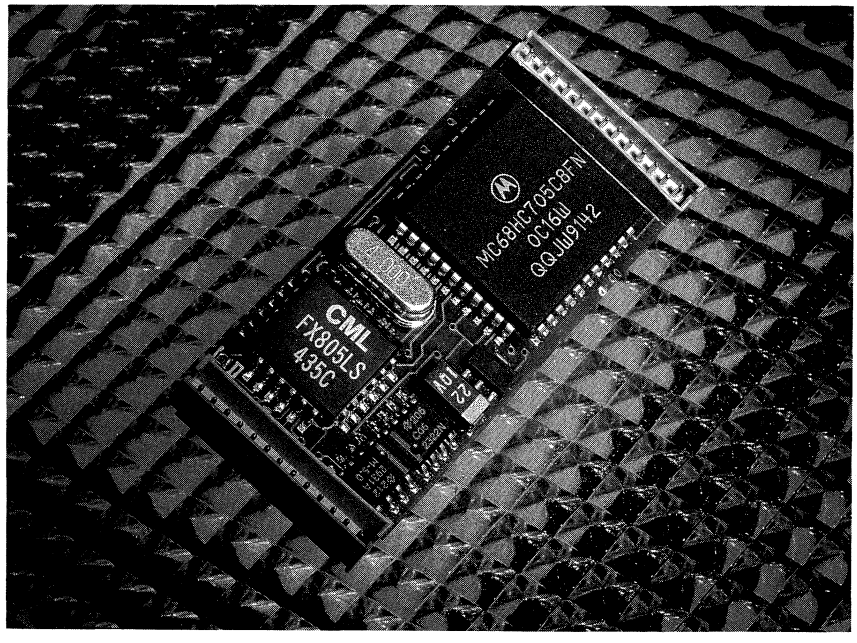
CM1482 CTCSS and DCS Sub-Audio Signalling Module

Publication D/1482/1 April 1993
Provisional Issue

Applications

- **Private Mobile Radio**
  - Mobile and Portable Field Units
  - Community (CTCSS and DCS)
  - Base-Stations
  - Trunked Radio Systems
  - Paging Systems
  - Alarm Systems

★ *THE INTELLIGENT NEXT GENERATION OF SUB-AUDIO SIGNALLING AND CONTROL* ★



CM1482

Features

- ★ **CTCSS and DCS Operation**
  (41 CTCSS Tones/104 DCS Codes)
- ★ **Duplex CTCSS Encode/Decode**
- ★ **Radio and Repeater Capabilities**
- ★ **Selective CTCSS/DCS Lockout**
- ★ **Multiple Tone/Code Rx and Tx Capabilities**
- ★ **'NEXT' Trunking Capability**
- ★ **Simple Radio Interface**
- ★ **Low-Power Requirement**
  (5.0mA @ 6v to 26v D.C. [typ])
- ★ **EMERGENCY Call Facilities**
- ★ **Simple, Serial Configuration**
- ★ **Multiple Coded Audio Alerts**
- ★ **Tx Time-Out/Penalty Timers**
- ★ **PTT Lockout**

Features

- **CTCSS and DCS**
  Coverage of 41 CTCSS tones and 104 DCS codes.
- **Duplex CTCSS Encode/Decode**
  Simultaneous encode and non-predictive decode of CTCSS tones in repeater mode.
- **DCS Encode/Decode**
  Encode or non-predictive decode of DCS signals. To encode and decode DCS simultaneously, two CM1482 modules are required.
- **Multiple Operating Modes**
  - Radio
  - Community Repeater
  - Community Trunking
- **Selective CTCSS/DCS Lockout**
  Up to 41 CTCSS frequencies and 104 DCS codes may be configured as 'friendly' lockout tones/codes.
- **'NEXT' Trunking Capability**
  Sub-audio trunking system for multi-channel, single-site community systems.
- **Simple PC Based Operating Configuration**
  Menu driven function and parameter programming.
- **Two Powersave Modes**
  Sub-audio decoder ON (Wait) or
  Sub-audio decoder OFF (Stand-by) - (lower power/ carrier dependant).
- **Compact Construction/Low Power Requirements**
  Board size - 50mm x 22mm x 8mm.
  Power requirements - 6V to 26V @ 5.0mA
  (Tx 10%/Rx 10%/Sby 80%).
- **No Programming Links or Switches**
  All CM1482 functions and parameters are set by a configuration operation from a PC type computer. Configuration may take place without removal of the module from the host equipment.

Configurable Parameters

- **Module Operating Modes**
  - Radio
  - CTCSS Community Repeater
  - DCS Community Repeater (Master + Slave)
- **CTCSS and/or DCS in System**
- **Module Identity Tone/Code**
- **Sub-Audio and/or Busy Lockout**
- **Input/Output Operating Polarities**
- **HANG, Tx Timeout, Tx Penalty and Mute Reset Timer Periods**
- **HANG Lockout Selection**
- **CTCSS Squelch-Tail Elimination**
- **DCS Rx/Tx Polarities (Normal/Inverted)**
- **Voice Audio-Enable Mode**
- **Audio Mute/Unmute Method (Push-Button/Hook)**
- **Channel Monitor Mode (Manual/Automatic)**
- **Powersave Activation**
- **Transmit Tones/Codes**
- **Receive Tones/Codes**
- **Receive PAGE/REPLY Modes**
- **CTCSS 'Selective Lockout' Frequencies**
- **DCS 'Selective Lockout' Codes**
- **EMERGENCY Tones/Codes**
- **'NEXT' Trunking Selection Tone/Code**
- **'NEXT' Marker Ident**
- **'NEXT' Free Transmit**

Features

- **Multiple Tone/C**
  For a structured c
- **Comprehensive S**
  Hang, Warning, T
  Timers.
- **Coded Audio and**
  Call Progress and
- **EMERGENCY T**
  Programmed sub-
  indication.
- **Configurable In**
  Custom inputs an
- **Manual or Auto**
  PTT operation wit
  monitoring.
- **Switched Voice-**
  On-board sub-au
  switching.
- **Signalling and/o**
  Busy and/or Carr
- **DCS Inversion F**
  Independent Rx/T
  systems.
- **Configurable U**
  Individual Rx, Tx
- **Simple Installat**
  All radio inputs ar
  accessible Radio
- **'ZETRON' Pane**
  Tones/Codes/Tim
- **Page or Reply F**
  Configuration to F

The CM1482

A non-predictive CTCSS and DCS encoder-decoder module for mobile and portable radios.

Measuring only 50mm x 22mm x 8mm with a power requirement of (typically) 5.0mA (6 to 26 volts), the CM1482 offers a range of features normally only available on advanced, expensive repeater panels.

A simple, accessible configuration system will program the module to operate, under the control of its on-board µProcessor, as either an individual radio unit, or a full-duplex 'tactical' CTCSS + Audio repeater.

Using two inter-linked modules (master and slave) will produce a full-duplex 'tactical' CTCSS + DCS + Audio repeater.

The FX805 Sub-Audio Signalling Processor IC with its non-predictive sub-audio decode capability will encode and decode ANY one of 41 sub-audio tones and 104 DCS codes (with error correction and turn-off codes), allowing the module to cover all system variations and requirements in a single installation.

In all operating modes the module will automatically determine whether the received sub-audio signal is CTCSS or DCS and decode it accordingly.

A unique Selective Lockout feature allows CBS and PMR operators to program the module to completely ignore the presence of any non-selected interfering co-channel signals from 'other' areas, and only to lockout on their own friendly, legitimate tones and codes.

The CM1482, with additional system control software, forms the heart, in both base and remote units, of the NEXT trunking scheme; a low-cost, channel efficient, sub-audio trunking system for multi-channel, single-site community systems; requiring only one CM1482 module per unit.

AND TX CAPABILITIES
ication hierarchy.

TIMERS
Out, Penalty and Audio-Mute

OPERATOR ALERTS
ıg alerts

DE FACILITIES
ɔne/code as EMERGENCY

TPUT POLARITIES
ts for various installations.

AUDIO MONITORING
ıout operator channel

PATH
ct' voice filter and audio path

Y TX LOCKOUT
ɛct lockout function.

inversion for differing radio

TITIES
ERGENCY identities.

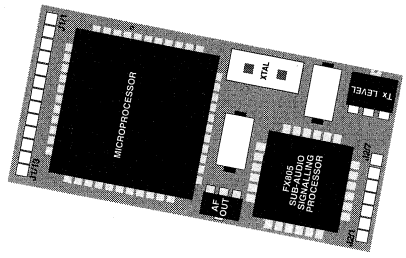
ıts connected via two
ɛe Connectors (supplied).

CODE COMPATIBLE

NS
or Rx/Tx operation.

High Intelligence

CTCSS and DCS Encoding, Decoding and Control



'NEXT' TRUNKING SYSTEM

Using a selected sub-audio signal as a NEXT FREE channel indicator in a community repeater system.

To optimize air-usage and reduce operator frustration, the 'NEXT' Trunking System will indicate to all modules when one RF channel on a community system is available (NEXT FREE) by radiating the pre-configured sub-audio tone or code on the channel.

Units operating to the 'NEXT' Trunking System will scan the allocated RF band to locate the NEXT FREE marker and then congregate on that frequency. A scan-drive output from the module is available for channel scanning.

Any unit able to transmit may operate (Tx/Rx) on the indicated (NEXT FREE) frequency using its own sub-audio tone/code. Upon detection of the commencement of traffic, the (repeater) module will move the NEXT FREE marker to another (if) available RF channel; units not involved in that call, when losing the NEXT FREE marker, will scan-on to locate the new FREE channel.

SIMPLE MODULE PROGRAMMING

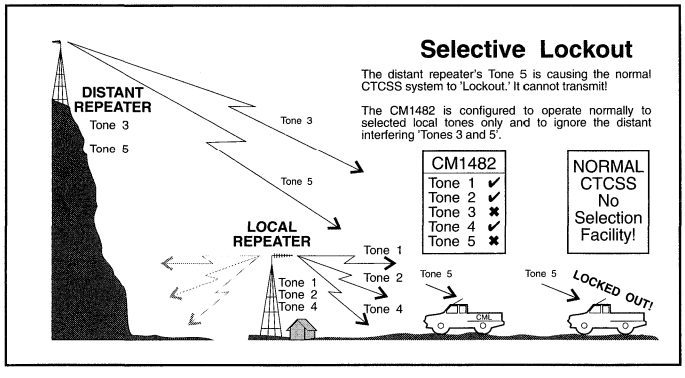
The CM1482 requires no awkward on-board links, solder-bridges or DIP switches for programming and there is no requirement for removal of the module from its host equipment for configuration.

All mode, function and parameter information can be speedily transferred to and from the module using any DOS-based computer running the CM1482 Configuration Software.

Configuration and re-configuration operations may be carried out at any location, i.e. Workshop, Office, Remote Site or at the roadside. Operating software for use with the on-board µProcessor is embedded in the module's EEPROM with configuration software available on floppy-disk; a library of module set-ups can be generated and carried in the same directory making the whole configuration operation self-contained.

Configuration of the CM1482 is achieved via a simple serial interface lead which replaces the normal operating Radio Interface Connector to the module, automatically placing the CM1482 in the Configuration mode.

SELECTIVE CTCSS/DCS LOCKOUT



One of the main inconveniences encountered in a signalling and communications control system is that any received co-channel information will prevent radio transmission by initiating Tx Lockout.

The CM1481 overcomes this by careful configuration. Any number (up to the maximum tones and codes available) of friendly tones or codes can be programmed to provide selective-lockout for a community's legitimate sub-audio signals.

Any other 'nuisance' sub-audio signals encountered by the module will be ignored. Interfering co-channel signals that are NOT configured into the CM1481 lockout list will NOT prevent module transmission.

MULTIPLE USER GROUPS

The CM1482 is capable of decoding more than one sub-audio tone or code; a feature that will allow supervisors/managers/controllers to communicate with up to four user groups simultaneously.

Specification

Module Dimensions	50mm x 22mm x 8mm
Operating Temperature Range	0°C to 70°C
Supply Voltage Range	6V to 26V d.c.
Operating Current	
Typical Operating Cycle	5.0mA (Tx 10%/Rx 10%/Sby 80%).
Encode Output Level	variable up to 308mVrms
Selective Lockout Range	- up to 41 CTCSS Tones
	- up to 104 DCS Cod
CTCSS	
Encode	41 Sub-Audio Tones
Distortion	5.0%$_{(typ)}$
Tone Accuracy	0.2%$_{(typ)}$
Non-Predictive Decode	41 Sub-Audio Tones
Sensitivity	30mVrms to 100mVrms
SINAD Performance	better than 10.0dB
Response/De-Response Time	250ms
DCS	
Encode	104 Codes + Tx Inversion
Non-Predictive Decode	104 Codes + Rx Inversion
Sensitivity	30mVrms to 100mVrms
SINAD Performance	better than 10.0dB
Response Time	350ms
De-Response Time	250ms
Turn-Off Detection Time	30ms to 70ms

Continuous Tone Controlled Squelch System (CTCSS) Frequencies (Hz) Available

62.5	64.7	67.0	69.3	71.9	74.4	77.0	79.7
82.5	85.4	88.5	91.5	94.8	97.4	100.0	103.5
107.2	110.9	114.8	118.8	123.0	127.3	131.8	136.5
141.3	146.2	151.4	156.7	162.2	167.9	173.8	179.9
186.2	192.8	203.5	210.7	218.1	225.7	233.6	241.8
250.3							

Digitally Coded Squelch Codes Available

023	025	026	031	032	036	043	047
051	053	054	065	071	072	073	074
115	116	114	122	125	131	132	134
143	145	152	155	156	162	165	172
174	205	212	223	225	226	243	244
245	246	251	252	255	261	263	265
266	271	274	306	311	315	325	331
332	343	346	351	356	364	365	371
411	412	413	423	431	432	445	446
452	454	455	462	464	465	466	503
506	516	523	526	532	546	565	606
612	624	627	631	632	654	662	664
703	712	723	731	732	734	743	754

Operator Audio ALERTS Available

Normal Call Received	*PAGE Call Received*
EMERGENCY Call Received/Progress	*Illegal PTT Attempt*
Tx Time-Out Warning	*Call Ended*
QUIET State	*OPEN State*

Operator Visual ALERTS Available (LED)

Module Active in Call

Powerup Failure

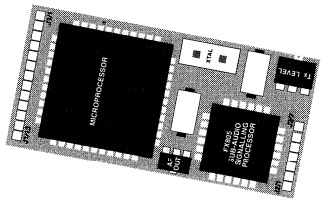
'NEXT' Signal Out-Of-Range

The CM1482 and Configuration Kit Ordering Information

CM1482 **CTCSS and DCS Module**
(Module + Radio Interface Connectors)

CK1482 **Configuration Kit**
(Configuration Interface Connector + Software {5¼ & 3½" disks})

CM1482 Module Actual Size



For Further Information Please Contact CML or Your Local Distributor

Integrated Circuits Data Book

Section 3

Cellular Radio

CML Semiconductor Products

PRODUCT INFORMATION

FX306 Audio Filter Array

Publication D/306/6 July 1994

Features/Applications

- Cellular Radio Audio Processing to NMT TACS AMPS Specification
- Low Group Delay Distortion
- Switched Capacitor Filters
- On-Chip Uncommitted Amplifier
- Xtal Controlled
- Chip Enable Powersave Feature
- Low-Power CMOS Process
- Choice of Package Styles
- Few External Components
- Single 5-Volt Supply

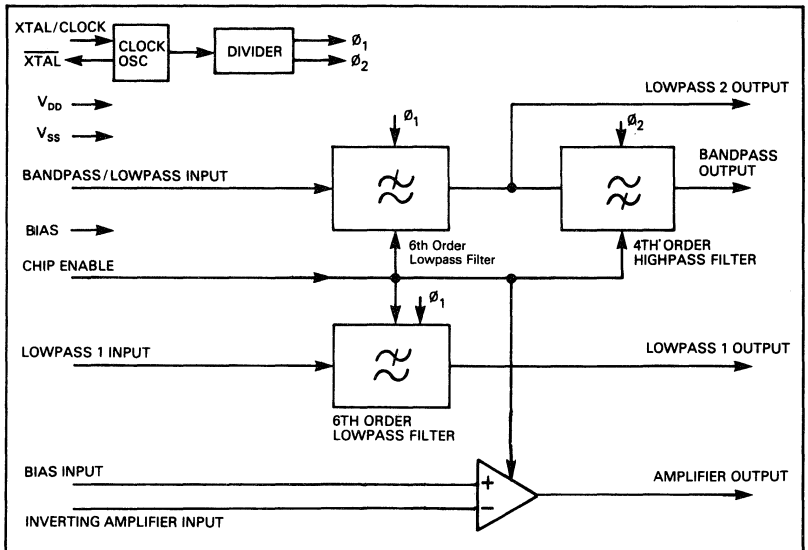


Fig. 1 Internal Block Diagram

FX306

Brief Description

The FX306 is a low-power CMOS switched capacitor filter array designed to meet the NMT TACS and AMPS audio processing specifications. The device consists of:

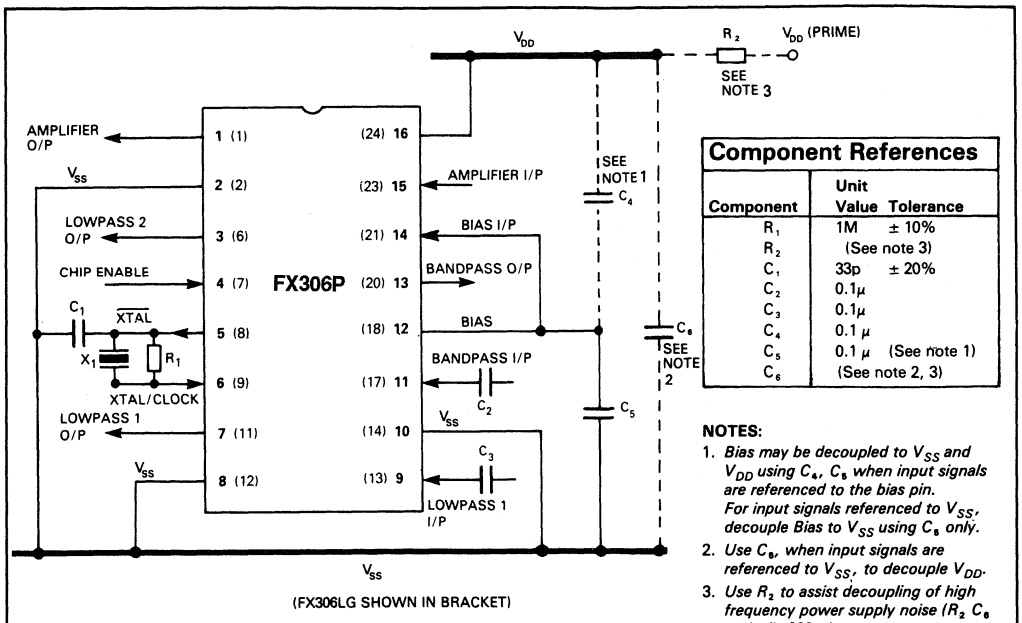
(1) a 3.4 kHz lowpass filter.
(2) a 300 Hz—3.4 kHz bandpass filter (lowpass filter identical to that of (1) in series with a highpass filter).
(3) an uncommitted amplifier.

The two 6th order lowpass filters provide a low group delay distortion path. The amplifier may be used for any specific applications such as, pre-emphasis, de-emphasis, buffering etc. An on-chip oscillator uses a 1 MHz Xtal and provides all reference clocks for the switched capacitor filters via a divider chain. Alternatively an external clock maybe used.

The chip enable feature is used to disable the filter sections and the amplifier, thus reducing current consumption.

Pin Number		Function
FX306P	FX306LG	
1	1	**Amp O/P:** Uncommitted amplifier output.
2	2	**V_{SS}:** Negative Supply.
3	6	**LP (2) O/P:** Buffered output from the intermediate lowpass filter (Bandpass arrangement).
4	7	**Chip Enable:** Internally pulled to V_{DD}. A logic '0' applied to this input will disable all filters (powersave mode).
5	8	**$\overline{\text{Xtal}}$:** 1 MHz Xtal O/P. Inverting output of on-chip oscillator.
6	9	**Xtal/Clock:** 1 MHz Xtal I/P or externally derived clock can be injected into this I/P. Input to on-chip inverting oscillator.
7	11	**LP (1) O/P:** Output of separate lowpass filter.
8	12	**V_{SS}:** Negative Supply.
9	13	**LP (1) I/P:** Input of separate lowpass filter.
10	14	**V_{SS}:** Negative Supply.
11	17	**BP I/P / LP (2) I/P:** Bandpass/lowpass filter (2) input.
12	18	**Bias:** $V_{SS}/2$ Bias Pin. Externally decoupled by C_4 and C_5. (See Fig 2, Note 1.)
13	20	**BP O/P:** Bandpass filter output.
14	21	**Bias: I/P:** Connect externally to 'Bias' pin.
15	23	**Amp I/P:** Uncommitted inverting amplifier input.
16	24	**V_{DD}:** Positive Supply.

FX306LG Pin numbers 3, 4, 5, 10, 15, 16, 19, 22 are not connected.



Component References

Component	Unit Value	Tolerance
R_1	1M	± 10%
R_2	(See note 3)	
C_1	33p	± 20%
C_2	0.1μ	
C_3	0.1μ	
C_4	0.1 μ	
C_5	0.1 μ	(See note 1)
C_6	(See note 2, 3)	

NOTES:

1. *Bias may be decoupled to V_{SS} and V_{DD} using C_4, C_5 when input signals are referenced to the bias pin. For input signals referenced to V_{SS}, decouple Bias to V_{SS} using C_5 only.*
2. *Use C_6, when input signals are referenced to V_{SS}, to decouple V_{DD}.*
3. *Use R_2 to assist decoupling of high frequency power supply noise (R_2 C_6 typically 300μs)*

Fig.2 External Component Connections

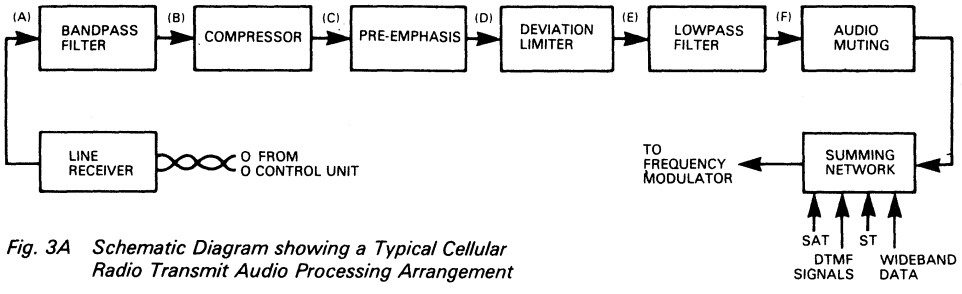


Fig. 3A Schematic Diagram showing a Typical Cellular Radio Transmit Audio Processing Arrangement

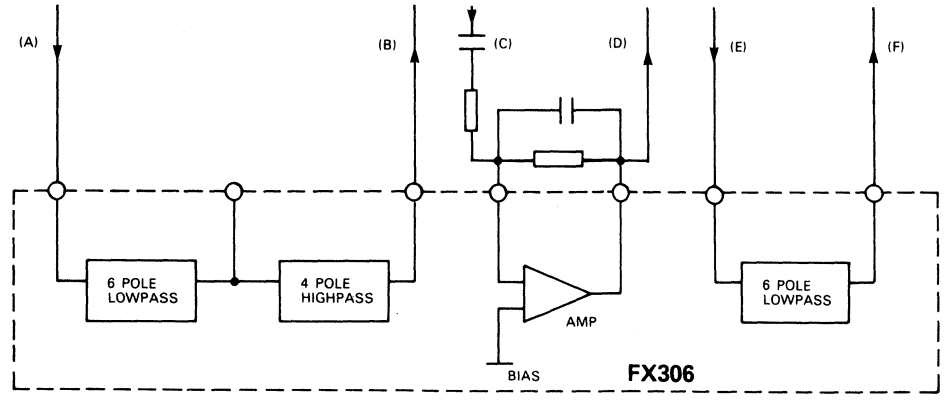


Fig. 3B The FX306 used in the above application

Specification

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating Temperature:	**FX306LG/P**	-30°C to +70°C
Storage Temperature:	**FX306LG/P**	-40°C to +85°C
Maximum device dissipation:	all versions	100mW

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5V, T_{amb} = 25°C, Ø = 1MHz, $\Delta f \phi$ = 0, f_{in} = 1kHz.

Characteristics	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply voltage		4.5	5	5.5	V
Supply current (Enabled)		—	3.5		mA
Supply current (Disabled)		—	500		µA
Input impedance (Filters & Amplifier)		100		—	kΩ
Output impedance (Filters)		—	3		kΩ
Output impedance (Amplifier open loop)		—	800		Ω
Output impedance (Amplifier closed loop)		—	6		Ω
Input logic '1'		3.5	—	—	V
Input logic '0'		—	—	1.5	V
Dynamic Characteristics					
Signal input dynamic range LP	1		40		dB
BP	1		40		dB
Cut off frequency (−3dB) LP			3400		Hz
HP			260		Hz
Group Delay (900—2100Hz) LP			30	60	µs
BP			60		µs
Noise and Distortion LP	2		45		dB sinad
BP	2		35		dB sinad
Passband ripple (400—3000Hz)				2	dB absolute
Lowpass attenuation f> 4kHz	3		10		dB
f> 6kHz	3		35		dB
Highpass attenuation f< 200Hz	3		15		dB
Insertion loss f = 1kHz			0		dB
Inverting Amplifier					
Open loop gain	3		30		dB
Gain bandwidth product			1		MHz

Note: *1. For 20dB sinad (psophometrically weighted)*
2. −6dBm input (psophometrically weighted)
3. Relative to 1kHz 100mV rms input level

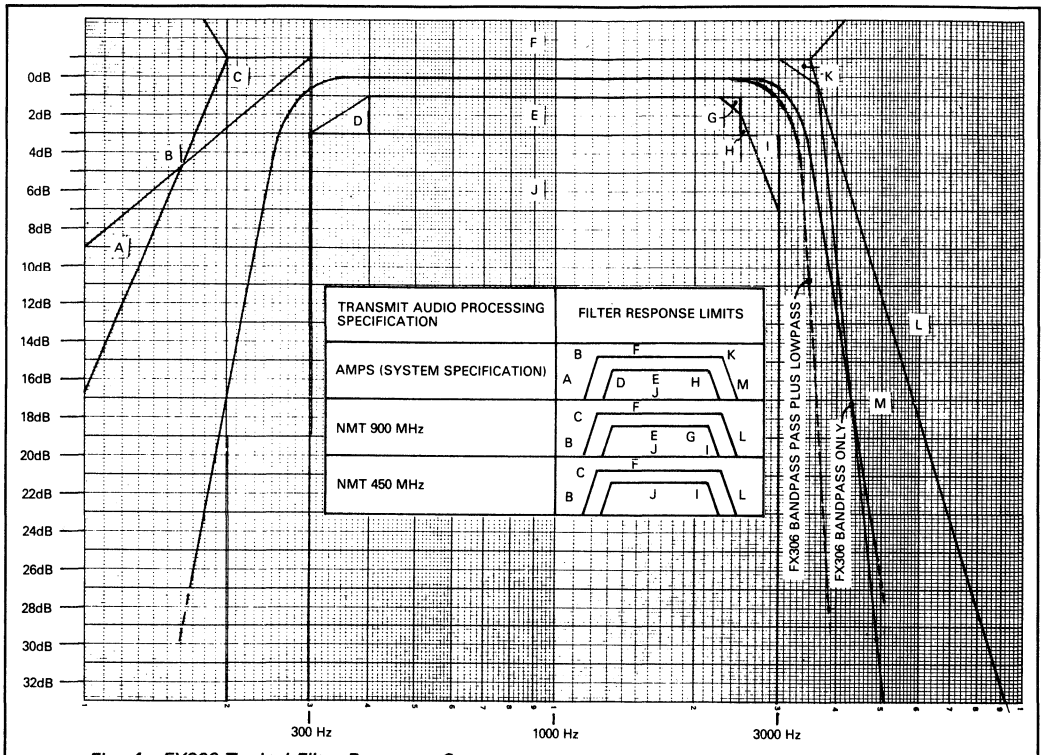


Fig. 4 FX306 Typical Filter Response Curves

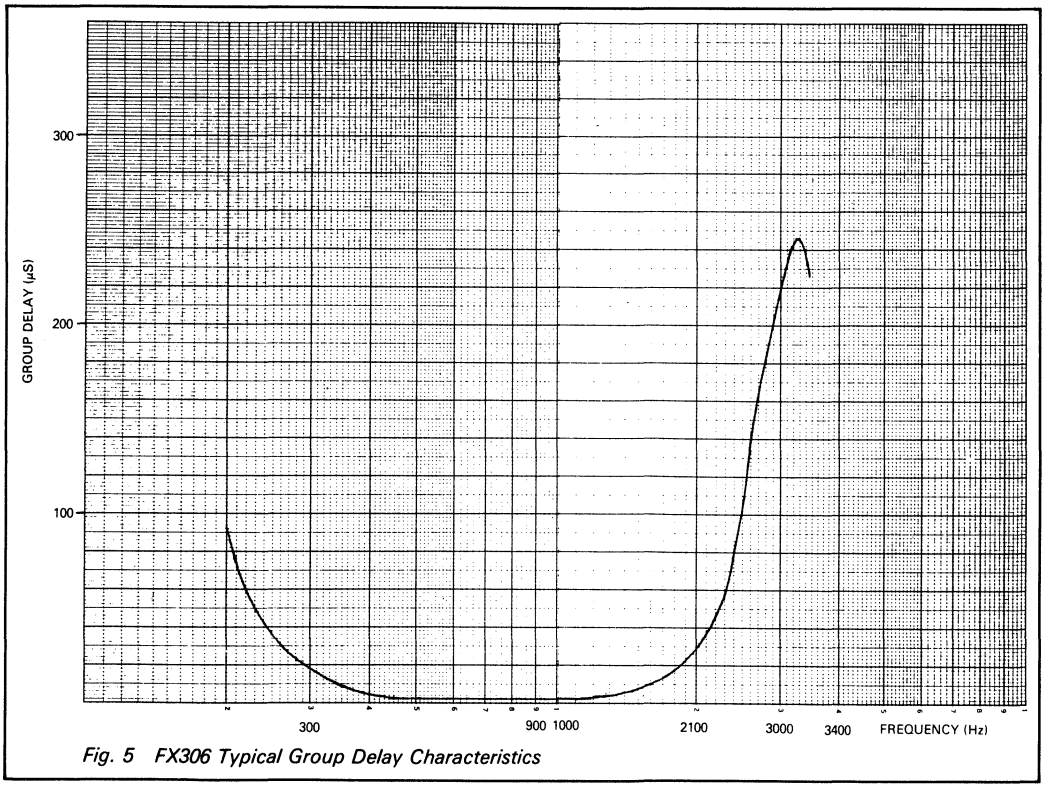


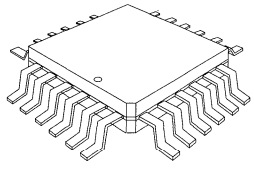
Fig. 5 FX306 Typical Group Delay Characteristics

Package Outlines

The FX306 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX306LG 24-pin quad plastic encapsulated bent and cropped (L1)

NOT TO SCALE



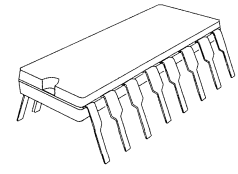
Max. Body Length 10.25mm
Max. Body Width 10.25mm

Handling Precautions

The FX306 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX306P 16-pin plastic DIL (P3)

NOT TO SCALE



Max. Body Length 19.24mm
Max. Body Width 6.41mm

Ordering Information

FX306LG 24-pin encapsulated bent and cropped (L1)

FX306P 16-pin plastic DIL (P3)

CML Semiconductor Products

PRODUCT INFORMATION

FX316 NMT Audio Filter Array

Publication D/316/5 July 1994

Features/Applications

- Cellular Radio Audio Processing
- NMT 450 & 900MHz Base Station and Mobile Specifications
- High Order Lowpass Filter including SAT Rejection
- Low Group Delay Distortion
- 4kHz SAT Recovery Bandpass Filter
- Uncommitted Amplifier
- Switched Capacitor Filters
- Xtal Controlled
- Single 5 Volt CMOS Process
- Chip Enable Powersave Feature
- Few External components
- Surface Mount or DIL Package Style

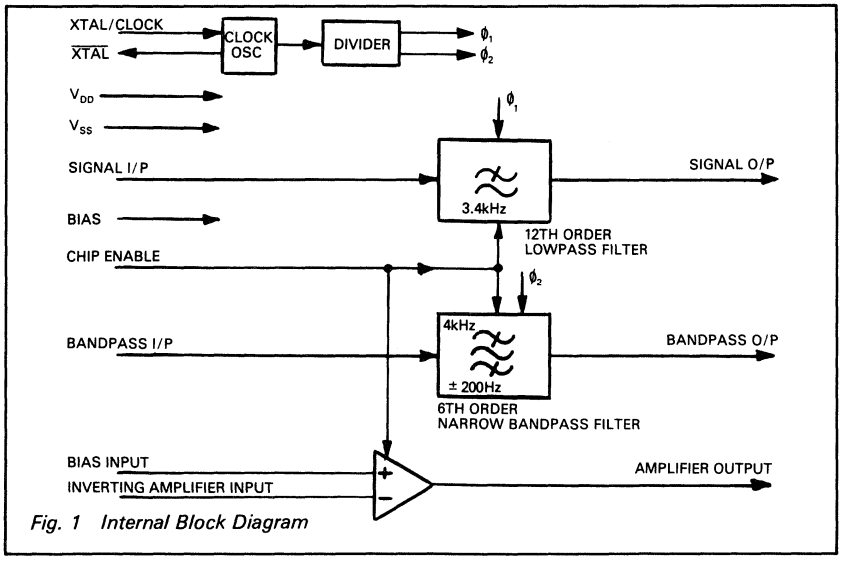


Fig. 1 Internal Block Diagram

FX316

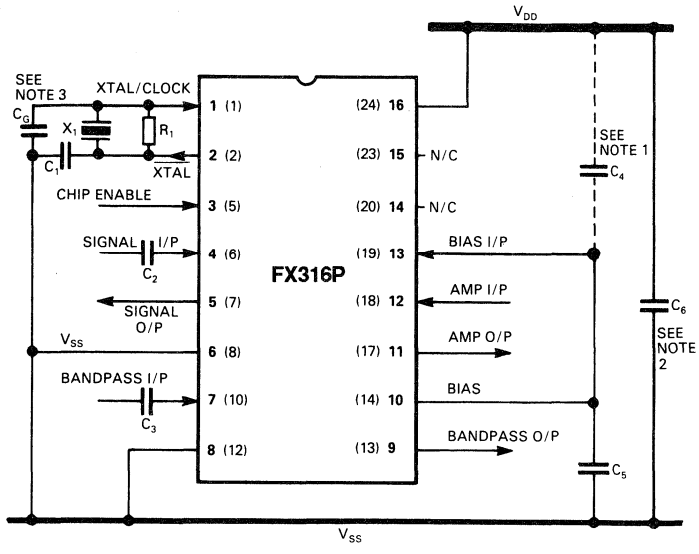
Brief Description

The FX316 is a low-power CMOS Switched Capacitor filter array designed to meet NMT Base and Mobile specifications.

The device in detail consists of:
(1) a 12th order 3.4kHz lowpass filter with sufficient rejection of 4kHz signals to meet NMT 450 and 900 filter response specifications for both base and mobile equipments. The lowpass filter also provides a low group delay distortion path.
(2) a 6th order 4kHz narrow bandpass filter which meets the NMT 450 and 900 mobile specifications for SAT recovery.
(3) an uncommitted amplifier which may be used for any specific applications such as pre-emphasis, de-emphasis, buffering etc. An on chip oscillator uses a 1MHz Xtal and provides all reference clocks for the switched capacitor filters via a divider chain. Alternatively, an external clock may be used. The chip enable feature is used to disable the three circuit elements thus reducing current consumption.

Pin Functions

FX316 LG/LS	FX316 P	
1	1	**Xtal/Clock:** 1 MHz Xtal I/P or externally derived clock can be injected into this input. Input to on-chip inverting oscillator.
2	2	**$\overline{\text{Xtal}}$:** 1 MHz Xtal O/P. Inverting output of on-chip oscillator.
5	3	**Chip Enable:** Internally pulled to V_{DD}. A logic '0' applied to this input will disable all filters and the uncommitted amplifier (powersave mode).
6	4	**Signal I/P:** Input to lowpass filter. This input is internally biased and externally ac coupled by C_2.
7	5	**Signal O/P:** Lowpass filter output internally biased to $V_{DD}/2$.
8	6	**V_{SS}:** Negative supply.
10	7	**Bandpass I/P:** Input to the bandpass filter. This input is iunternally biased and externally ac coupled by C_3.
12	8	**V_{SS}:** Negative supply.
13	9	**Bandpass O/P:** Bandpass filter output internally biased to$V_{DD}/2$.
14	10	**Bias:** $V_{DD}/2$ Bias Pin. Externally decoupled by C_5 (see Figure 2, Note 1).
17	11	**Amp O/P:** Uncommitted amplifier output.
18	12	**Amp I/P:** Uncommitted amplifier inverting input.
19	13	**Bias I/P:** Connect externally to 'Bias' pin.
20	14	No Connection: Internally connected leave open circuit.
23	15	No Connection: Internally connected leave open circuit.
24	16	**V_{DD}:** Positive supply.
		FX316LG/LS: Pin numbers 3, 4, 9, 11, 15, 16, 21 and 22 are not connected.
		Note: Output Loading Large capacitive loads could cause the output pins of this device to oscillate. If capacitive loads in excess of 200 pF are unavoidable, a resistor of typically <100Ω put in series with the load should minimise this effect.



(FX316LG SHOWN IN BRACKETS. N/C = NO CONNECTIONS)

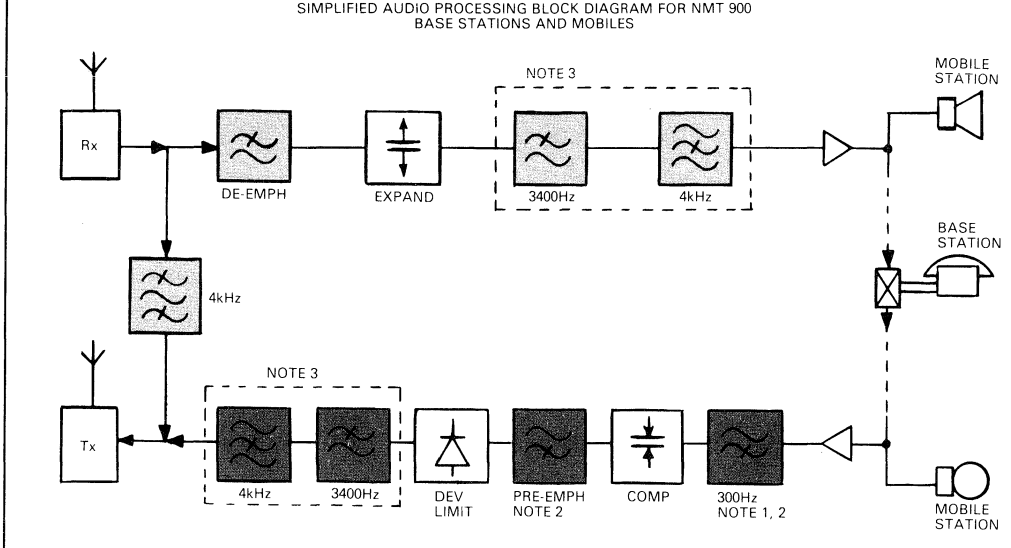
Component References

Component	Typical Unit Value	
R_1	1M	10%*
C_1	33p	20%*
C_2	0.1µ	20%
C_3	0.1µ	20%
C_4	0.1µ	20%
C_5	0.1µ Min.	20%
C_6	0.1µ	20%
C_G	68p	20%*
X_1	1MHz*	
*	See Note 3	

NOTES:

1. *Bias may be decoupled to V_{SS} and V_{DD} using C_4, C_5 when input signals are referenced to the bias pin. For input signals referenced to V_{SS}, decouple Bias to V_{SS} using C_5 only.*
2. *Use C_6, when input signals are referenced to V_{SS}, to decouple V_{DD}.*
3. *Xtal circuitry shown is in accordance with CML application note D/XT/I April 1986.*

Fig. 2 External Component Connections



NOTES:

1). Not required in base station.
2). Pre-emph and highpass filter may be constructed using on-chip amplifier.
3). FX316 Lowpass Filter achieves both these functions.

FX316 (DEVICE A) FX316 (DEVICE B) BASE STATION ONLY

Fig. 3 FX316 Typical Application

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating Temperature:	**FX316LG/LS/P**	-30°C to +70°C
Storage Temperature:	**FX316LG/LS/P**	-40°C to +85°C
Maximum device dissipation:	all versions	100mW

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5V, T_{amb} = 25°C, Ø = 1MHz, $\Delta f_{\emptyset}$ = 0, f_{in} = 1kHz.

Characteristics		See Note	Min	Typ	Max	Unit
Static Characteristics						
Supply voltage			4.5	5	5.5	V
Supply current (Enabled)			—	6.0	—	mA
Supply current (Disabled)			—	700	—	μA
Input impedance (Filters & Amplifier)			100	1000	—	kΩ
Output impedance (Filters)			—	3	—	kΩ
Output impedance (Amplifier open loop)			—	800	—	Ω
Output impedance (Amplifier closed loop)			—	6	—	Ω
Input logic '1'			3.5	—	—	V
Input logic '0'			—	—	1.5	V
Dynamic Characteristics						
Passband Ripple	(300-3000Hz) LP	5	—	—	2	dB
	(4kHz±55Hz) BP	5	—	—	2	dB
Cut-off Frequency	(−3dB) LP	4, 5	3000	3450	3800	Hz
	(−6dB) BP	4, 5	4200	—	3800	Hz
Attenuation	(3800−4200Hz) LP	4, 5	36	46	—	dB
	(<2000Hz,>6000Hz) BP	4, 5	35	37	—	dB
Group Delay Distortion	(900-2100Hz) LP		—	80	—	μs
	(600-3000Hz) LP		—	450	—	μs
Output Noise (rms)	LP	1	—	1.6	—	mV
	BP	1	—	1	—	mV
Signal Input (rms)	LP	2	—	0.4	1.0	V
	BP	2	—	0.4	1.0	V
Insertion loss (1kHz)	LP		—	0	—	dB
(4kHz)	BP		—	0	—	dB
Aliasing Frequency			50	—	—	kHz
Inverting Amplifier						
Open loop gain		3	—	30	—	dB
Gain bandwidth product			—	1	—	MHz

Notes: *1. Measured with input a.c. s/c.*
2. 'MAX' figure specified for nominal 3% distortion (30dB SINAD).
'TYP' figure specified for minimum distortion (MAX SINAD).
3. Relative to 1kHz 100mV rms input level.
4. Refer to Figs. 4 and 5.
5. Specified over the full operating voltage and temperature range.

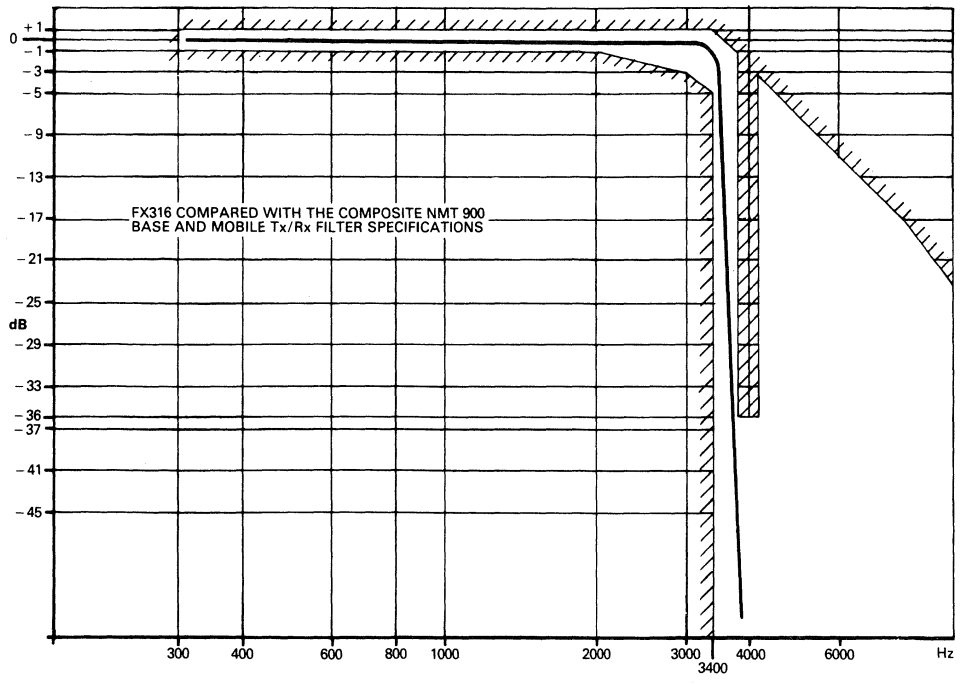


Fig. 4 Typical FX316 Lowpass Filter Response

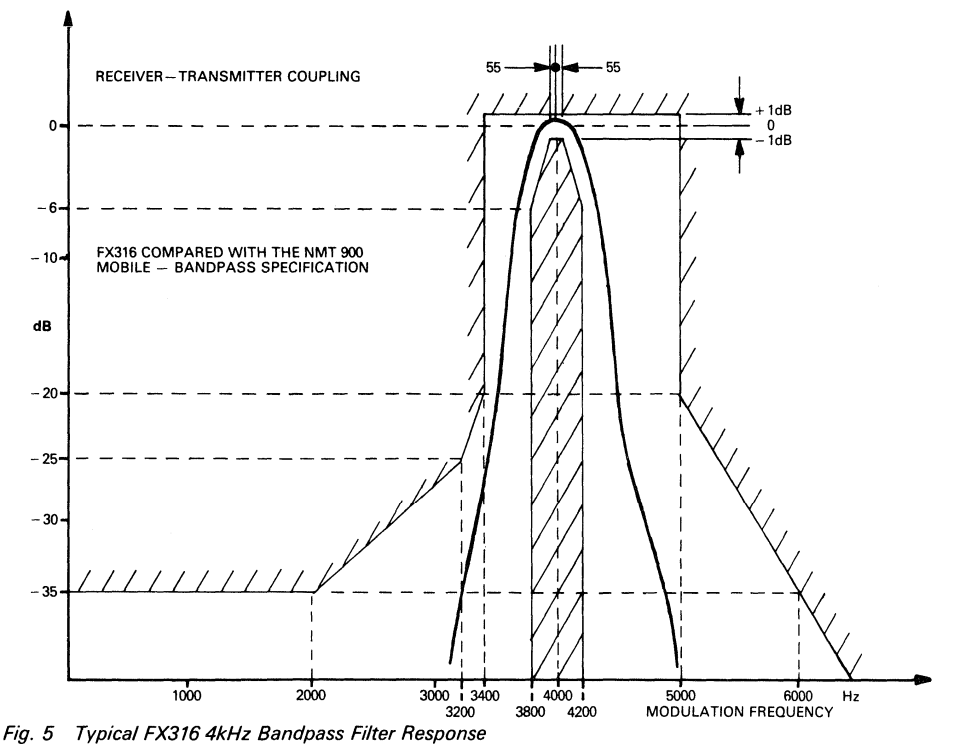


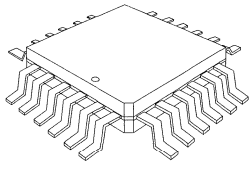
Fig. 5 Typical FX316 4kHz Bandpass Filter Response

Package Outlines

The FX316 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX316LG 24-pin quad plastic encapsulated bent and cropped (L1)

NOT TO SCALE



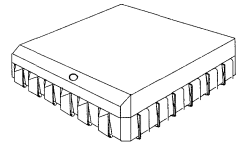
Max. Body Length 10.25mm
Max. Body Width 10.25mm

Handling Precautions

The FX316 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX316LS 24-lead plastic leaded chip carrier (L2)

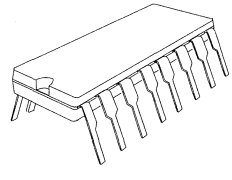
NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

FX316P 16-pin plastic DIL (P3)

NOT TO SCALE



Max. Body Length 19.24mm
Max. Body Width 6.41mm

Ordering Information

FX316LG	24-pin encapsulated bent and cropped	(L1)
FX316LS	24-lead plastic leaded chip carrier	(L2)
FX316P	16-pin plastic DIL	(P3)

CML Semiconductor Products

PRODUCT INFORMATION

FX336 R2000 Filter Array

Publication D/336/3 July 1994

Features/Applications

- R2000 Trunked Radio Audio Processing
- High Order 300Hz Highpass Filter
- Low Group Delay 2550Hz Lowpass Filter
- On-Chip 120–175Hz Bandpass
- Uncommitted Amplifier and Analogue Switch
- Typical 43dB Rejection Below 170 Hz
- Switched Capacitor Filters
- Xtal Controlled
- Single 5 Volt CMOS Process
- Chip Enable Powersave Feature
- Surface Mount or DIL Package Styles

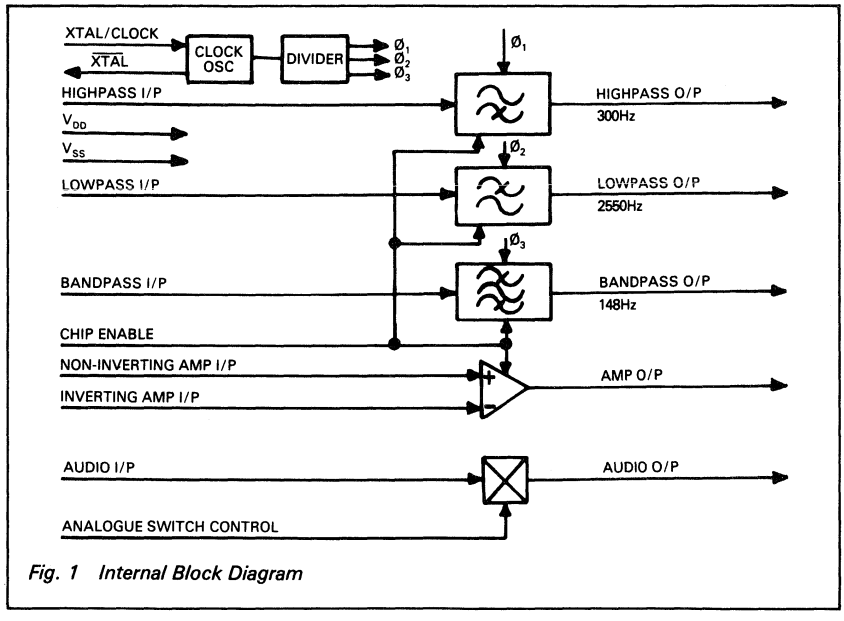


Fig. 1 Internal Block Diagram

FX336

Brief Description

The device is a single chip CMOS filter array used to process speech and 50 baud FSK signals as specified in the Radiocom 2000 system specification. The device consists of:

(a) Highpass audio filter with typically 43dB attenuation of signals below 170 Hz.

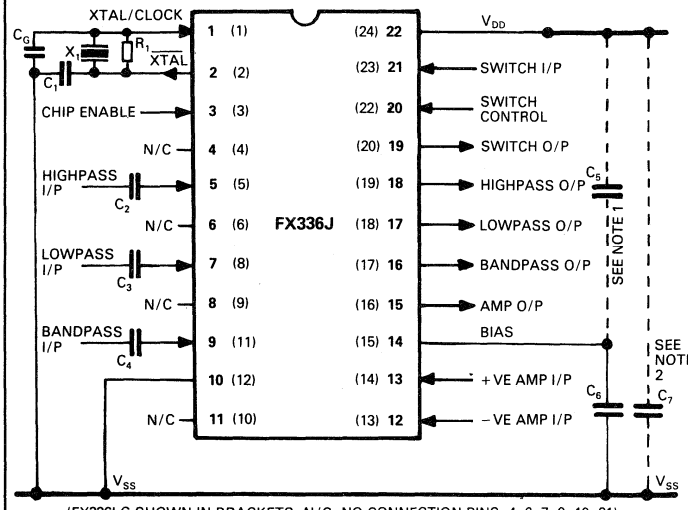
(b) Lowpass audio filter for band-limiting speech in 12.5 kHz channel spacing radios. The group delay of this lowpass filter is controlled over the range 900–2100Hz, hence allowing the filter to pass 1200 Baud FFSK data.

(c) Narrow bandpass filter for processing 50 baud FSK data.

(d) Uncommitted audio amplifier.

(e) Mute switch with external control.

Pin Number			Function
FX336J	FX336LG	FX336LS	
1	1	1	**Xtal/Clock:** This is the input to the clock oscillator inverter. 1MHz xtal input or externally derived clock can be injected into this input.
2	2	2	**$\overline{\text{Xtal}}$:** Output of clock oscillator inverter.
3	3	3	**Chip Enable:** This input has an internal 1MΩ pull up resistor to V_{DD}. When pulled to V_{SS} (logic '0') all internal amplifiers are disabled and current consumption is reduced.
4	4	4, 5	**No Connection.**
5	5	6	**Highpass I/P:** Input to highpass filter.
6	6, 7	7, 8	**No Connection.**
7	8	9	**Lowpass I/P:** Input to lowpass filter.
8	9, 10	10, 11, 12	**No Connection.**
9	11	13	**Bandpass I/P:** Input to narrow bandpass filter.
10	12	14	V_{SS}: Negative supply.
11	—	15	**No Connection.**
12	13	16	**Amp Negative:** Inverting input of uncommitted amplifier.
13	14	17	**Amp Positive:** Non-inverting input of uncommitted amplifier.
14	15	18	**Bias:** This is the bias or analogue ground pin and is set internally at $V_{DD}/2$. It should be decoupled to V_{SS} by an externally connected 1.0μF (min).
—	—	19	**No Connection.**
15	16	20	**Amp O/P:** Output of uncommitted amplifier.
16	17	21	**Bandpass O/P:** Output of narrow bandpass filter.
17	18	22	**Lowpass O/P:** Output of lowpass filter.
18	19	23	**Highpass O/P:** Output of highpass filter.
19	20	24	**Switch O/P:** Output of analogue switch. This output is internally biased to approximately $V_{DD}/2$.
—	21	25	**No connection.**
20	22	26	**Switch Control:** Control input of analogue switch, internally pulled to V_{DD} by 1MΩ resistor with switch in 'closed' position. When this input is pulled to V_{SS} the switch is in 'open' position.
21	23	27	**Switch I/P:** Input of analogue switch.
22	24	28	V_{DD}: Positive supply.
			Note: Output Loading. Large capacitive loads could cause the output pins of this device to oscillate. If capacitive loads in excess of 200pF are unavoidable, a resistor of typically <100Ω put in series with the load should minimise this effect.



(FX336LG SHOWN IN BRACKETS. N/C: NO CONNECTION PINS: 4, 6, 7, 9, 10, 21)

Component References

Component	Typical Unit Value	
R_1	1MΩ	Note 3
C_1	33p	
C_2	0.1μ	
C_3	0.1μ	
C_4	0.1μ	
C_5	0.1μ	Note 1
C_6	1.0μ Min.	Note 1
C_7	0.1μ Min.	Note 3
C_G	47p	Note 3
X_1	1MHz	Note 3
R = ±10%	C = ±20%	

NOTES:

1. *Bias may be decoupled to V_{SS} and V_{DD} using C_5, C_6 when input signals are referenced to the bias pin. For input signals referenced to V_{SS}, decouple Bias to V_{SS} using C_6 only.*
2. *Use C_7, when input signals are referenced to V_{SS}, to decouple V_{DD}.*
3. *Xtal circuitry shown is in accordance with CML application note D/XT/I April 1986.*

Fig. 2 External Component Connections

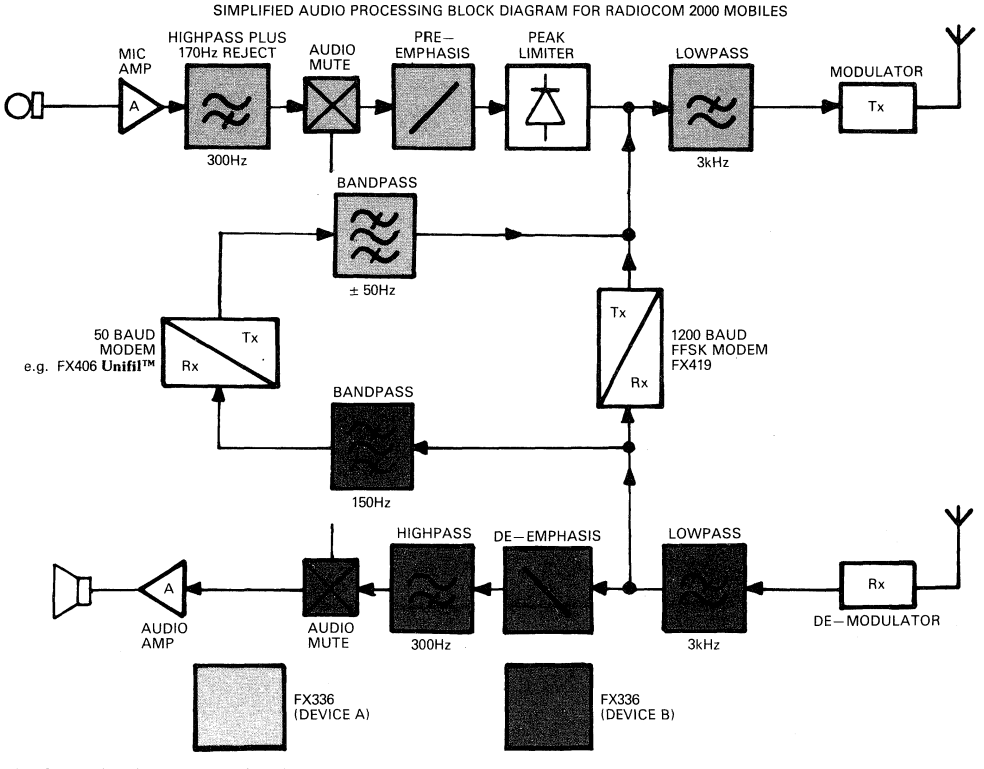


Fig. 3 FX336 Typical Application

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating Temperature:	FX336J	-30°C to +85°C
	FX336LG/LS	-30°C to +70°C
Storage Temperature:	FX336J	-55°C to +125°C
	FX336LG/LS	-40°C to +85°C

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5V, T_{amb} = 25°C, Ø = 1MHz, Δf_O = 0, f_{in} = 1kHz, V_{in} = 1.0 V(rms)

Characteristics		See	Note	Min	Typ	Max	Unit
Static Characteristics							
Supply voltage				4.5	5	5.5	V
Supply current (Enabled)				—	6.8	—	mA
Supply current (Disabled)				—	600	—	µA
Input impedance (Filters & Amplifier)				100	800	—	kΩ
Output impedance (Filters & Amplifier)				—	1.0	—	kΩ
Input logic '1'				70%V_{DD}	—	—	V
Input logic '0'				—	—	30%V_{DD}	V
Dynamic Characteristics							
Passband Ripple	(300-2550Hz)	HP+LP	1	—	—	2	dB
	(280-300Hz)	HP+LP	2	+1	0	−2	dB
	(120−175Hz)	BP	2	—	—	3	dB
Cut-off Frequency	(−3dB)	HP		—	265	—	Hz
	(−3dB)	LP		—	3800	—	Hz
	(−6dB)>150Hz	BP		—	190	—	Hz
	(−6dB)<150Hz	BP		—	115	—	Hz
Stopband Attenuation	<170Hz	HP		40	43	—	dB
	>9000Hz	LP		40	47	—	dB
	<65Hz>290Hz	BP		30	40	—	dB
Group Delay Distortion	(900-2100Hz)	LP		—	30	60	µs
	(900-2100Hz)	HP+LP		—	300	—	µs
	(136-164Hz)	BP	3	—	1.7	—	ms
Output Noise		LP	4	—	2.0	—	mV(rms)
		HP	4	—	2.0	—	mV(rms)
		BP	4	—	2.0	—	mV(rms)
Signal Input		LP	5	—	0.5	1.0	V(rms)
		HP	5	—	0.5	1.0	V(rms)
		BP	5	—	0.5	1.0	V(rms)
Passband Gain	(1kHz)	HP+LP		−0.5	+0.5	+1.5	dB
	(150Hz)	BP		−1	0	+1	dB
Aliasing Frequency				50	—	—	kHz
Audio Switch							
Output Noise	(rms)		4	—	—	1	mV
Channel Resistance	(on)			—	500	—	kΩ
Channel Resistance	(off)			10	—	—	MΩ
Uncommitted Amplifier							
Open loop gain				35	50	—	dB
Bandwidth				—	200	—	kHz

Notes: *1. Absolute ripple—see Fig. 4.*
2. Absolute ripple—see Fig. 5.
3. Relative delay between 136 and 164Hz.
4. Measured with input a.c. s/c; at 30kHz Bw.
5. 'MAX' figure specified for nominal 3% distortion (30dB).
'TYP' figure specified for minimum distortion (MAX SINAD).

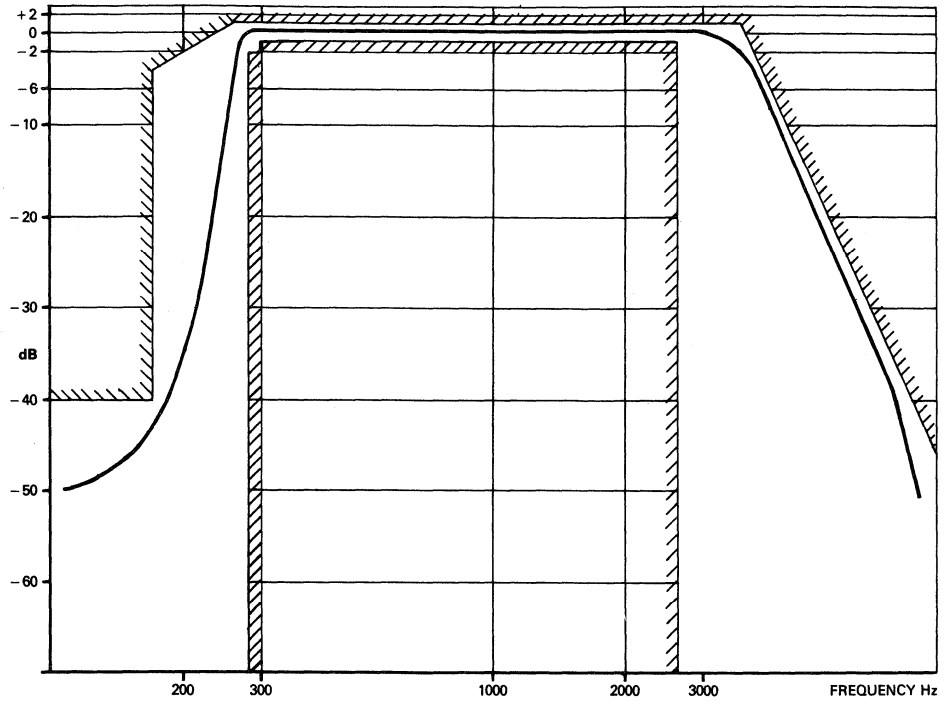


Fig. 4 Typical audio bandpass filter frequency response versus R2000 filter specification.

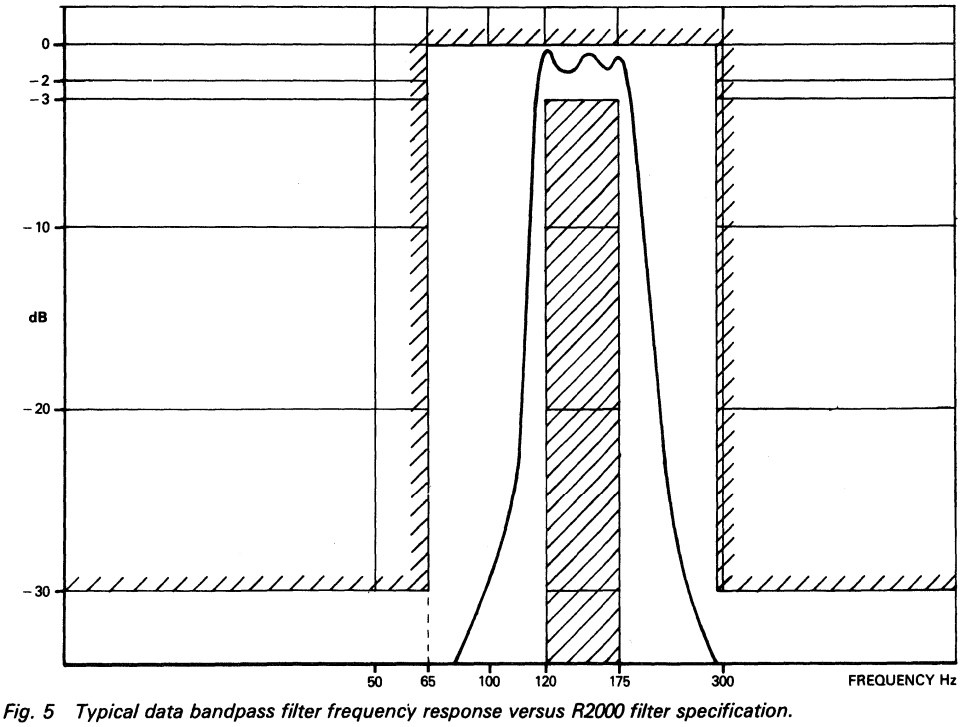


Fig. 5 Typical data bandpass filter frequency response versus R2000 filter specification.

Package Outlines

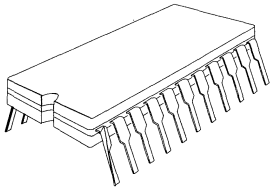
The FX336 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX336 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX336J 22-pin cerdip DIL (J3)

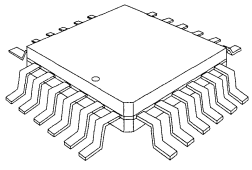
NOT TO SCALE



Max. Body Length 27.38mm
Max. Body Width 9.75mm

FX336LG 24-pin quad plastic encapsulated bent and cropped (L1)

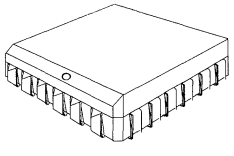
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX336LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX336J	22-pin cerdip DIL	(J3)
FX336LG	24-pin encapsulated bent and cropped	(L1)
FX336LS	24-lead plastic leaded chip carrier	(L2)

CML Semiconductor Products
PRODUCT INFORMATION

FX366 AMPS/TACS Quad Filter Array

Publication D/366/3 July 1994
Provisional Issue

Features/Applications

- **Separate Bandpass and Lowpass Gain/Filter Blocks**
- **Global AMPS/TACS Cellular Applications**
- **Bandpass Filters**
  4.5dB Gain (300Hz to 3000Hz)
- **Lowpass Filters (3000Hz)**
- **Input Gain Adjustments**
- **Output Enable/Mute for Squelch Functions**
- **Small Outline Surface Mount and DIL Packages**
- **Low-Power 5V CMOS**

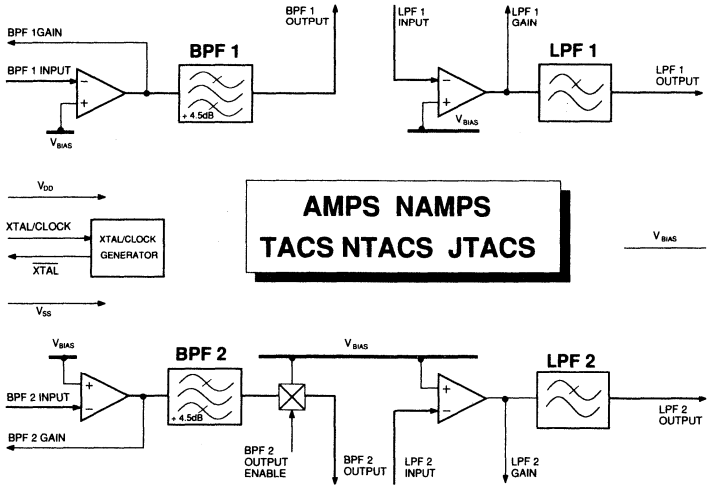


Fig.1 The FX366 Quad Filter Array

Brief Description

The **FX366** AMPS/TACS Quad Filter Array comprises 4 separate individual filter/gain blocks in a single microcircuit, containing:

2 Bandpass Filters BPF 1 and BPF 2.
– 14th order 300Hz to 3000Hz –

2 Lowpass Filters LPF1 and LPF 2.
– 10th order 3100Hz –

Each filter block has an amplifier at its input for use with external components to provide functions such as, level adjustment, pre- or de-emphasis and limiting.

BPF 2 has the added facility of Output Enable which could be used as 'audio mute' in a squelch or Inband-Mixing environment.

The provision of 2 bandpass and 2 lowpass filter sections allows 2 audio channels, each of LPF and BPF pairing for use in a full-duplex Tx/Rx cellular system.

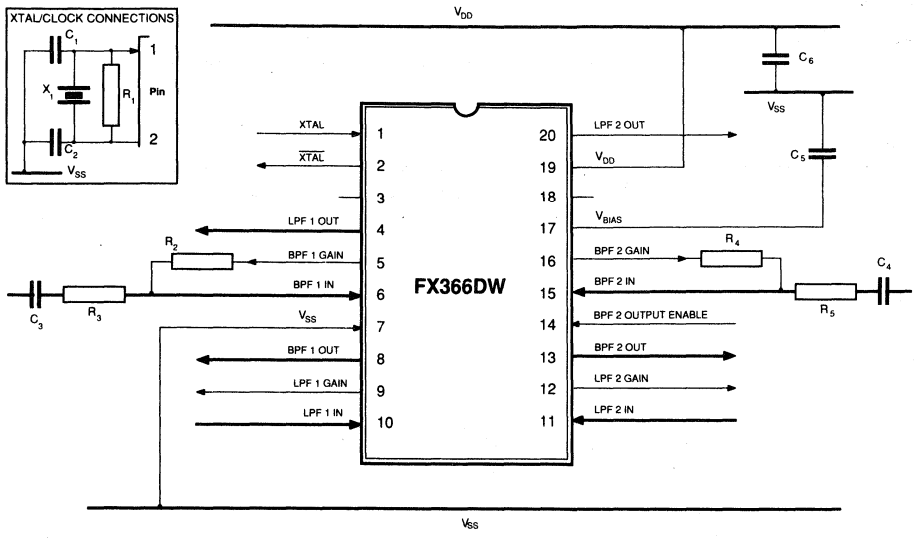
All on-chip filters meet the AMPS and TACS cellular system speechband specifications; Including NAMPS, NTACS and JTACS. Switched capacitor filter technology is employed on this chip with all switching clocks derived from an externally applied single Xtal/clock source.

These simple, comprehensive amplifier/filter combinations eliminate the need for several separate integrated circuits therefore saving power and space.

The **FX366** is a low-power, single 5V CMOS device and is available in a 22-pin cerdip Dual-in-Line and a 20-pin plastic Small Outline (S.O.I.C.) surface mount package.

Pin Number		Function
FX366DW	FX366J	
1	1	**Xtal/Clock:** A 4.433619MHz Xtal or externally derived clock is injected at this pin. Operation of the FX366 without a Xtal or clock input may cause device damage.
2	2	**$\overline{\text{Xtal}}$:** Output of the on-chip clock oscillator inverter.
4	4	**LPF 1 Output:** The output of LPF 1 filter/gain block.
5	5	**BPF 1 Gain:** The output of BPF 1 gain-adjusting amplifier. This output is used with BPF 1 Input and external components.
6	6	**BPF 1 Input:** The input to BPF 1 filter/gain block.
7	7	**V_{SS}:** Negative supply (GND).
8	8	**BPF 1 Output:** The output of BPF 1.
9	10	**LPF 1 Gain:** The output of LPF 1 gain-adjusting amplifier. This output is used with LPF 1 Input and external components.
10	11	**LPF 1 Input:** The input to LPF 1 filter/gain block.
11	12	**LPF 2 Input:** The input to LPF 2 filter/gain block.
12	13	**LPF 2 Gain:** The output of LPF 2 gain-adjusting amplifier. This output is used with LPF 2 Input and external components.
13	15	**BPF 2 Output:** The output of BPF 2. This output is under the control of the BPF 2 Output Enable input.
14	16	**BPF 2 Output Enable:** Controls the status of BFP 2 Output. Logic "1" = Enable, Logic "0" = Muted. This pin has an internal 1.0MΩ pullup resistor.
15	17	**BPF 2 Input:** The input to BPF 2 filter/gain block.
16	18	**BPF 2 Gain:** The output of BPF 2 gain-adjusting amplifier. This output is used with BPF 2 Input and external components.
17	19	**V_{BIAS}:** The internal analogue bias line at $V_{DD}/2$. This pin should be decoupled to V_{SS} by a capacitor of 1.0µF.
19	21	**V_{DD}:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within this device are dependent upon this supply.
20	22	**LPF 2 Output:** The output of LPF 2.
3, 18	3, 9, 14, 20	No internal connection. Leave open circuit.

Application Information



Component		Value
R_1	=	1.0MΩ

1. Configurations R_2, R_3, C_3 and R_4, R_5, C_4 should be chosen with respect to the specific application.
2. Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail (V_{DD}) is fitted with a current limiting device (resistor or fast-reaction fuse).

Component		Value
C_1	=	33.0pF
C_2		47.0pF
C_5		1.0µF
C_6		0.47µF
X_1		4.433619MHz

Tolerances

C = ±20% *R = ±10%*

Fig.2 Recommended External Components

The FX366 in a System

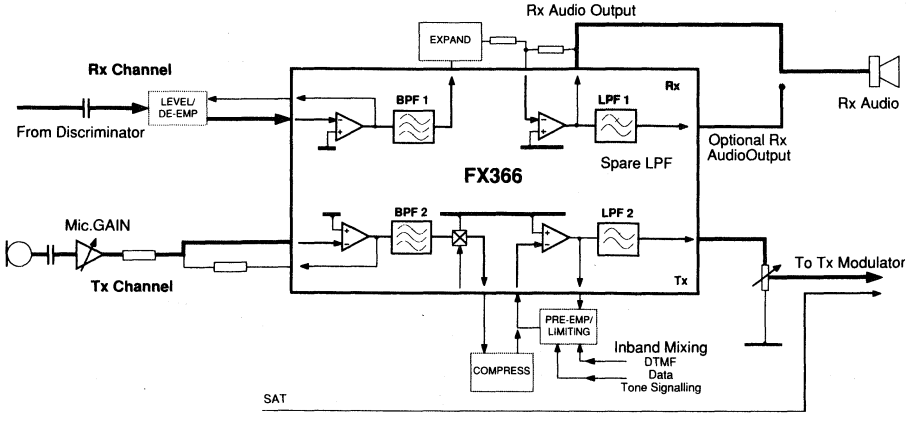


Fig.3 Example of the FX366 Employed in the Audio Stages of a TACS Application

Application Information .....

Performance

Bandpass Sections

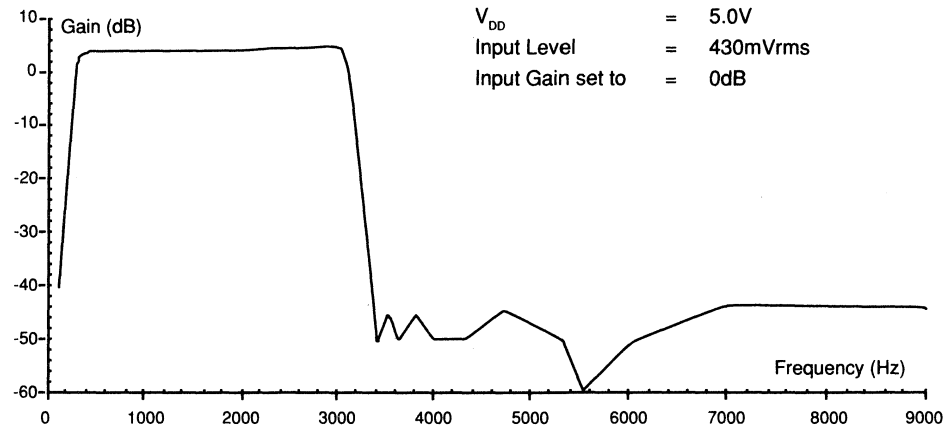


Fig.4 Example of the FX366 Bandpass (BPF1/BPF2) Frequency Response

When using the FX366 Quad Filter Array within a cellular system, the following points should be considered.

(1) Each bandpass filter section has a frequency range of 300Hz to 3000Hz and a typical passband gain of 4.5dB.

(2) Each lowpass filter section has a cut-off frequency of 3100Hz and a typical passband gain of 0.5dB.

(3) BPF2 Output Enable has an enable/disable operating time as shown on the Specification page.

Lowpass Sections

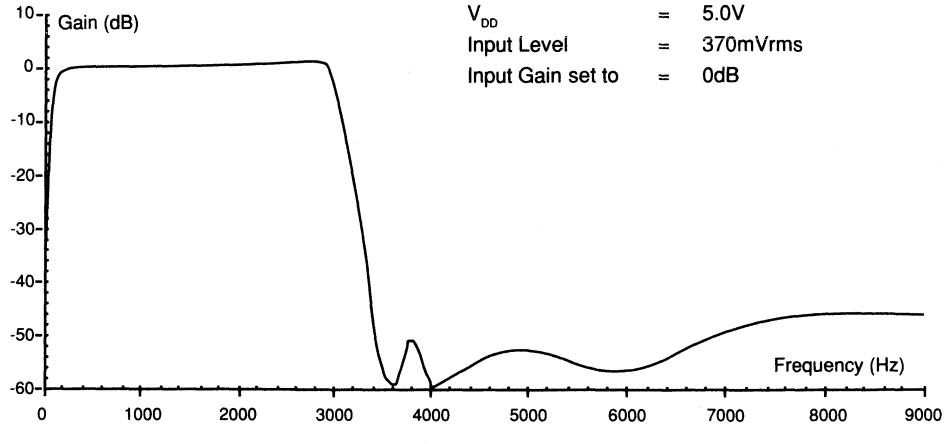


Fig.5 Example of the FX366 Lowpass (LPF1/LPF2) Frequency Response

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX366DW**	-40°C to +85°C
	FX366J	-40°C to +85°C
Storage temperature range:	**FX366DW**	-40°C to +85°C
	FX366J	-55°C to +125°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.433619MHz. Audio level 0dB ref: = 775mV rms @ 1.0kHz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current		–	5.0	–	mA
Input Impedance (Amplifiers)		1.0	10.0	–	MΩ
Input Impedance (Digital)		100	–	–	kΩ
Output Impedance (BP Filters)		–	2.0	–	kΩ
Output Impedance (LP Filters)		–	2.0	–	kΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}		–	10.0	–	kΩ
Inverter d.c. Voltage Gain		–	10.0	–	V/V
Gain/Bandwidth Product		–	10.0	–	MHz
Dynamic Values					
Input Logic "1"		3.5	–	–	V
Input Logic "0"		–	–	1.5	V
Analogue Levels					
LP Filters					
Input		-30.0	–	4.5	dB
Output		-29.5	–	5.0	dB
BP Filters					
Input		-30.0	–	-1.5	dB
Output		-26.0	–	2.5	dB
Output Noise	2	–	-50.0	–	dBp
Filters					
Bandpass Filter	**1, 3**				
Passband Frequencies		300		3000	Hz
Passband Ripple		–	±1.0	–	dB
Low Freq. Roll-Off <200Hz		12.0	–	–	dB/oct.
High Freq. – Attenuation at 3.4kHz		–	48.0	–	dB
Passband Gain		3.5	4.5	5.5	dB
Bandpass Filter 2 Output Enable					
Enable Time		–	8.0	–	µS
Disable Time		–	20.0	–	µS
Lowpass Filter	**1,3**				
Cut-Off Frequency (-3dB)		–	3100	–	Hz
Passband Ripple (300Hz - 3kHz)		–	±1.0	–	dB
Attenuation at 3.3kHz		–	30.0	–	dB
Attenuation at 3.6kHz		–	45.0	–	dB
Passband Gain		–	0.5	–	dB
Distortion	1, 4	–	2.0	–	%

Notes:

1. Measured with an audio input level of –3.8dB (500mVrms).
2. With a short circuit input, at any analogue output and the measurement psophometrically weighted.
3. With Input Amplifier gain at 0dB.
4. Measured in a 30.0kHz bandwidth.

Package Outlines

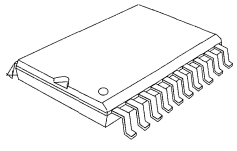
The FX366 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX366 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX366DW 20-pin plastic S.O.I.C. (D3)

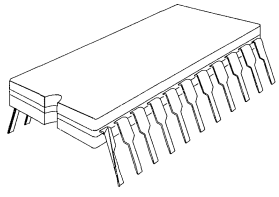
NOT TO SCALE



Max. Body Length 12.85mm
Max. Body Width 7.59mm

FX366J 22-pin cerdip DIL (J3)

NOT TO SCALE



Max. Body Length 27.38mm
Max. Body Width 9.75mm

Ordering Information

FX366DW 20-pin plastic S.O.I.C. (D3)

FX336J 22-pin cerdip DIL (J3)

CML Semiconductor Products
PRODUCT INFORMATION

FX812 Voice Store and Retrieve Codec

Publication D/812/3 July 1994
Provisional Issue

Features/Applications

- **Half-Duplex Voice Storage and Replay**
- **Serial Bus µProcessor Control**
- **On-Chip DRAM Controller**
- **Up To 2 Minutes of High-Quality Recorded Audio**
- **Answerphone and Voice-Notepad**
- **Selectable Sample Rates and "Memory Size"**
- **Small Outline (S.O.I.C.) SMD and DIL Packages**
- **Low-Power 5-Volt CMOS**

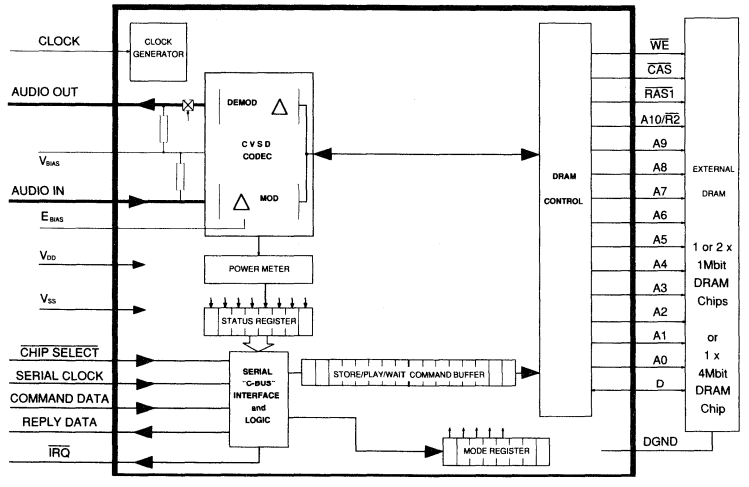


Fig.1 FX812 Voice Store and Retrieve Codec

FX812

Brief Description

The FX812 is a half-duplex VSR Codec, which when connected to an audio processing microcircuit (such as the FX816, 826 or 836), provides the storage and recovery of speechband audio in attached Dynamic RAM. The addition of this device will enhance the communications system by providing cellular radios with "Answerphone," "Message-Notepad" and general announcement facilities.

The FX812 will enable:

- Storage of a speech message for transmission (replay) at a later time.
- Storage of a received speech message when the operator is not attending.
- The storage and subsequent replay of speech.

All VSR operating functions are controlled by a simple serial µProcessor interface which may operate from the radio's own µProcessor/Controller.

Input audio from the "Store" output of the audio processor is digitized by delta modulation and stored via the DRAM controller, in attached memory.

Audio for replay is recovered from the assigned memory locations and after demodulation made available for supply to the "Play" input of the audio processor. For use with other audio systems, the input/output audio can be connected to relevant points in circuit.

The FX812 has no on-chip input or output audio filtering, this facility must therefore be provided by the host system. Sampling rates and memory capacity are selectable to 32kb/s or 63kb/s and 1 x 4Mbit or 2 x 1Mbit respectively, which when used in conjunction allow control of audio-quality and storage-time.

This low-power CMOS device is available 28-pin plastic small outline SMD and 28-pin cerdip DIL packages.

Pin Number Function

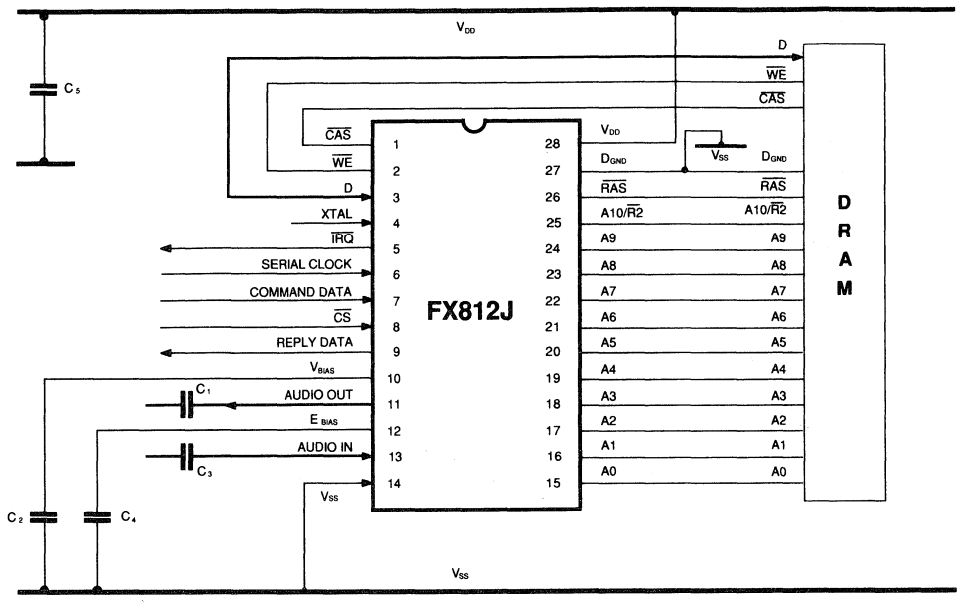
FX812DW FX812J	Function
1	**$\overline{\text{CAS}}$:** This output should be connected to the "Column Address Strobe" input pin(s) of all DRAM devices fitted.
2	**$\overline{\text{WE}}$:** This output should be connected to the "Write Enable" input pin(s) of all DRAM devices fitted.
3	**D:** Digital (speech) data into and out of the VSR Codec. This pin should be connected to the "Data In" and "Data Out" pins ("D" and "Q") of DRAM devices.
4	**Xtal:** The nominal 4.0MHz clock input to the VSR Codec. The signal applied to this device may be derived from the attached Audio Processor on-chip Xtal Oscillator circuits (see Figures 2 and 3). **Note** that the VSR Codec will be able to function and maintain correct DRAM refresh, with Xtal input frequencies down to 2.0MHz. Compand and Local Decoder time constants will change accordingly and minimum "C-BUS" timings (Figures 6 and 7) would have to be increased pro-rata.
5	**Interrupt Request ($\overline{\text{IRQ}}$):** This Interrupt Request output from the FX812 is 'wire-OR able' allowing the Interrupt Outputs of other peripherals to be commoned and connected to the Interrupt input of the µProcessor (see the CML Serial µProcessor Data Interface publication D/µINT/1 June 1991). This output has a low-impedance pulldown to V_{SS} when active, and a high-impedance when inactive.
6	**Serial Clock:** The "C-BUS" serial clock input. This clock produced by the µController, is used for transfer timing of commands and data to and from the VSR Codec. See Timing Diagrams.
7	**Command Data:** The "C-BUS" serial (command) data input from the µController. Data is loaded to this device in 8-bit bytes MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock.
8	**Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data transfer control function. This input is provided by the µController. Transfer sequences are initiated, completed or aborted by this signal. See Timing Diagrams.
9	**Reply Data:** The "C-BUS" serial data output to the µController. The transmission of reply bytes is synchronized to the Serial Clock under the control of the Chip Select input. This is a 3-state output which is held at a high-impedance when not sending data to the µController.
10	**V_{BIAS}:** The output of the internal analogue circuitry bias line, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_2 (see Figure 2).
11	**Audio Out:** The analogue output to the Audio Processor "Play" input when the VSR Codec is configured as a Decoder. When configured as an active Decoder but with no Play Page commands (62_H) active, the VSR Codec will play-out an idle pattern of "101010.....10^{s}". When not configured as a Decoder, or Powersaved (Mode Register), this output will be held at V_{BIAS} via an internal 500kΩ resistor. The output at this pin is unfiltered; An external speechband filter – such as that included on the FX816/826/836 Audio Processors – will be required. As this output is centred about $V_{DD}/2$ a coupling capacitor is required.
12	**E_{BIAS}:** The Encoder d.c. internal balancing circuitry line. This pin should be decoupled to V_{SS} by a capacitor C_4, (see Figure 2). **Note** that in the 'Encode' mode (Mode Register DE and PS both "0") the Codec drives this pin to approximately $V_{DD}/2$ through a very high impedance; It can take more than one second for the E_{BIAS} voltage to stabilize when power is first applied to this device. A faster start--up can be achieved by setting Bit DE or PS to "1" for 250mS (approx) during power-up. This will cause the E_{BIAS} pin to be connected to V_{BIAS} through a resistance of approximately 100kΩ.
13	**Audio In:** The analogue input to the VSR Codec in the Encode mode. When not configured as an Encoder, or Powersaved (Mode Register), this input will be held at V_{BIAS} via an internal 500kΩ resistor. This pin should be coupled via a capacitor, see Figure 2. As this input does not contain an internal audio filter, the audio to this pin should be limited to a 3400Hz "speechband" by an external audio filter – such as included in the FX816/826/836 Audio Processors.
14	**V_{SS}:** The "analogue" ground connection. See D_{GND} description.

Pin Number Function

FX812DW FX812J	
15	**A0:** DRAM address line outputs from the FX812. These pins should be connected to the corresponding address inputs of the associated DRAM.
16	**A1:**
17	**A2:**
18	**A3:**
19	**A4:**
20	**A5:**
21	**A6:**
22	**A7:**
23	**A8:**
24	**A9:**
25	**A10/$\overline{R2}$:** A dual function output pin selected by the memory size (MS) bit (Mode Register), as detailed in the table below:
26	**$\overline{RAS}$:** An output from the VSR Codec which should be connected to the "Row Address Strobe" pin of the 4Mbit DRAM or the first 1Mbit DRAM, see Figure 4, Example DRAM connections.
27	**D_{GND}:** The digital signal ground connection to the VSR Codec. Both D_{GND} and V_{SS} pins should be connected to the negative side of the d.c. power supply, however the printed circuit board should be laid out so that D_{GND} is connected as closely as possible to the DRAM section ground pins.
28	**V_{DD}:** Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the VSR Codec are dependent upon this supply. This pin should be decoupled to V_{SS} via capacitor C_5, located close to the FX812 pins.

MS bit	DRAMs	Connected To	This Output
"0"	1Mbits'	DRAM No 2 $\overline{RAS}$	RAS2
"1"	4Mbit	DRAM A10	A10 Signal

Application Information



Component	Value
C_1	Dependant upon the input impedance of the driven stage
C_2	1.0µF
C_3	100nF
C_4	1.0µF non-electrolytic

Tolerance: Capacitors = -50/+100%

Fig.2 Recommended External Components

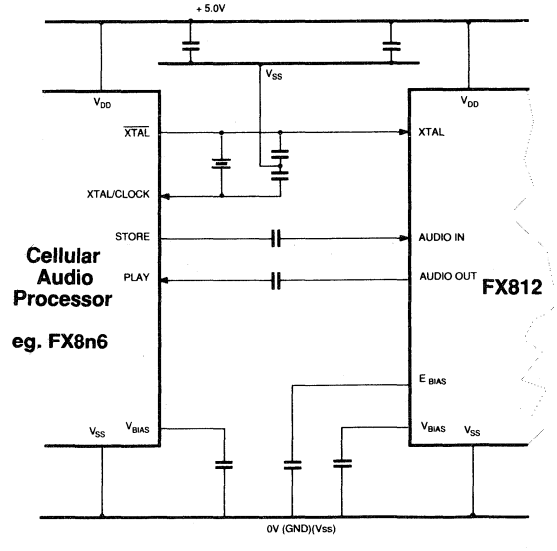


Fig.3 Interfacing to an Audio Processor

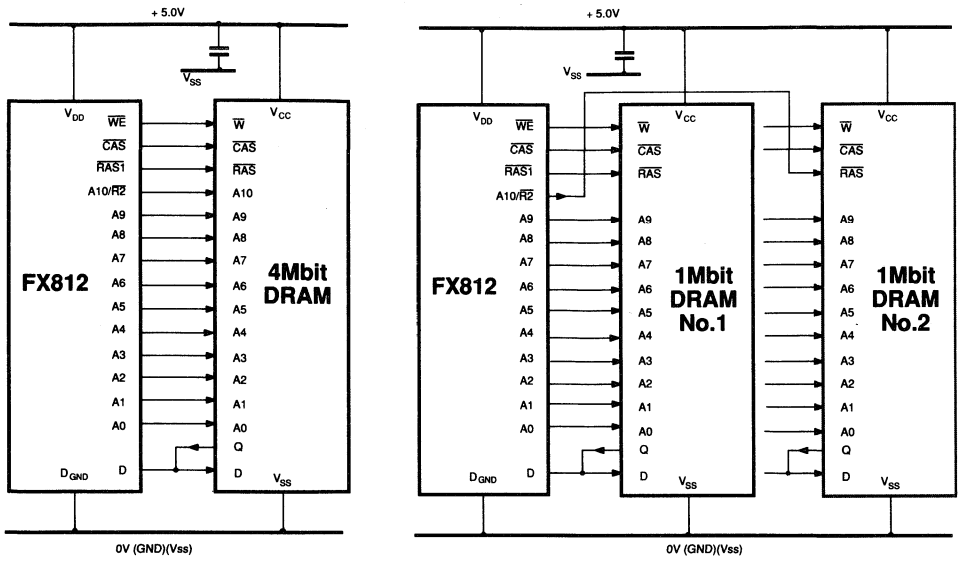


Fig.4 Example DRAM Connections

Choice of DRAM Devices

DRAM devices chosen should be standard 1,048,576 x 1 or 4,194,304 x 1 Dynamic Random Access memories, with 'CAS before RAS' refresh, and a Row Address access time of 200 nano-seconds or less.

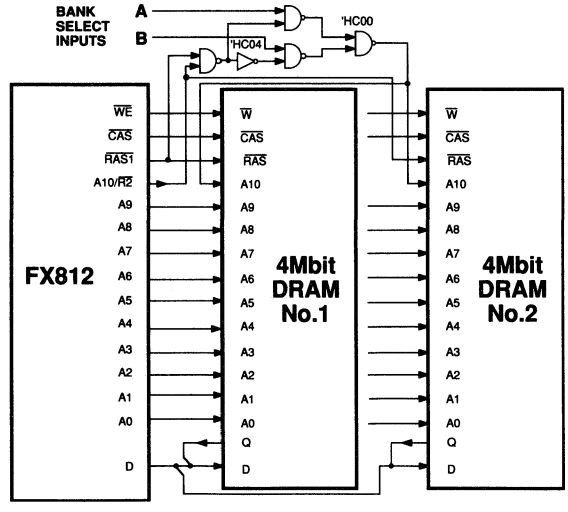


Fig.5 Employment of External Elements to Drive Two 4-MBit DRAM Chips

Driving Two 4-MBit DRAM Sections

By the addition of external logic circuitry, the FX812 can be configured to drive two 4-MBit DRAM sections. This will have the effect of doubling the available storage time. i.e. 4 minutes at 32kb/s.

With reference to the circuitry shown in Figure 5:

With the Mode Register **MS** Bit set to "0" the FX812 treats the DRAM sections as two 1-Mbit devices. The external logic makes each 4-MBit DRAM appear as four 1-MBit banks selected by the Bank Select lines '**A**' and '**B**.'

Bank Select Inputs A	B	DRAM No 1 Pages 0 – 1023	DRAM No 2 Pages 1024 – 2047
0	0	■	■
1	0	■	■
0	1	■	■
1	1	■	■

The Controlling System

"C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's New Generation microcircuits.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the FX812 VSR Codec is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the FX812.
The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB							LSB	+	Data Byte/s
General Reset	01	0	0	0	0	0	0	0	1		
Write to Mode Register	60	0	1	1	0	0	0	0	0	+	1 byte Instruction to Mode Register
Read Status Register	61	0	1	1	0	0	0	0	1	+	1 byte Reply from Status Register
Store/Play Page	62	0	1	1	0	0	0	1	0	+	2 bytes Command
Wait	63	0	1	1	0	0	0	1	1		

Table 1 – "C-Bus" Address/Commands

"Write to Mode Register" – A/C 60_H, followed by 1 byte of Command Data.

Interrupt Output – IE
Controls the FX812 IRQ output driver.

Sampling Rates – SR
The CVSD Codec sampling rates. Accurate rates depend upon the applied Xtal/clock frequency (see Table 5).

Memory Size – MS
The FX812 can operate with 1 x 1Mbit, 2 x 1Mbit or 1 x 4Mbit of DRAM (see Figure 4).

Powersave – PS
Powersaves the CVSD Codec only. Logic functions and DRAM refresh are maintained.

Decode/Encode – DE
The Codec and DRAM operational mode."
"Play" or "Store"

Setting	*Mode Bits*
MSB	***Transmitted to 812 First***
7	**Interrupt Output**
1	Enable
0	Disable
6	**Sampling Rate**
1	63kb/s
0	32kb/s
5	**Memory (DRAM) Size**
1	Single 4Mbit
0	1 or 2 x 1Mbit
4	**Powersave**
1	CVSD Codec Powersaved
0	CVSD Codec Powered
3	**Decode/Encode**
1	Decode – Play Mode
0	Encode – Store Mode
2 1 0	**Not Used**
0 0 0	Set to 'zeros'

Table 2 Control Register

Interrupts

The FX812's Interrupt Output is driven by the Status Bit 7 (IF) when the Mode Register Bit7 (IE) is set to a "1."

The IF bit and the Interrupt Output (If enabled) are set when the Store/Play/Wait command Buffer is emptied (MT bit) by transferring from the buffer to the DRAM control circuits.

and/or

The IF bit and the Interrupt Output (if enabled) are set when a Store, Play or Wait command has finished **and** the Command Buffer is empty.

The notes below illustrate the $\overline{IRQ}$ pin conditions:

IF Bit	IE Bit	$\overline{IRQ}$
"0" cleared	"0" disable	High Z
"0" cleared	"1" enable	High Z
"1" Interrupt	"0" disable	High Z
"1" Interrupt	"1" enable	V_{SS} (logic "0")

"General Reset" – A/C 01_H

Upon Power-Up the "bits" in the FX812 registers will be random (either "0" or "1"). A General Reset Command (01_H) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX812.

Clear all Mode Register bits to "0"
Status Register Bit 7 (IF) to "0"
Bits 5 and 6 (MT and I) to "1"
Halt any current Store, Play or Wait execution
Clear the Store/Play/Wait Command Buffer

"Read Status Register" – A/C 61_H, followed by 1 byte of Reply Data.

Reading	*Status Bits*
MSB	***Received from 812 First***
7	**Interrupt Condition (Flag)**
1	Bit 6 or 5 set to a "1"
0	Cleared condition
6	**Command Buffer**
1	Buffer Empty
0	Cleared condition
5	**Device Condition**
1	Idle
0	Storing, Playing or Waiting
4 3 2 1 0	**Input Power Level**

Table 3 Status Register

Interrupt Condition (Flag) – IF

Set to a logic "1" whenever Bit 6 or Bit 5 goes from "0" to "1" (unless the transition is caused by a "General Reset" command 01_H). This indication allows monitoring by 'poll' whilst Interrupts are disabled.
Cleared to a logic "0" by a General Reset command or immediately following a read of the Status Register.

Command Buffer Status – MT

Set to a logic "1" when the Command Buffer is empty or by a General Reset command.
Cleared to a logic "0" by loading a new Store, Play, Wait commands.

Device Condition – I

Set to a logic "1" when **NO** Store, Play or Wait command is being executed or by a General Reset command.
Set to a logic "0" whilst a Store, Play or Wait command is being executed.

Encode Input Power Level – POWER

Available in the Encode mode, a 5-bit representation of the analogue signal input level, updated at the end of every Store or Wait command.

Store/Play/Wait Command Buffer

A buffer used to accept and hold the latest Store, Play or Wait command received over the "C-BUS" while the FX812 is executing the previous command. The Status Register, bit 6, indicates the condition of this buffer.

When a command is received it is first loaded into this buffer. If the FX812 is already executing a previously loaded Store, Play or Wait command the new command will be stored temporarily in the Command Buffer from where it will be taken on completion of the previous command.

This permits the FX812 to perform a continuous sequence of Store, Play or Wait commands, without gaps and without requiring an unduly fast response from the µController.

Note that this Command Buffer can only hold one Store, Play or Wait instruction, each new command received into this buffer will overwrite any previously loaded contents.

To Store or Play a sequence of pages the relevant commands should be loaded with sequential page numbers whilst observing the Status Register – Bit 6.

"Store/Play Page" – A/C 62_H, followed by 2 bytes of Command Data.

For the purposes of storage and replay, the attatched DRAM is divided into 'data-pages' of 1024 bits (1kbit).
One Store/Play command (loaded MSB first) will instruct the FX812 to store or play (depending upon the setting of the Mode Register, Bit-3) to or from 1 x 1024 "page" of DRAM. The Store/Play/Wait command buffer will allow continuity of operation.

The particular page selected is identified by the 12 lowest bits of the 2 x Store/Play bytes as shown below.
If a Store command is loaded and executed whilst the Codec is "Powersaved" in the Encode mode, the selected DRAM page will be filled with an idle pattern ("101010.....").

					Bit Number												
	MSB – Loaded to FX812 First															*Loaded Last – LSB*	
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Bit**
Value	**x**	**x**	**x**	**x**	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	**Value**
Page	"0"	"0"	"0"	"0"	DRAM Page Number												Page

DRAM Size	Valid Page Nos	Bit Nos
4Mbit	0 – 4095	0 – 11
1 + 1Mbit	0 – 2047	0 – 10
1Mbit	0 – 1023	0 – 9

"Wait" – A/C 63_H, — Wait for 1024 bit periods

Causes the FX812 to wait for 1024 bit periods (approximately 16 0r 32msec).
If the Codec is set to the Encode mode, a new "Power" reading that is relevant to the input audio level, will be loaded into the Status Register at the end of the Wait period.
If the Codec is set to the Decode mode it will 'Play' a perfect idle pattern ("101010.....") during the Wait period.

Control Timing Information

Control Timing

Figure 6 shows the timing parameters for two-way communication between the µController and Cellular peripherals on the "C-BUS." Figure 7 shows the timing relationships between the Serial Clock and Data.

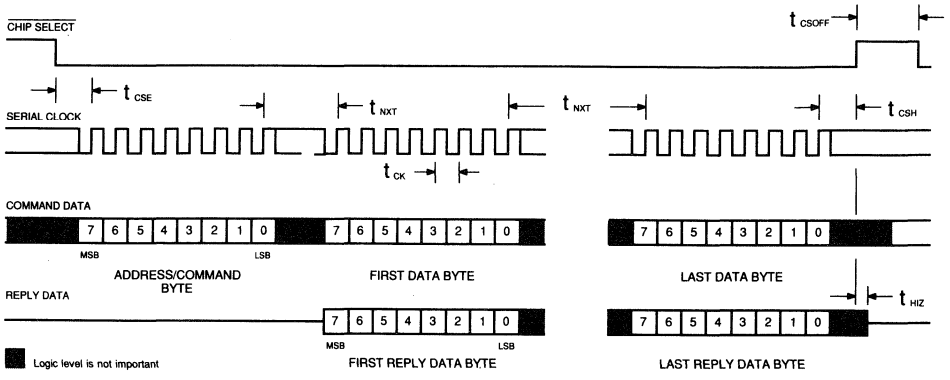


Fig.6 Control Timing Information

NOT TO SCALE

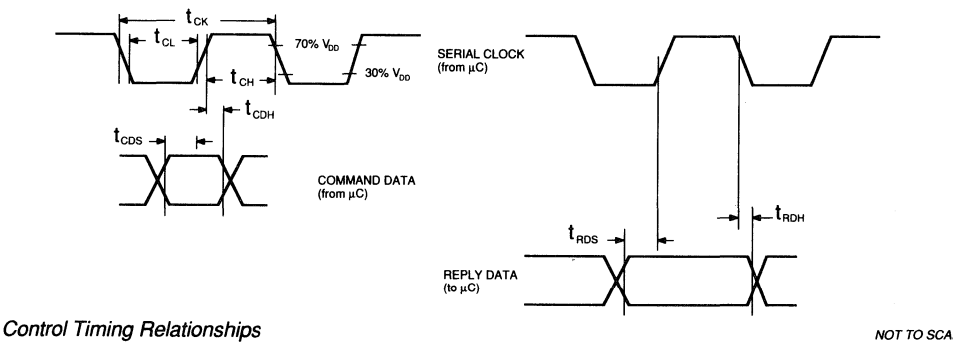


Fig.7 Control Timing Relationships

NOT TO SCALE

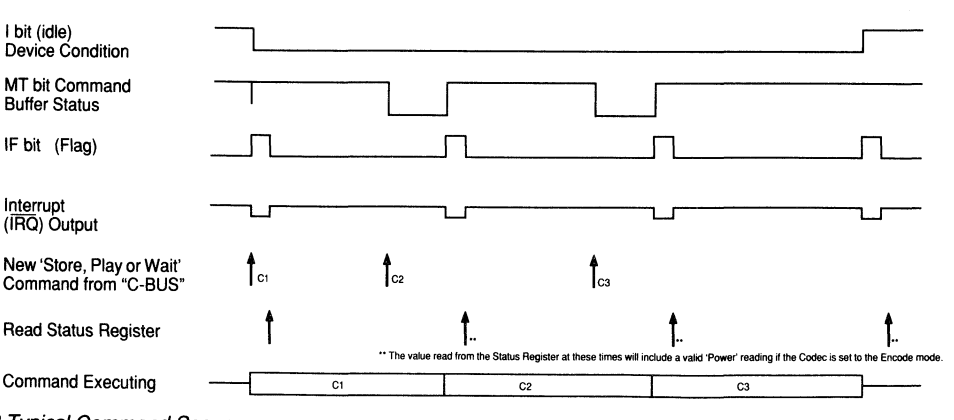


Fig.8 Typical Command Sequences

Control Timing Information .....

Timing Specification – Figures 6 and 7

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"		2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"		4.0	–	–	µs
t_{HIZ}	"CS-High to Reply Output Tri-state"		–	–	2.0	µs
t_{CSOFF}	"CS-High" Time between transactions		2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time		2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time		4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns
t_{RDS}	"Reply Data Set-Up" Time		250	–	–	ns
t_{RDH}	"Repy Data Hold" Time		50.0	–	–	ns

Address Line Decoding

MA0 to MA21 are the outputs of the internal 22-bit DRAM address counter, which are time multiplexed as 'Row' and 'Column' addresses onto the DRAM address lines A0 to A10 etc., as shown below.

Memory Size (MS) Bit = "1" – 4Mbit DRAM

Pin	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10/R2
Row Address	MA0	MA2	MA4	MA6	MA8	MA10	MA12	MA14	MA16	MA18	MA20
Column Address	MA1	MA3	MA5	MA7	MA9	MA11	MA13	MA15	MA17	MA19	MA21

Memory Size (MS) Bit = "0" – 1Mbit DRAM(s)

Pin	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9
Row Address	MA0	MA2	MA4	MA6	MA8	MA10	MA12	MA14	MA16	MA18
Column Address	MA1	MA3	MA5	MA7	MA9	MA11	MA13	MA15	MA17	MA19

MA20	MA21	RAS1	A10/R2	DRAM Selected
0	x	active		"first"
1	x		active	"second"

x = don't care

Table 4 Address Line Decoding

		Xtal/clock Frequency (MHz)		
		4.0	4.032	4.096
Sample Rate (SR) Bit	Division Ratio	Sampling Rate (kbits/s)		
SR = "1"	64	62.50	63.00	64.00
SR = "0"	128	31.25	31.50	32.00
		Internal Clock Rate (kHz)		
Local Decoder Clock		125.0	126.0	128.0

Table 5 Sampling Clock Rates Available

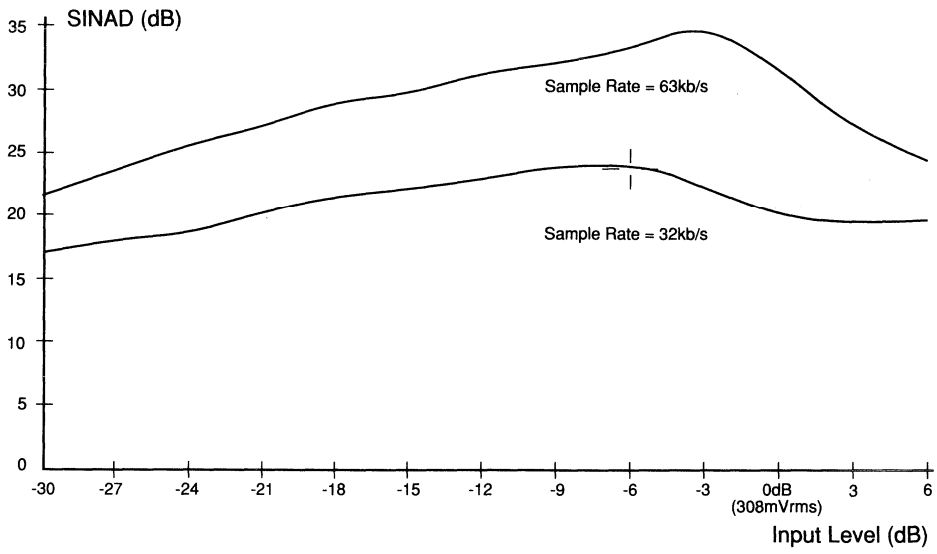


Fig.9 Typical "SINAD vs Input Level" Plot

Performance

Figure 9 Shows a typical graph of SINAD vs Input Level produced for both 32kb/s and 63kb/s sample rates at an input frequency of 1.0kHz.

Figure 10 shows a typical graph of the "Power" reading for increasing input signal levels. The "Power" figure (0 to 31) is the binary figure obtained from the 5-bit representation in the Status Register - Bits 0, 1, 2, 3 and 4 whilst the Codec is selected to the Encode mode.

This reading is updated at the end of every Store or Wait command; Excessive input signal levels will record "11111_2" (31_{10}).

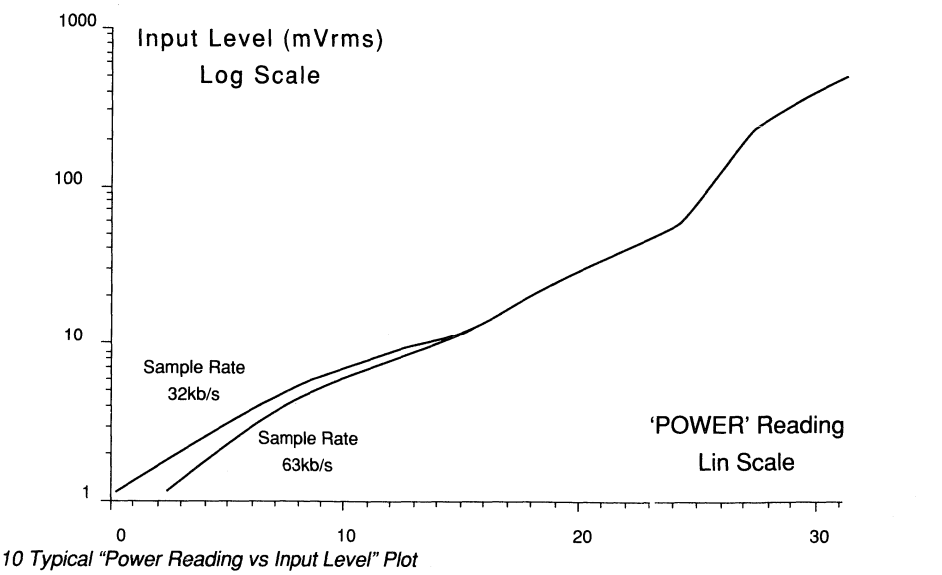


Fig.10 Typical "Power Reading vs Input Level" Plot

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref. V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX812DW**	-40°C to +85°C (plastic)
	FX812J	-40°C to +85°C (cerdip)
Storage temperature range:	**FX812DW**	-40°C to +85°C (plastic)
	FX812J	-55°C to +125°C (cerdip)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.00MHz. Audio level 0dB ref: = 308mV rms @ 1.0kHz. Reply Data Line loaded with 50pF//200kΩ to V_{SS}.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Enabled	1	–	3.0	–	mA
Powersaved	1	–	1.0	–	mA
Analogue Input Impedance		–	100	–	kΩ
Analogue Output Impedance (Decode)		–	1.0	–	kΩ
Analogue Output Impedance (Encode or Powersave)		–	500	–	kΩ
DRAM Interface					
Input Logic "1"	2	3.5	–	–	V
Input Logic "0"	2	–	–	1.5	V
Output Logic "1" (at I_o = -120µA)	3	2.7	–	–	V
Output Logic "0" (at I_o = 120µA)	3	–	–	0.4	V
Input Leakage Current (at V_{IN} = 0 to V_{DD})	4	-1.0	–	1.0	µA
Input Capacitance	2	–	10.0	–	pF
Digital Interface					
Input Logic "1"	5	3.5	–	–	V
Input Logic "0"	5	–	–	1.5	V
I_{IN} (logic "1" or "0")	5	-1.0	–	1.0	µA
Output Logic Levels					
Output Logic "1" (-120µA)	6	4.6	–	–	V
Output Logic "0" (360µA)	7	–	–	0.4	V
I_{Out} Tri-state (logic "1" or "0")	6	-4.0	–	4.0	µA
Input Capacitance	5	–	–	7.5	pF
IOX (V_{Out} = 5V)	8	–	–	4.0	µA
Dynamic Values					
"Xtal" Pin Input Frequency Range	12	4.0		4.1	MHz
Store Mode					
Analogue Input Signal Levels	9	-24.0	–	4.0	dB
Analogue Input Signal Frequency Range	9, 10	300		3400	Hz
Recommended Signal Source Impedance	9	–	–	2.0	kΩ
Play Mode					
Analogue Output Signal Levels	13	-7.0	–	-5.0	dB
Output Noise (idle)	11	–	-55.0	–	dBp
Overall 'Store to Play' Performance					
Output Noise (Input Short Circuit)	11	–	-50.0	–	dBp
SINAD (**SR** = 32kb/s) (Input = 1.0kHz @ -6.0dB)	11	–	23.0	–	dB

Notes

1. Not including DRAM current.
2. D input from DRAM
3. Outputs to DRAM.
4. All digital inputs.
5. Serial Clock, Command Data and Chip Select inputs.
6. Reply Data output.
7. Reply Data and Interrupt ($\overline{IRQ}$) outputs.
8. Leakage current into the "Off" Interrupt ($\overline{IRQ}$) output.
9. For optimum performance.
10. Input filtering must be performed at the source.
11. Measured in conjunction with the FX836 R2000 system Audio Processor.
12. For full "C-BUS" compatibility.
13. Playback of a stored "-6.0dB 1.0kHz Test Signal."

Package Outlines

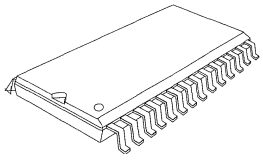
The FX812 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX812 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX812DW 28-pin plastic S.O.I.C. (D1)

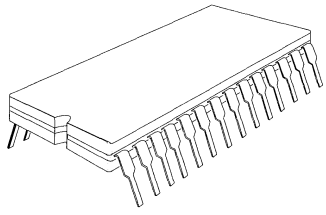
NOT TO SCALE



Max. Body Length 18.05mm
Max. Body Width 7.65mm

FX812J 28-pin cerdip DIL (J5)

NOT TO SCALE



Max. Body Length 37.05mm
Max. Body Width 13.36mm

Ordering Information

FX812DW 28-pin plastic S.O.I.C. (D1)

FX812J 28-pin cerdip DIL (J5)

CML Semiconductor Products
PRODUCT INFORMATION

FX816 NMT System Audio Processor

Publication D/816/3 July 1994
Provisional Issue

Features/Applications

- **Full-Duplex Audio Processing for NMT Cellular System**
- **On-Chip Speech and SAT Facilities**
  – Tx/Rx/SAT Filtering & Gain – VOGAD – Pre-/De-Emphasis – Deviation Limiter –
- **Serial µProcessor Interface**
- **Separate SAT Channel**
- **"Sidetone" Output Available**
- **HandsFree Compatibility**
- **Access to External Processes**
  – Compression – Expansion – Signalling/Data Mixing – VSR Codec (Store/Play) –
- **Powersave (Low-Current) Settings**

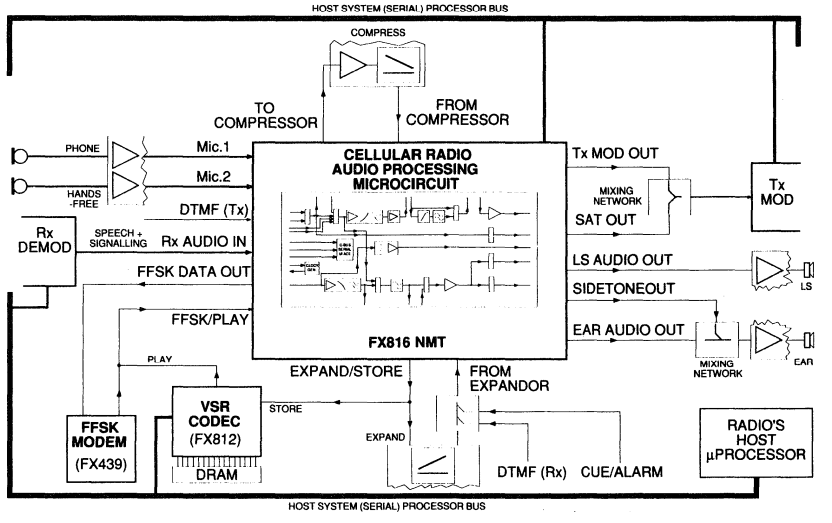


Fig.1 The FX816 NMT Audio Processor Installed within a Cellular System

FX816

Brief Description

The FX816 is a µProcessor controlled full-duplex audio processor on a single-chip with separate Tx and Rx paths to provide all the filter/gain/limiting functions necessary to pre-process audio, data and signalling in the Nordic Mobile Telephone (NMT) cellular communications system.

Selectable inputs available to the transmit path are: a choice of two microphones, DTMF/signalling or FFSK/data, with access, in this path, to external compression circuitry. Operationally the Tx path provides input gain/filtering, VOGAD, a deviation limiter and Tx Modulation Drive controls.

In the Rx path the SAT signal is separated from the incoming audio via a gain/filter block and made available at a separate pin for mixing externally with the Tx Modulation Drive.

The Rx path consists of an input gain/filter block for voice and data, inputs from an external audio expansion system and an output gain control driving either a loudspeaker system or earpiece.

Unique to the FX816/826/836 cellular audio processors is the ability to route audio (Tx or Rx) to an external Voice Store and Retrieve (VSR) device such as the FX802 or FX812 thus providing the radio system with a voice answering and announcement facility using external DRAM.

The FX816, a low-power CMOS device, which reduces the amount of microcircuits and components required in a cellular audio system by providing more functions on a single chip, is available in 28-pin plastic small outline (S.O.I.C.) surface mount and cerdip DIL packages.

Pin Number Function

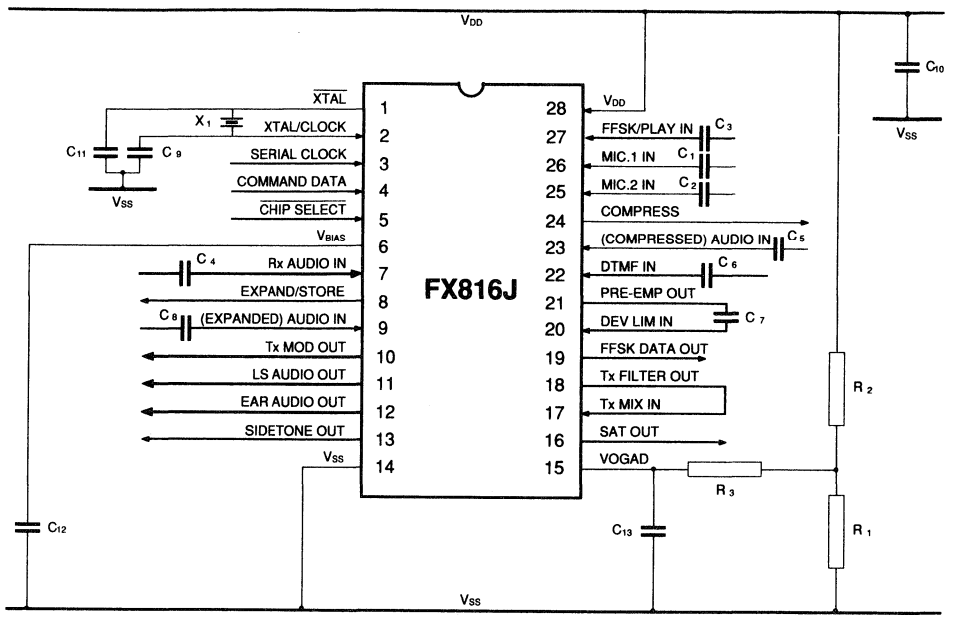
FX816DW	FX816J	
1	1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	2	**Xtal/Clock:** The input to the on-chip clock oscillator. A Xtal or externally derived clock (f_{XTAL}) should be connected here. Note that operation of the FX816 without a suitable Xtal or clock input may cause device damage. See Figure 2 (notes).
3	3	**Serial Clock:** The "C-BUS" serial data clock input. This clock, produced by the µController, is used for transfer timing of commands and data to the FX816. See Timing Diagrams.
4	4	**Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to the FX816 in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams.
5	5	**Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing Diagrams.
6	6	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS}. See Figure 2.
7	7	**Rx Audio In:** Normally taken from the radio's discriminator output, this input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor.
8	8	**Expand/Store:** A common output that can be used as either an input to an external audio expander or the input to a voice storage medium such as the FX812. Components relevant to the external device requirements should be used at this output. See Figures 2 and 3.
9	9	**(Expanded) Audio In:** The audio input, via SW5, from an external expander or audio mixing function. This input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor. See Figures 2 and 3.
10	10	**Tx Mod Out:** The composite Tx audio output to the transmitter modulator from a variable attenuation stage (11_H). This output is set to V_{BIAS} via an internal 1MΩ resistor when set to Powersave or OFF.
11	11	**LS Audio Out:** An audio output of the Rx path (or selected audios, see Figures 3 and 4) for a loudspeaker system. This is available for handsfree operation. This output can be connected to V_{BIAS} when not required, by SW6 (Configuration Command (10_H)). A driver amplifier may be required.
12	12	**Ear Audio Out:** An audio output of the Rx path (or selected audios, see Figures 3 and 4), available as an output for a handset earpiece. This output in parallel with the LS Audio Out function, can be connected to V_{BIAS} when not required, by SW7 (Configuration Command (10_H)). A driver amplifier may be required.
13	13	**Sidetone:** A switched "sidetone" from the microphone inputs made available for mixing externally with the "Ear" audio. See Figure 3.
14	14	**V_{SS}:** Negative supply rail. Signal ground.
		Notes on Inputs: *To minimize aliasing effects, lowpass filtering may be required at the inputs to this device (especially those supplied from switched-capacitor-type devices) to ensure the input spectrum is kept below 63kHz.*

Pin Number Function

FX816DW	FX816J	Function
15	15	**VOGAD:** External components (R and C) at this pin control the attack and decay time constants of the on-chip VOGAD function.
16	16	**SAT Out:** The output of the SAT bandpass filter. This level, which is recovered from the input Rx audio. This tone level can be modified by the SAT and Powersave Command (13_H) and is available for mixing externally with the transmitter modulation. See Figures 3 and 4.
17	17	**Tx Mix In:** An input and output available, with external components, to introduce signalling tones into the Tx Path prior to the final level adjustment.
18	18	**Tx Filter Out:**
19	19	**FFSK Out:** The de-emphasized Rx audio output available for access to the received FFSK data. This output could be directed to an FFSK Modem such as the FX439.
20	20	**Deviation Limiter In:** Input to the on-chip deviation limiter. This input should be a.c. coupled to the Pre-Emphasis Out pin. The a.c. coupling will achieve the best possible symmetry of limiting as this input has a 1MΩ internal resistor to V_{BIAS}. See Figure 2.
21	21	**Pre-Emphasis Out:** Audio output from the VOGAD circuitry in the Tx Input Gain/Pre-Emphasis function. This output should be a.c. coupled to the Deviation Limiter In pin. See Figure 2.
22	22	**DTMF In:** To introduce DTMF type audio, at a suitable level for transmission, to the Tx Path, controlled by SW2 (Configuration Command (10_H)). This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
23	23	**Compression In:** The audio input from an external compression system. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
24	24	**Compression:** The output to an external audio compression system. Currently available compressor/ expanders have Op-Amps incorporated. The compressor can be by-passed by SW2.
25	25	**Mic.2 In:** Tx voice (Mic.) inputs, selectable by SW1 available for handsfree mic./handset mic. or any Tx audio input. Pre-amplification may be required at these inputs. These inputs each have an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
26	26	**Mic.1 In:**
27	27	**FFSK/Play In:** The Tx FFSK data input via SW2. This can also be used to input (replay) from a voice storage device such as the FX812. This "replayed" audio can be sent to Rx or Tx paths allowing a Messaging/Voice Notepad/Answering facility. Both FX439 FFSK Modem and FX812 VSR Codec outputs can be wired directly to this pin if the functions are activated one-at-a-time. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
28	28	V_{DD}: Positive supply rail. A single +5-volt power supply is required. Levels and voltages within this Audio Processor are dependent upon this supply.

"C-BUS" *is CML's proprietary standard for the transmission of commands and data between a µController and the relevant Cellular microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController. For further details refer to CML Publication No. D/µINT/1 June 1991.*

Application Information



R_1	=	100kΩ	C_2	=	100nF	C_6	=	100nF	C_{10}	=	100nF
R_2		100kΩ	C_3		100nF	C_7		100nF	C_{11}		33pF
R_3		2.2MΩ	C_4		100nF	C_8		100nF	C_{12}		1.0µF
C_1		100nF	C_5		100nF	C_9		33pF	C_{13}		0.1µF
									X_1		4.032MHz

Tolerances – Resistors ±10% Capacitors ±20%

Fig.2 Recommended External Components

Notes

1. **Xtal/clock operation**
Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail (V_{DD}) is fitted with a current limiting device (resistor or fast-reaction fuse).

2. **VOGAD components**
R_1, R_2, R_3 and C_{13} with the VOGAD Pin internal impedance, form the VOGAD timing circuitry.
Control-Voltage Attack Time is set by
C_{13} x Internal Impedance.
Control-Voltage Decay Time is set by
C_{13} x R_3 – *assuming* $R_3 >> R_1$ *and* R_2.

3. **FFSK Modem**
The FX469, a general purpose FFSK Modem could be employed with this NMT system Audio Processor. The FX469 is a non-formatted modem, which with due regard to Xtal/clock frequencies and µProcessor interface, is compatible with both Mobile/Portable and Base Station applications.

4. **SAT Output**
It is possible, due to the high output impedance of this output, that an external buffer amplifier is required at this output when interfacing or mixing with other system sections.

NMT Cellular System Interfaces

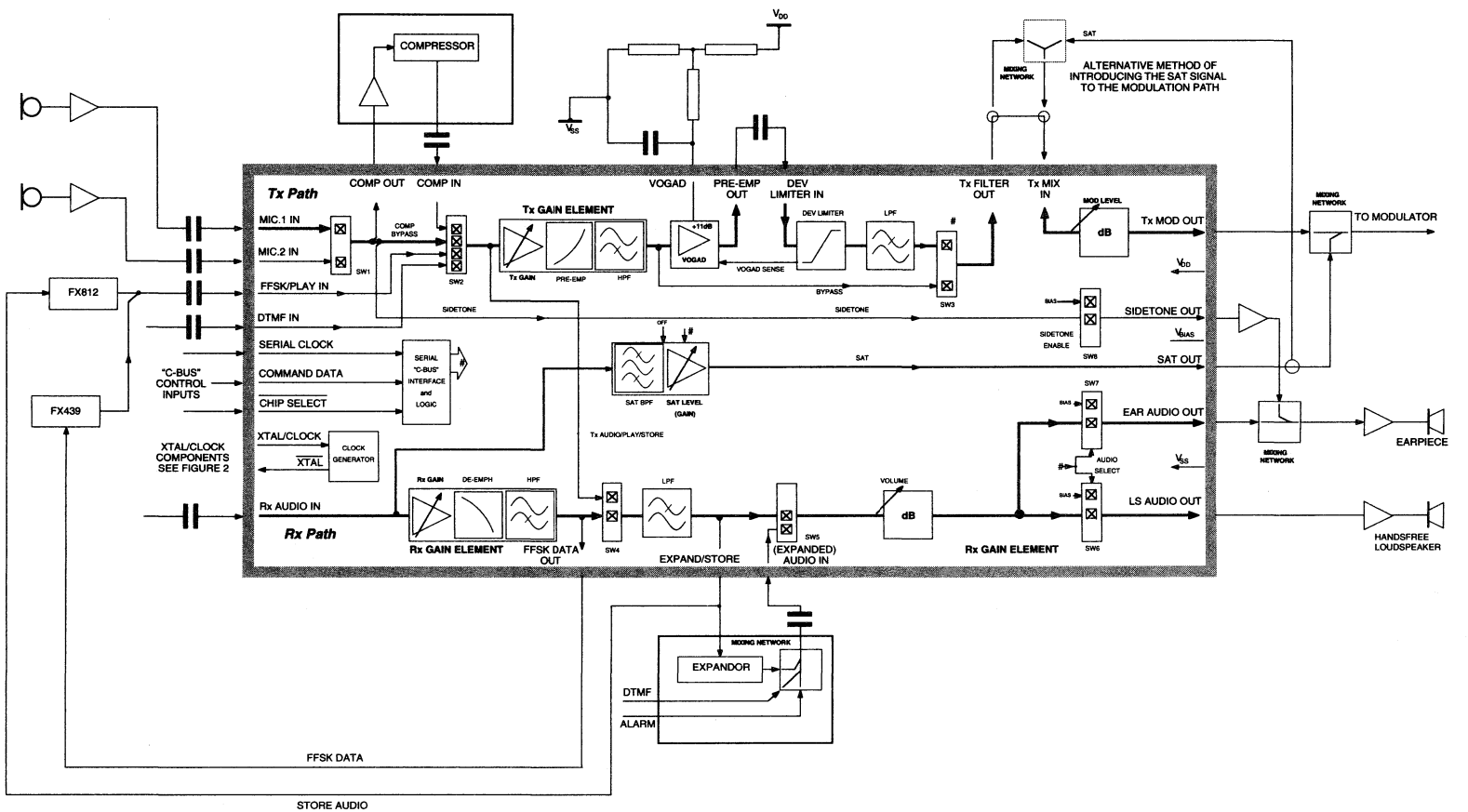


Fig.3 The FX816 within an NMT Cellular Radio System

The Controlling System

"C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's New Generation microcircuits.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the FX816 NMT Audio Processor is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the device.
The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex	Binary MSB LSB		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Configuration Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
Tx Gain & Mod. Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
Rx Gain & Vol. Command	12	0 0 0 1 0 0 1 0	+	1 byte	4
SAT & P/Save Command	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 "C-Bus" Address/Commands

In "C-BUS" protocol the audio processor is allocated Address/Command (A/C) values 10_H to 13_H. Configuration, Tx/Rx Gains and SAT/Powersave assignments and data requirements are given in Table 1.
Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the "C-BUS" interface recognises the first byte after Chip Select (logic "0") as an Address/Command. Function or Level control data, which is detailed in Tables 2, 3, 4 and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams–Figures 5 and 6.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). A **General Reset Command (01_H)** will be required to set all FX816 registers to 00_H.

Configuration Command *(Preceded by A/C 10_H)*

Setting		*Control Bits*
MSB		***Transmitted First***
Bit 7		**Sw8 Sidetone**
0		Sidetone Bias
1		Sidetone Enabled
6		**Sw6/7 Rx Audio**
0		Ear Enabled, LS Bias
1		LS Enabled, Ear Bias
5		**Sw5 Expander**
0		Expander By-Pass
1		Expander Route
4		**Sw4 Tx/Rx Audio**
0		Tx Store/Audio
1		Rx Store/Audio
3		**Sw3 Dev. Limiter**
0		Dev. Limiter By-Pass
1		Dev. Limiter Route
2		**Sw1 Mic. Inputs**
0		Mic. 1 Input
1		Mic.2 Input
1	***0***	**Sw2 Tx Function**
0	0	DTMF In
0	1	Compressor In
1	0	Compressor By-Pass
1	1	FFSK/Play In

Table 2 Configuration Commands

Tx Gain & Mod. Command *(Preceded by A/C 11_H)*

Setting				*Gain (dBs)*
MSB				***Transmitted First***
7	***6***	***5***	***4***	**Tx Mod. Level**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-5.6
0	0	1	0	-5.2
0	0	1	1	-4.8
0	1	0	0	-4.4
0	1	0	1	-4.0
0	1	1	0	-3.6
0	1	1	1	-3.2
1	0	0	0	-2.8
1	0	0	1	-2.4
1	0	1	0	-2.0
1	0	1	1	-1.6
1	1	0	0	-1.2
1	1	0	1	-0.8
1	1	1	0	-0.4
1	1	1	1	0
3	***2***	***1***	***0***	**Tx Input Gain**
0	0	0	0	-2.65
0	0	0	1	-2.05
0	0	1	0	-1.50
0	0	1	1	-0.95
0	1	0	0	-0.45
0	1	0	1	0
0	1	1	0	0.45
0	1	1	1	0.85
1	0	0	0	1.25
1	0	0	1	1.65
1	0	1	0	2.05
1	0	1	1	2.40
1	1	0	0	2.70
1	1	0	1	3.05
1	1	1	0	3.35
1	1	1	1	3.65

Table 3 Tx Gain & Mod. Commands

The Controlling System .....

Rx Gain & Vol. Command *(Preceded by A/C 12_H)*

Setting				Gain (dBs)
MSB				**Transmitted First**
7	**6**	**5**	**4**	**Rx LS Volume**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-28.0
0	0	1	0	-26.0
0	0	1	1	-24.0
0	1	0	0	-22.0
0	1	0	1	-20.0
0	1	1	0	-18.0
0	1	1	1	-16.0
1	0	0	0	-14.0
1	0	0	1	-12.0
1	0	1	0	-10.0
1	0	1	1	-8.0
1	1	0	0	-6.0
1	1	0	1	-4.0
1	1	1	0	-2.0
1	1	1	1	0
3	**2**	**1**	**0**	**Rx Input Gain**
0	0	0	0	3.75
0	0	0	1	4.30
0	0	1	0	4.80
0	0	1	1	5.30
0	1	0	0	5.80
0	1	0	1	6.20
0	1	1	0	6.55
0	1	1	1	7.05
1	0	0	0	7.40
1	0	0	1	7.80
1	0	1	0	8.15
1	0	1	1	8.50
1	1	0	0	8.80
1	1	0	1	9.10
1	1	1	0	9.40
1	1	1	1	9.70

Table 4 Rx Gain and Vol. Commands

SAT & P/Save Command *(Preceded by A/C 13_H)*

Setting				Control Bits
MSB				**Transmitted First**
Bit 7				
0				Must be a logic "0"
6				
0				Must be a logic "0"
5	**4**	**3**	**2**	**SAT Tone Level**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-1.95
0	0	1	0	-1.40
0	0	1	1	-0.90
0	1	0	0	-0.45
0	1	0	1	-0
0	1	1	0	0.40
0	1	1	1	0.85
1	0	0	0	1.20
1	0	0	1	1.60
1	0	1	0	1.95
1	0	1	1	2.30
1	1	0	0	2.60
1	1	0	1	2.90
1	1	1	0	3.25
1	1	1	1	3.50
1				**Powersave Rx Gain Element**
0				Powersave Element
1				Enable Element
0				**Powersave FX816** (except Rx Gain Element)
0				Powersave FX816
1				Enable FX816

Table 5 SAT and Powersave Commands

Reference Signal Levels

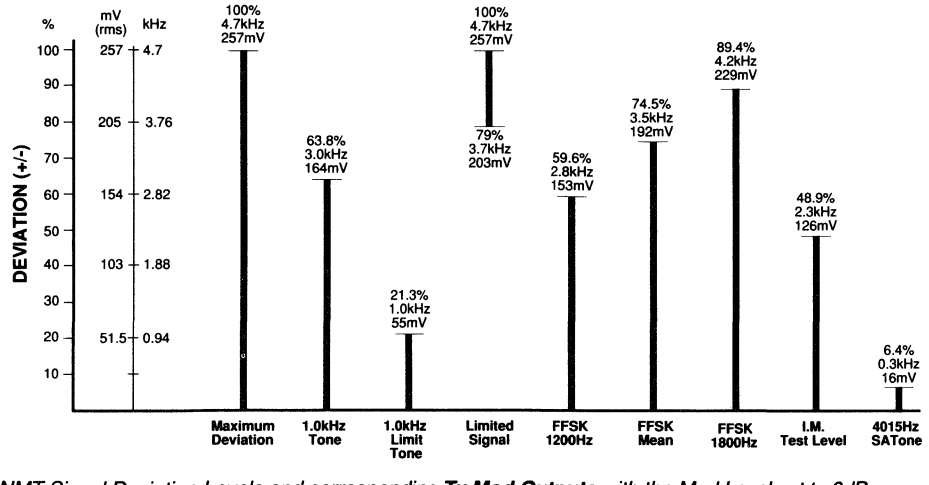


*Fig.4 NMT Signal Deviation Levels and corresponding **Tx Mod Outputs** with the Mod Level set to 0dB*

Control Timing Information

Timing Specification – Figures 5 and 6.

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"	1	2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"	1	4.0	–	–	µs
t_{CSOFF}	"CS-High" Time between transactions	1, 2	2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time	1	2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time	1	4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns

Notes

1. These Minimum Timing values are altered during operation of the FX812 VSR Codec.
2. Chip Select must be taken to a logic "1" between each individual transaction.

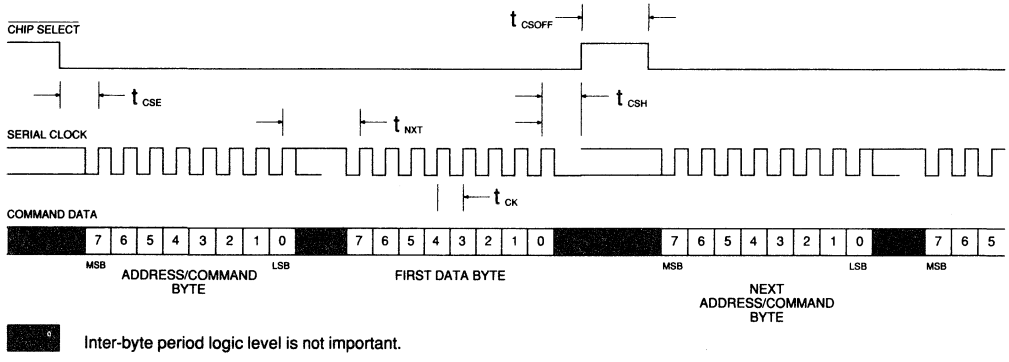


Fig.5 Control Timing Information

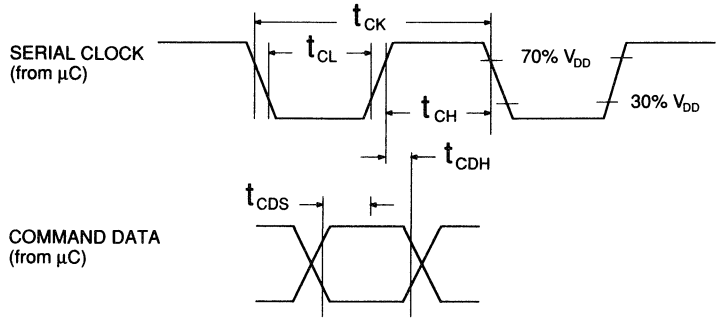


Fig.6 Control Timing Relationships

System Performance

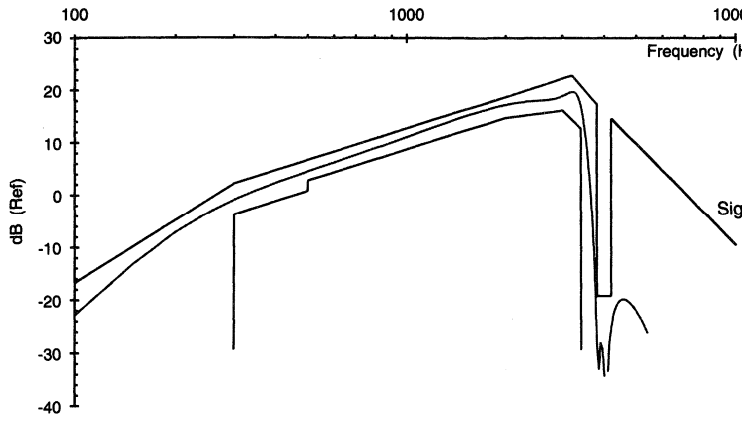


Fig.7 Tx Frequency Response

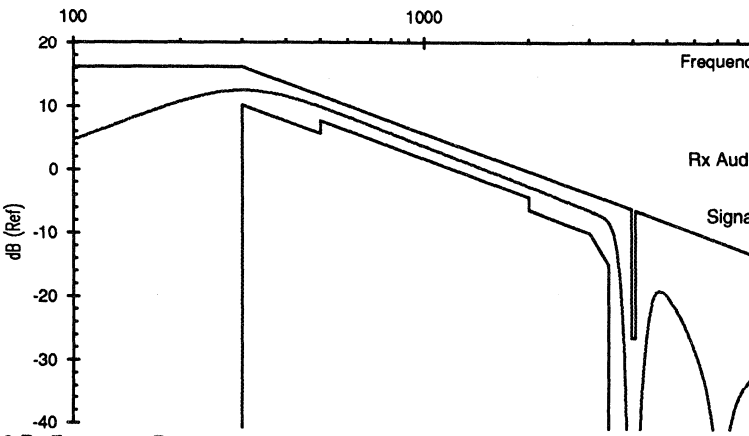


Fig.8 Rx Frequency Response

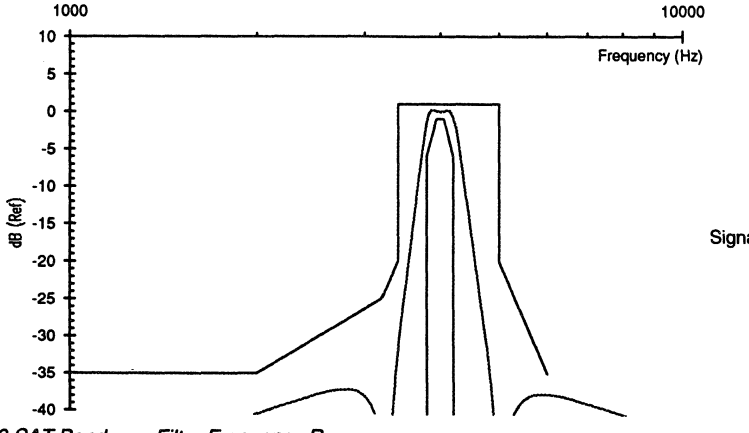


Fig.9 SAT Bandpass Filter Frequency Response

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref. V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX816DW**	-40°C to +85°C (plastic)
	FX816J	-40°C to +85°C (cerdip)
Storage temperature range:	**FX816DW**	-40°C to +85°C (plastic)
	FX816J	-55°C to +125°C (cerdip)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.032MHz. Audio level 0dB ref. = 164mV rms @ 1.0kHz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
All Operating		–	6.0	–	mA
Rx Data Mode	1	–	1.0	–	mA
Powersave All		–	0.6	–	mA
Alias Frequency		–	63.0	–	kHz
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}		–	10.0	–	kΩ
Inverter d.c. Voltage Gain		–	10.0	–	V/V
Gain/Bandwidth Product		–	10.0	–	MHz
Analogue Input Impedances					
Mic.1 & 2		–	500	–	kΩ
FFSK/Play		–	500	–	kΩ
Comp In		–	500	–	kΩ
DTMF In		–	500	–	kΩ
Dev. Limiter In		–	100	–	kΩ
(Expanded) Audio In		–	47.0	–	kΩ
Tx Mix In		–	100	–	kΩ
Rx Audio In		–	100	–	kΩ
Analogue Output Impedances					
Pre-Emp Out		–	1.4	–	kΩ
Tx Mod Out		–	600	–	Ω
Expand/Store		–	600	–	Ω
LS and Ear Audio		–	1.0	–	kΩ
FFSK Data Out		–	600	–	Ω
SAT Out		–	10.0	–	kΩ
Tx Filter Out		–	600	–	Ω
VOGAD		–	500	–	Ω
Switches – ON		–	1.0	–	kΩ
– OFF		10.0	–	–	MΩ
Control Interface Parameters					
Input Logic Levels					
Logic "1"	2	3.5	–	–	V
Logic "0"	2	–	–	1.5	V
I_{IN} (logic "1" or "0")	2	-1.0	–	1.0	µA
Input Capacitance	2	–	–	7.5	pF
Channel Performances					
Tx Path					
Analogue Signal Input Levels					
Mic. 1 and 2	3	–	-11.0	–	dB
FFSK/Play	3	–	-11.0	–	dB
DTMF	3	–	-11.0	–	dB
Comp. In	3	–	-11.0	–	dB
Tx Mix In	3	–	0	–	dB

Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
Analogue Signal Output Levels					
Pre-Emp Out	3	–	0	–	dB
Tx Filter Out	3	–	0	–	dB
Tx Mod Out	3	–	0	–	dB
Sidetone Out	3	–	-11.0	–	dB
Path Gains/Levels					
Tx Gain – 11_H					
Nominal Adjustment Range		-2.65	–	3.65	dB
Error of any Setting		-0.2	–	0.2	dB
VOGAD					
Gain (Non-Compressing)		–	11.0	–	dB
(Full Compressing)		–	-34.0	–	dB
Attack Time	4	–	3.0	–	ms
Dev Limiter					
Threshold		–	713	–	mVp-p
Symmetry		–	7.0	–	%
Mod Level Attenuation – 11_H					
Nominal Adjustment Range		-5.6		0	dB
Step Size		0.2	0.4	0.6	dB
Error of any Setting		-1.0	–	1.0	dB
Overall					
Tx Distortion		–	-40.0	-32.0	dBp
Tx Hum and Noise		–	-40.0	-20.0	dB
Rx Signal Path					
Rx Audio Input Level	3	–	-7.0	–	dB
LS/Ear Audio Output Level	3	–	0	–	dB
Path Gains/Levels					
Rx Gain – 12_H					
Nominal Adjustment Range		3.75		9.70	dB
Error of any Setting		-0.2	–	0.2	dB
FFSK Output					
Frequency Range		900	–	2100	Hz
Gain at 1kHz		-1.0	0	1.0	dB
Response		–	6.0	–	db/oct
Volume – 12_H					
Nominal Adjustment Range		-28.0		0	dB
Step Size		1.5	2.0	2.5	dB
Error of any Setting		-1.0	–	1.0	dB
Overall					
Rx Distortion		–	-40.0	-32.0	dBp
Rx Hum and Noise		–	-40.0	-34.0	dB
SAT Signal Path					
Bandpass Filter					
Frequency Range		3945		4055	Hz
Gain		-0.5	–	1.5	dB
SAT Level – 13_H					
Nominal Adjustment Range		-1.95		3.50	dB
Error of any Setting		-0.2	–	0.2	dB

Notes

1. With reference to the Powersave Command and Figure 3, all functions with the exception of the Rx Gain Element may be powersaved. This will still allow signalling data through the FX816 to activate the system via the µProcessor.
2. Serial Clock, Command Data and Chip Select inputs.
3. Levels equivalent to ±3.0kHz deviation with the settings below:

   Tx Gain = 0dB *Mod Level = 0dB*
   Rx Gain = 7.05dB *Volume = 0dB*
   SAT Level = 0dB

   Other levels can be achieved by adjusting the above variable gain blocks in accordance with Tables 1 to 5.
4. Using the components shown in Figure 2.

Package Outlines

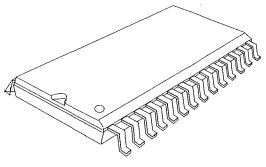
The FX816 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX816 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX816DW 28-pin plastic S.O.I.C. (D1)

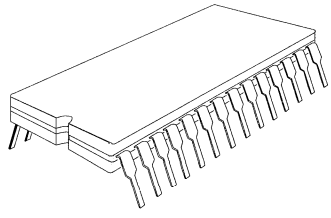
NOT TO SCALE



Max. Body Length 18.05mm
Max. Body Width 7.65mm

FX816J 28-pin cerdip DIL (J5)

NOT TO SCALE



Max. Body Length 37.05mm
Max. Body Width 13.36mm

Ordering Information

FX816DW 28-pin plastic S.O.I.C. (D1)

FX816J 28-pin cerdip DIL (J5)

CML Semiconductor Products

PRODUCT INFORMATION

FX826 AMPS/TACS System Audio Processor

Publication D/826/3 July 1994
Provisional Issue

Features

- **Full-Duplex Audio Processing for AMPS & TACS Cellular Systems**
- **On-Chip Speech and SAT Facilities**
  – Tx/Rx Filtering & Gain – SAT Channel Pre-/De-Emphasis – Deviation Limiter –
- **Serial µProcessor Interface**
- **Separate SAT Channel**
- **"Sidetone" Output Available**
- **HandsFree Compatibility**
- **Access to External Processes**
  – Compression – Expansion – Signalling – VSR Codec (Store/Play) –
- **Powersave (Low-Current) Settings**

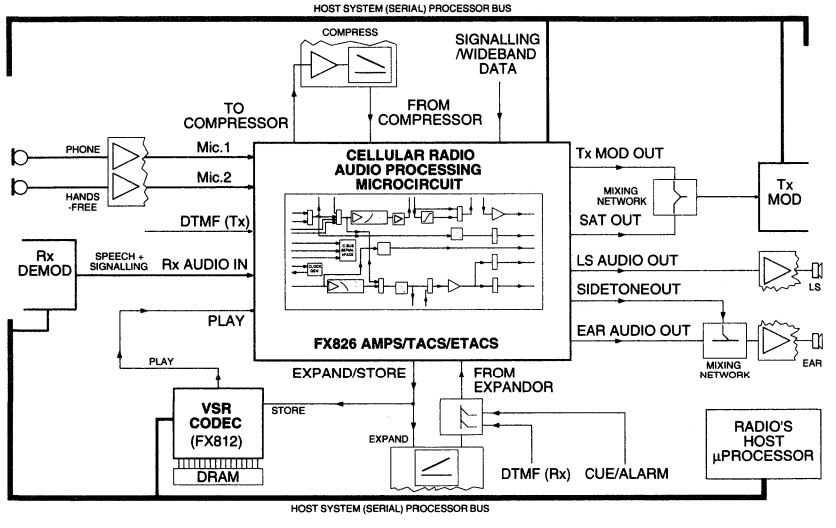


Fig.1 The FX826 AMPS/TACS Audio Processor Installed within a Cellular System

FX826

Brief Description

The FX826 is a µProcessor controlled full-duplex audio processor on a single-chip with separate Tx and Rx paths to provide all the filter/gain/limiting functions necessary to pre-process audio, wideband-data and signalling in cellular communications systems using the AMPS or TACS/ETACS/JTACS specifications.

Selectable inputs available to the transmit path are: a choice of two microphones and DTMF/signalling, with access, in this path, to external compression circuitry. Operationally the Tx path provides input gain/filtering, a deviation limiter and Tx Modulation Drive controls.

In the Rx path the SAT signal is separated from the incoming audio via a filter block and made available at a separate pin for mixing externally with the Tx Modulation Drive.

The Rx path consists of an input gain/filter block for voice, inputs from an external audio expansion system and an output gain control driving either a loudspeaker system or earpiece.

Unique to the FX816/826/836 cellular audio processors is the ability to route audio (Tx or Rx) to an external Voice Store and Retrieve (VSR) device such as the FX802 or FX812 thus providing the radio system with a voice answering and announcement facility using external DRAM.

The FX826, a low-power CMOS device, which reduces the amount of microcircuits and components required in a cellular audio system by providing more functions on a single chip, is available in 28-pin plastic small outline (S.O.I.C.) surface mount and cerdip DIL packages.

Pin Number Function

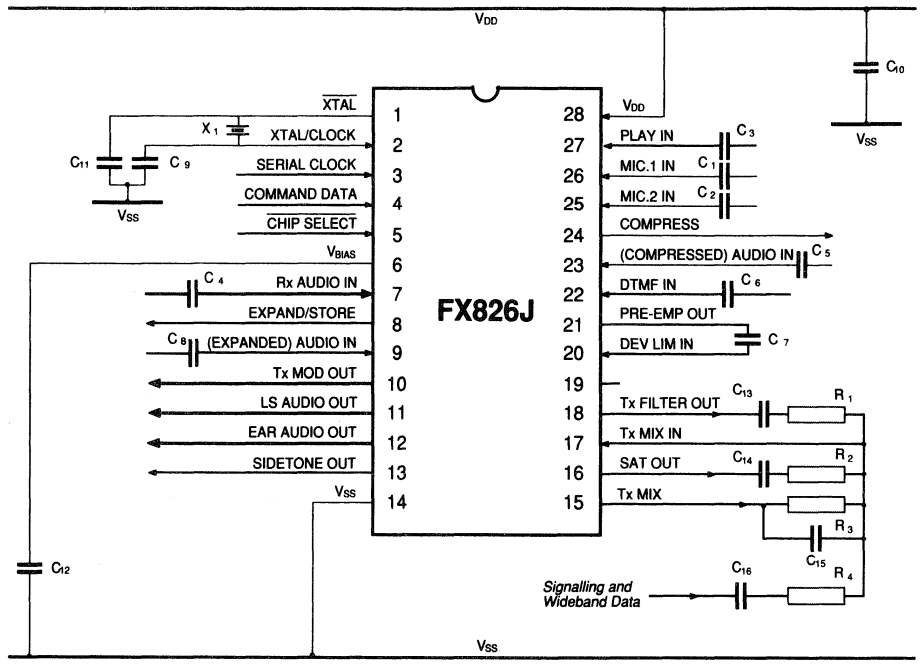
FX826DW	FX826J	Function
1	1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	2	**Xtal/Clock:** The input to the on-chip clock oscillator. A Xtal or externally derived clock (f_{XTAL}) should be connected here. Note that operation of the FX826 without a suitable Xtal or clock input may cause device damage. See Figure 2 (notes).
3	3	**Serial Clock:** The "C-BUS" serial data clock input. This clock, produced by the µController, is used for transfer timing of commands and data to the FX826. See Timing Diagrams.
4	4	**Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to the FX826 in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams.
5	5	**Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by this signal. See Timing Diagrams.
6	6	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS}. See Figure 2.
7	7	**Rx Audio In:** Normally taken from the radio's discriminator output, this input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor.
8	8	**Expand/Store:** A common output that can be used as either an input to an external audio expander or the input to a voice storage medium such as the FX812. Components relevant to the external device requirements should be used at this output. See Figures 2 and 3.
9	9	**(Expanded) Audio In:** The audio input, via SW5, from an external expander or audio mixing function. This input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor. See Figures 2 and 3.
10	10	**Tx Mod Out:** The composite Tx audio output to the transmitter modulator from a variable attenuation stage (11_H). This output is set to V_{BIAS} via an internal 1MΩ resistor when set to Powersave or OFF.
11	11	**LS Audio Out:** An audio output of the Rx path (or selected audios, see Figure 3) for a loudspeaker system. This is available for handsfree operation. This output can be connected to V_{BIAS} when not required, by SW6 (Configuration Command (10_H)). A driver amplifier may be required.
12	12	**Ear Audio Out:** An audio output of the Rx path (or selected audios), available as an output for a handset earpiece. This output, in parallel with the LS Audio Out function, can be connected to V_{BIAS} when not required, by SW7 (Configuration Command (10_H)). A driver amplifier may be required.
13	13	**Sidetone:** A switched "sidetone" from the microphone inputs made available for mixing externally with the "Ear" audio. See Figure 3.
14	14	**V_{SS}:** Negative supply rail. Signal ground.
		Notes on Inputs: *To minimize aliasing effects, lowpass filtering may be required at the inputs to this device (especially those supplied from switched-capacitor-type devices) to ensure the input spectrum is kept below 63kHz.*

Pin Number Function

FX826DW	FX826J	
15	15	**Tx Mix:** The output of the Tx Mix Amplifier. Used with external components, it allows the Tx Filter Out output to mix with externally generated signalling tones prior to the final level adjustment.
16	16	**SAT Out:** The output of the SAT Bandpass filter. This level is recovered from the input Rx audio and is available for mixing externally with the transmitter modulation. See Figure 3.
17	17	**Tx Mix In:** The input to the Tx Mix Amplifier. Used with external components, it allows the Tx Filter Out output to mix with externally generated signalling tones prior to the final level adjustment. The recovered SAT signal may be introduced at this point. See Figures 2 and 3.
18	18	**Tx Filter Out:** The output of the Deviation Limiter/Lowpass Filter stage. This stage can be by-passed using SW3 (Configuration Command). See Figure 3.
19	19	No internal connection – Leave open circuit.
20	20	**Deviation Limiter In:** Input to the on-chip deviation limiter. This input should be a.c. coupled to the Pre-Emphasis Out pin. The a.c. coupling will achieve maximum possible symmetry of limiting as this input has a 1MΩ internal resistor to V_{BIAS}. See Figure 2.
21	21	**Pre-Emphasis Out:** Audio output from the Tx Gain/Pre-Emphasis function. This output should be a.c. coupled to the Deviation Limiter In pin. See Figures 2 & 3.
22	22	**DTMF In:** To introduce DTMF type audio, at a suitable level for transmission, to the Tx Path, controlled by SW2 (Configuration Command (10_H)). This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
23	23	**Comp**ression **In:** The audio input from an external compression system. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
24	24	**Comp**ression: The output to an external audio compression system. Currently available compressor/ expanders have Op-Amps incorporated. The compressor can be by-passed by SW2.
25	25	**Mic.2 In:** Tx voice (Mic.) inputs, selectable by SW1 available for handsfree mic./handset mic. or any Tx audio input. Pre-amplification may be required at these inputs. These inputs each have an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
26	26	**Mic.1 In:**
27	27	**Play In:** The input via SW2 from a voice storage device such as the FX812. This "replayed" audio can be sent to Rx or Tx paths allowing a Messaging/Voice Notepad/Answering facility. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
28	28	V_{DD}: Positive supply rail. A single +5-volt power supply is required. Levels and voltages within this Audio Processor are dependent upon this supply.

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and the relevant Cellular microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController. For further details refer to CML Publication No. D/µINT/1 June 1991.

Application Information



R_1	=	100kΩ	C_3	=	100nF	C_8	=	100nF	C_{13}	=	100nF
R_2		as required	C_4		100nF	C_9		33pF	C_{14}		100nF
R_3		100kΩ	C_5		100nF	C_{10}		100nF	C_{15}		100pF
R_4		as required	C_6		100nF	C_{11}		33pF	C_{16}		100nF
C_1		100nF	C_7		100nF	C_{12}		1.0µF	X_1		4.000MHz
C_2		100nF									

Tolerances – Capacitors ±20%

Fig.2 Recommended External Components

Notes

1. **Xtal/clock operation**
   Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail (V_{DD}) is fitted with a current limiting device (resistor or fast-reaction fuse).

2. **SAT Output**
   It is possible, due to the impedance of this output, that an external buffer amplifier is required when interfacing or mixing with other cellular system sections.

3. **Tx Mix Gain**
   The value of R_4 should be chosen with R_3/C_{15} so as to provide the required gain.

AMPS/TACS Cellular System Interfaces

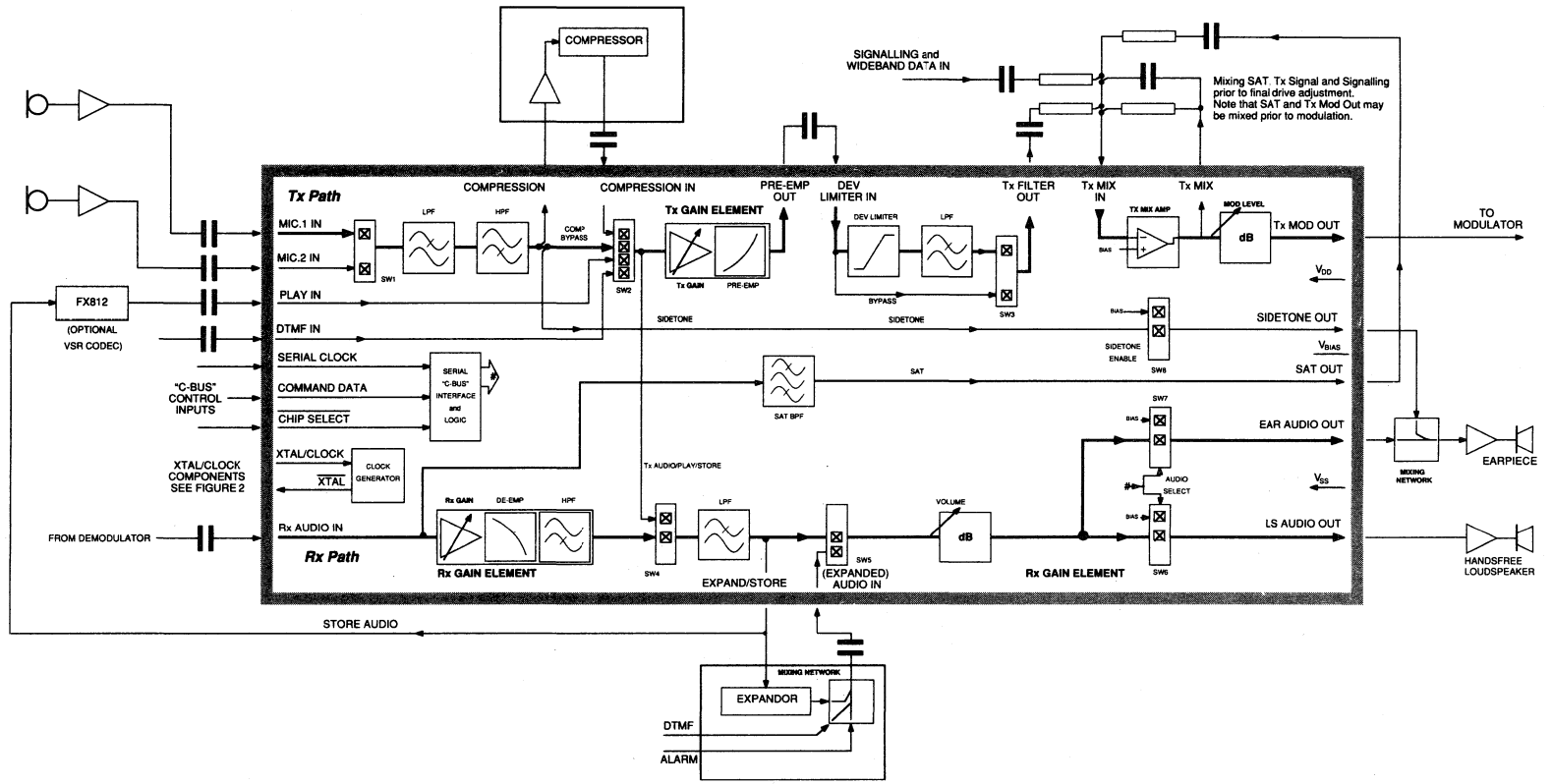


Fig.3 The FX826 Internal and External Signal Paths within a TACS Cellular Radio System

The Controlling System

"C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's New Generation microcircuits.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the FX826 AMPS and TACS Audio Processor is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the device. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex	Binary MSB LSB		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Configuration Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
Tx Gain & Mod. Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
Rx Gain & Vol. Command	12	0 0 0 1 0 0 1 0	+	1 byte	4
Powersave Command	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 "C-Bus" Address/Commands

In "C-BUS" protocol the audio processor is allocated Address/Command (A/C) values 10_H to 13_H. Configuration, Tx/Rx Gains and Powersave assignments and data requirements are given in Table 1.
Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the "C-BUS" interface recognises the first byte after Chip Select (logic "0") as an Address/Command. Function or Level control data, which is detailed in Tables 2, 3, 4 and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams Figures 5 and 6.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). A **General Reset Command (01_H)** will be required to set all FX826 registers to 00_H.

Configuration Command *(Preceded by A/C 10_H)*

Setting		Control Bits
MSB		***Transmitted First***
Bit 7		**Sw8 Sidetone**
0		Sidetone Bias
1		Sidetone Enabled
6		**Sw6/7 Rx Audio**
0		Ear Enabled, LS Bias
1		LS Enabled, Ear Bias
5		**Sw5 Expandor**
0		Expandor By-Pass
1		Expandor Route
4		**Sw4 Tx/Rx Audio**
0		Tx Store/Audio
1		Rx Store/Audio
3		**Sw3 Dev. Limiter**
0		Dev. Limiter By-Pass
1		Dev. Limiter Route
2		**Sw1 Mic. Inputs**
0		Mic. 1 Input
1		Mic.2 Input
1	***0***	**Sw2 Tx Function**
0	0	DTMF In
0	1	Compressor By-Pass
1	0	Compressor In
1	1	Play In

Table 2 Configuration Commands

Tx Gain & Mod. Command *(Preceded by A/C 11_H)*

Setting				Gain (dBs)
MSB				***Transmitted First***
7	***6***	***5***	***4***	**Tx Mod. Level**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-5.6
0	0	1	0	-5.2
0	0	1	1	-4.8
0	1	0	0	-4.4
0	1	0	1	-4.0
0	1	1	0	-3.6
0	1	1	1	-3.2
1	0	0	0	-2.8
1	0	0	1	-2.4
1	0	1	0	-2.0
1	0	1	1	-1.6
1	1	0	0	-1.2
1	1	0	1	-0.8
1	1	1	0	-0.4
1	1	1	1	0
3	***2***	***1***	***0***	**Tx Input Gain**
0	0	0	0	-2.65
0	0	0	1	-2.05
0	0	1	0	-1.50
0	0	1	1	-0.95
0	1	0	0	-0.45
0	1	0	1	0
0	1	1	0	0.45
0	1	1	1	0.85
1	0	0	0	1.25
1	0	0	1	1.65
1	0	1	0	2.05
1	0	1	1	2.40
1	1	0	0	2.70
1	1	0	1	3.05
1	1	1	0	3.35
1	1	1	1	3.65

Table 3 Tx Gain & Mod. Commands

The Controlling System .....

Rx Gain & Vol. Command *(Preceded by A/C 12_H)*

Setting				Gain (dBs)
MSB				**Transmitted First**
7	**6**	**5**	**4**	**Rx Volume**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-28.0
0	0	1	0	-26.0
0	0	1	1	-24.0
0	1	0	0	-22.0
0	1	0	1	-20.0
0	1	1	0	-18.0
0	1	1	1	-16.0
1	0	0	0	-14.0
1	0	0	1	-12.0
1	0	1	0	-10.0
1	0	1	1	-8.0
1	1	0	0	-6.0
1	1	0	1	-4.0
1	1	1	0	-2.0
1	1	1	1	0
3	**2**	**1**	**0**	**Rx Input Gain**
0	0	0	0	3.75
0	0	0	1	4.30
0	0	1	0	4.80
0	0	1	1	5.30
0	1	0	0	5.80
0	1	0	1	6.20
0	1	1	0	6.55
0	1	1	1	7.05
1	0	0	0	7.40
1	0	0	1	7.80
1	0	1	0	8.15
1	0	1	1	8.50
1	1	0	0	8.80
1	1	0	1	9.10
1	1	1	0	9.40
1	1	1	1	9.70

Table 4 Rx Gain and Vol. Commands

Powersave Command *(Preceded by A/C 13_H)*

Setting							Control Bits
MSB							
Bit 7							**Transmitted First**
7	*6*	*5*	*4*	*3*	*2*	*1*	
0	0	0	0	0	0	0	All must be a logic "0"
			0				**Powersave Setting**
			0				Powersave FX826
			1				Enable FX826

Table 5 Powersave Command

Reference Signal Levels

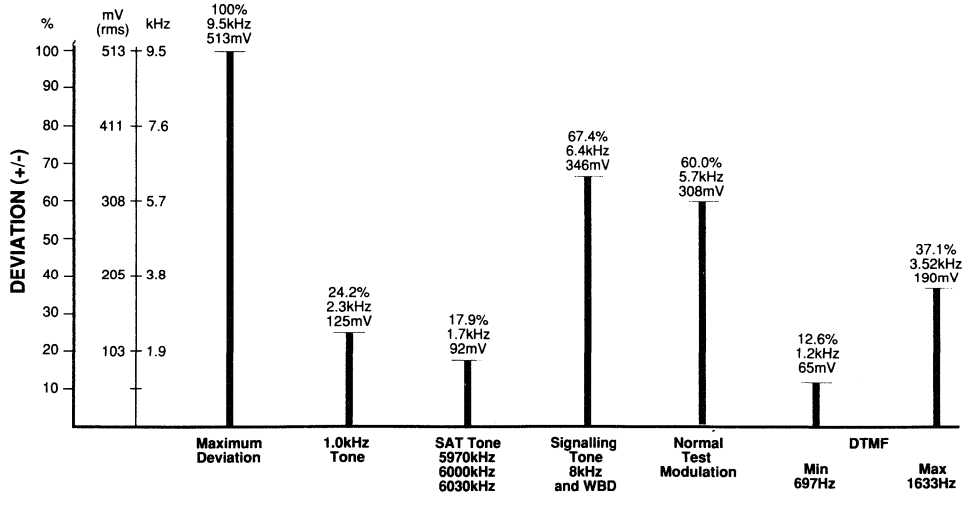


*Fig.4 TACS Signal Deviation Levels and corresponding **Tx Mod Outputs** with the Mod Level set to 0dB*

Control Timing Information

Timing Specification – Figures 5 and 6.

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"	1	2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"	1	4.0	–	–	µs
t_{CSOFF}	"CS-High" Time between transactions	1, 2	2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time	1	2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time	1	4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns

Notes

1. These Minimum Timing values are altered during operation of the FX812 VSR Codec.
2. Chip Select must be taken to a logic "1" between each individual transaction.

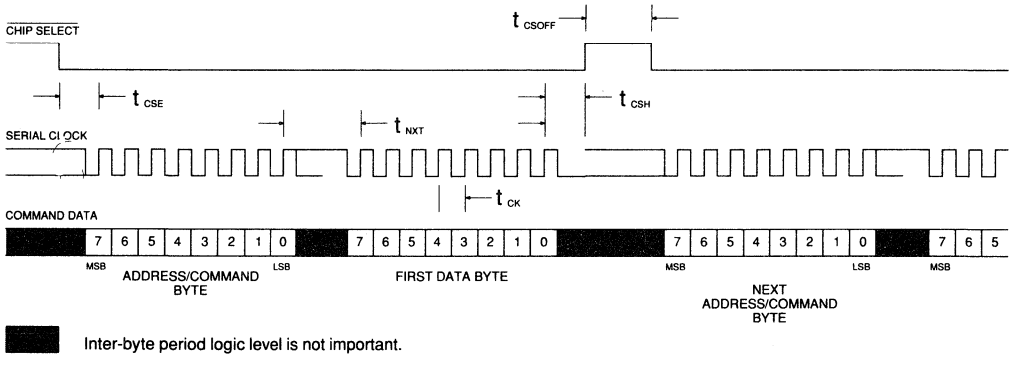


Fig.5 Control Timing Information

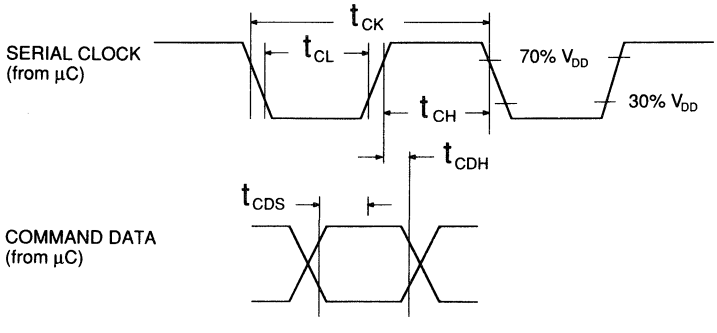


Fig.6 Control Timing Relationships

Frequency Responses

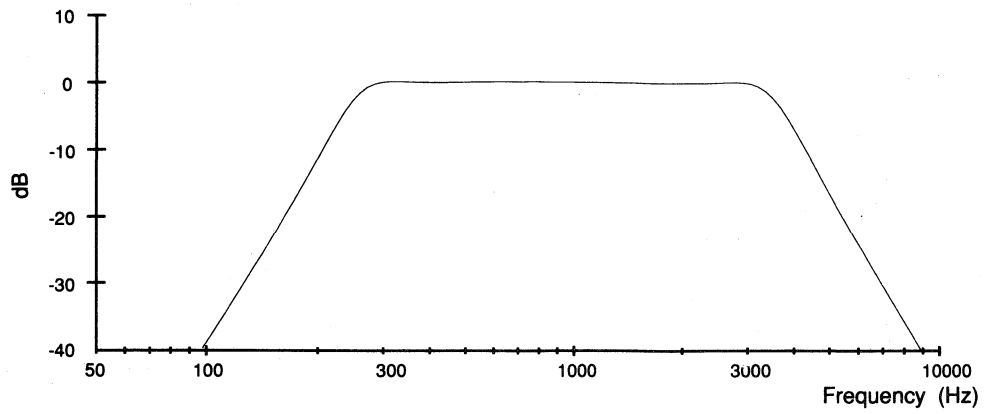


Fig.7 Microphone Input Stages -Combined Low and Highpass Filter Frequency Response

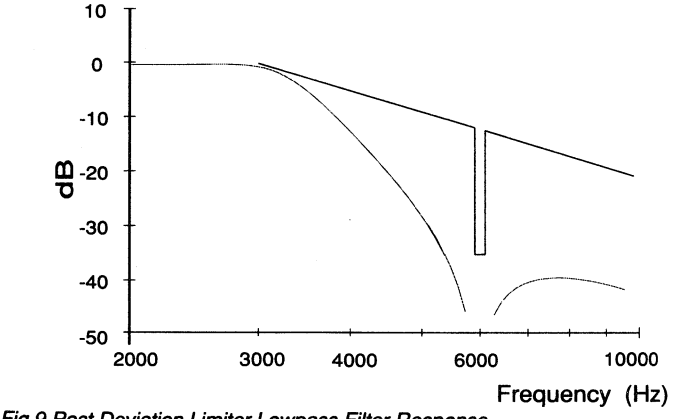


Fig.9 Post Deviation Limiter Lowpass Filter Response

Figure 7
Mic.1/2 In to Compression Out

V_{DD} = 5.0V

Signal Input Level = 55.0mVrms

Figure 8
Dev Limiter In to Tx Filter Out

V_{DD} = 5.0V

Signal Input Level = 55.0mVrms

Figure 9

Rx Audio In to SAT out

V_{DD} = 5.0V

Signal Input Level = 100mVrms

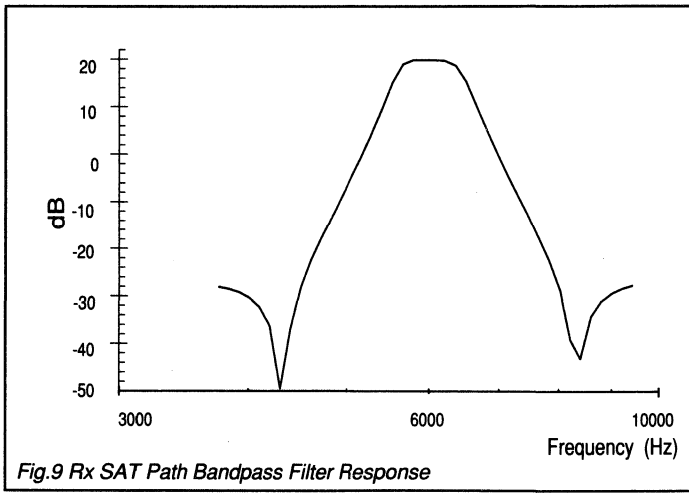


Fig.9 Rx SAT Path Bandpass Filter Response

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref. V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX826DW**	-40°C to +85°C (plastic)
	FX826J	-40°C to +85°C (cerdip)
Storage temperature range:	**FX826DW**	-40°C to +85°C (plastic)
	FX826J	-55°C to +125°C (cerdip)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.000MHz. Audio level 0dB ref. = 308mV rms @ 1.0kHz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Operating		–	6.5	–	mA
Powersave		–	0.5	–	mA
Alias Frequency		–	63.0	–	kHz
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}		–	10.0	–	kΩ
Inverter d.c. Voltage Gain		–	10.0	–	V/V
Gain/Bandwidth Product		–	10.0	–	MHz
Tx Mix Amp (Open Loop Gain)		–	50.0	–	dB
(Bandwidth)		20.0	–	–	kHz
Analogue Input Impedances					
Mic.1 & 2		–	500	–	kΩ
Play		–	500	–	kΩ
Comp In		–	500	–	kΩ
DTMF In		–	500	–	kΩ
Dev. Limiter In		–	100	–	kΩ
(Expanded) Audio In		–	47.0	–	kΩ
Tx Mix In		10.0	–	–	MΩ
Rx Audio In		–	100	–	kΩ
Analogue Output Impedances					
Pre-Emp Out		–	600	–	Ω
Tx Mod Out		–	600	–	Ω
Expand/Store		–	600	–	Ω
LS and Ear Audio		–	1.0	–	kΩ
SAT Out	3	–	1.0	–	kΩ
Tx Filter Out		–	600	–	Ω
Comp Out		–	600	–	Ω
Sidetone Out		–	2.0	–	kΩ
Tx Mix (Open Loop)		–	6.0	–	kΩ
(Closed Loop)		–	600	–	Ω
Switches – ON		–	1.0	–	kΩ
– OFF		10.0	–	–	MΩ
Control Interface Parameters					
Input Logic Levels					
Logic "1"	1	3.5	–	–	V
Logic "0"	1	–	–	1.5	V
I_{IN} (logic "1" or "0")	1	-1.0	–	1.0	µA
Input Capacitance	1	–	–	7.5	pF
Channel Performances					
Tx Path					
Filter Specifications					
Pre-Compression L/HPF Combination					
Passband		300		3000	Hz
Slope - below 300Hz		+24.0	–	–	dB/oct.
above 3000Hz		-24.0	–	–	dB/oct.
Tx Gain Pre-Emphasis					
Gain at 1.0kHz		–	0	–	dB
Slope (300Hz - 3000Hz)		–	6.0	–	dB/oct.

Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
Post Deviation Limiter LPF					
Attenuation Relative to 1.0kHz	3.0kHz - 5.9kHz		40 log(f/3000)		dB
	5.9kHz - 6.1kHz		35.0		dB
	6.1kHz - 15kHz		40 log(f/3000)		dB
	>15kHz		28.0		dB
Analogue Signal Input Levels					
Mic. 1 and 2	2	–	0	–	dB
Play	2	–	0	–	dB
DTMF	2	–	0	–	dB
Comp. In	2	–	0	–	dB
Tx Mix In	2	–	0	–	dB
Analogue Signal Output Levels					
Pre-Emp Out	2	–	0	–	dB
Tx Filter Out	2	–	0	–	dB
Tx Mod Out	2	–	0	–	dB
Sidetone Out	2	–	0	–	dB
Path Gains/Levels					
Tx Gain – 11_H					
Nominal Adjustment Range		-2.65	–	3.65	dB
Error of any Setting		-0.2	–	0.2	dB
Dev Limiter					
Threshold		–	1086	–	mVp-p
Symmetry		–	7.0	–	%
Mod Level Attenuation – 11_H					
Nominal Adjustment Range		-5.6		0	dB
Step Size		0.2	0.4	0.6	dB
Error of any Setting		-1.0	–	1.0	dB
Overall					
Tx Distortion		–	-40.0	-32.0	dBp
Tx Hum and Noise		–	-40.0	-20.0	dB
Rx Signal Path					
Filter Specifications					
Rx Gain De-Emphasis					
Gain at 1.0kHz		–	3.75	–	dB
Slope (300Hz - 3000Hz)		–	-6.0	–	dB/oct.
Rx Channel Bandpass		300		3000	Hz
Slope - below 300Hz		+24.0	–	–	dB/oct.
above 3000Hz		-36.0	–	–	dB/oct.
Analogue Signal Levels					
Rx Audio Input Level	2	–	-7.0	–	dB
LS/Ear Audio Output Level	2	–	0	–	dB
Path Gains/Levels					
Rx Gain – 12_H					
Nominal Adjustment Range		3.75		9.70	dB
Error of any Setting		-0.2	–	0.2	dB
Volume – 12_H					
Nominal Adjustment Range		-28.0		0	dB
Step Size		1.5	2.0	2.5	dB
Error of any Setting		-1.0	–	1.0	dB
Overall					
Rx Distortion		–	-40.0	-32.0	dBp
Rx Hum and Noise		–	-40.0	-34.0	dB
SAT Signal Path					
Bandpass Filter					
Frequency Range		5970		6030	Hz
Gain		19.0	20.0	21.0	dB

Notes

1. Serial Clock, Command Data and Chip Select inputs.
2. Levels equivalent to ±3.0kHz deviation with the settings below:

   Tx Gain = 0dB *Mod Level = 0dB*

   Rx Gain = 7.05dB *Volume = 0dB*

   Other levels can be achieved by adjusting the above variable gain blocks in accordance with Tables 1 to 5.
3. Recommended load >10.0kΩ.

Package Outlines

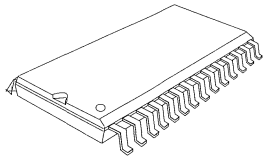
The FX826 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX826 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX826DW 28-pin plastic S.O.I.C. (D1)

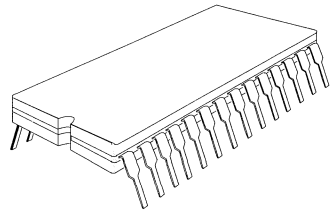
NOT TO SCALE



Max. Body Length 18.05mm
Max. Body Width 7.65mm

FX826J 28-pin cerdip DIL (J5)

NOT TO SCALE



Max. Body Length 37.05mm
Max. Body Width 13.36mm

Ordering Information

FX826DW 28-pin plastic S.O.I.C. (D1)

FX826J 28-pin cerdip DIL (J5)

CML Semiconductor Products

PRODUCT INFORMATION

FX836 Radiocom 2000 System Audio Processor

Publication D/836/3 July 1994
Provisional Issue

Features/Applications

- **Full-Duplex Audio Processing for R2000 Cellular System**
- **On-Chip Speech and Data Facilities**
  - **Tx/Rx/Data Filtering & Gain**
  - **Pre-/De-Emphasis – Deviation Limiter**
- **Serial µProcessor Interface**
- **Tx and Rx LF-Data Paths**
- **FFSK and (50 Baud) LF-Data Facilities**
- **Hands-Free Compatibility**
- **Access to External Processes**
  - ***Compression – Expansion***
  - ***Signalling/Data Mixing***
  - ***VSR Codec (Store/Play)***
- **Powersave (Low-Current) Settings**

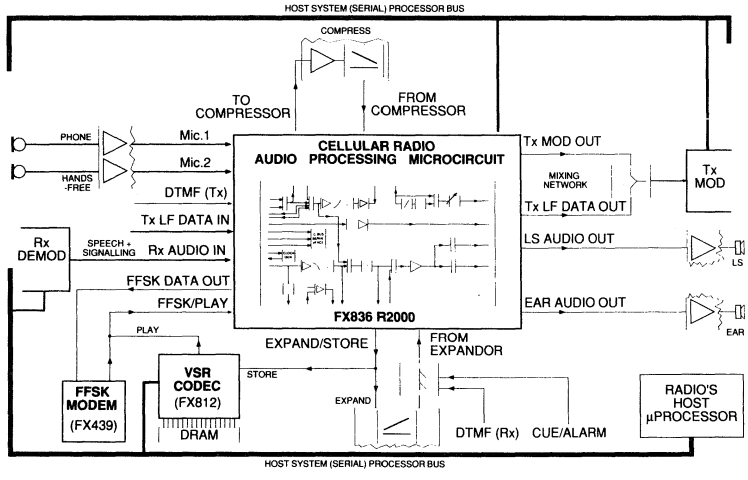


Fig.1 The FX836 R2000 Audio Processor within a Cellular System

Brief Description

The FX836 is a µProcessor controlled full-duplex audio processor on a single-chip with separate Tx, Rx and LF (50 baud) data paths to provide all the filter/gain/limiting functions necessary to pre-process audio, data and signalling in the Radiocom 2000 (R2000) Cellular communications system.

Selectable inputs available for transmission are: a choice of two microphones, DTMF/signalling or FFSK/data, with access, in this path, to external voice compression circuitry. Operationally the Tx path provides input gain/filtering, pre-emphasis, a deviation limiter and Tx Modulation Drive controls. Available to the transmit function is a separate path to process LF system control data for amalgamation externally with Tx voiceband audio.

The Rx path consists of an input gain/de-emphasis/filter block for voice and data, inputs from an external audio expansion system and output gain controls driving loudspeaker and earpiece circuitry.

In the Rx path LF data signals are separated from the incoming audio via an LF filter and made available at a separate pin for use by the system µProcessor

Unique to the FX816/826/836 cellular audio processors is the ability to route audio (Tx or Rx) to an external Voice Store and Retrieve (VSR) device such as the FX802 or FX812 thus providing the radio system with a voice answering and announcement facility using external DRAM.

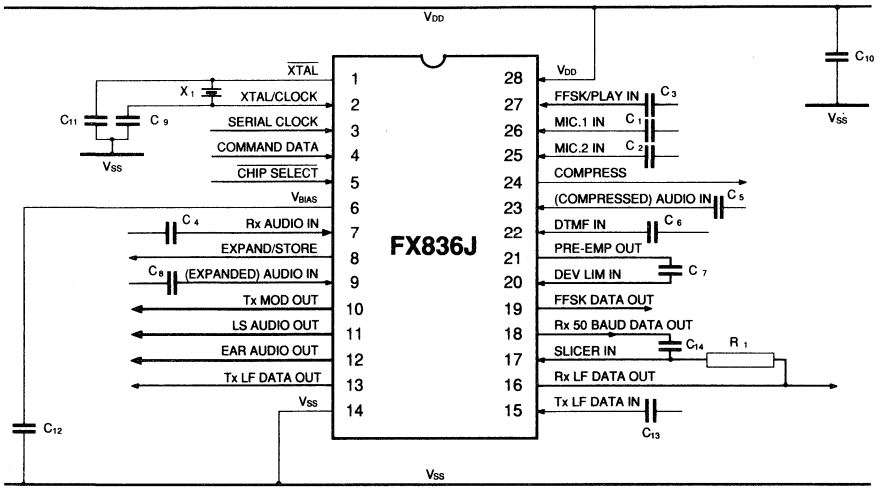
The FX836, a low-power CMOS device, which reduces the amount of microcircuits and components required in a cellular audio system by providing more functions on a single chip, is available in 28-pin plastic small outline (S.O.I.C.) surface mount and cerdip DIL packages.

FX836

Pin Number FX836DW FX836J	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	**Xtal/Clock:** The input to the on-chip clock oscillator. A Xtal or externally derived clock (f_{XTAL}) should be connected here. Note that operation of the FX836 without a suitable Xtal or clock input may cause device damage. See Figure 2 (notes).
3	**Serial Clock:** The "C-BUS" serial data clock input. This clock, produced by the µController, is used for transfer timing of commands and data to the FX836. See Timing Diagrams.
4	**Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to the FX836 in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams.
5	**Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing Diagrams.
6	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS}. See Figure 2.
7	**Rx Audio In:** Normally taken from the radio's discriminator output. This input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor.
8	**Expand/Store:** A common output that can be used as either an input to an external audio expandor or the input to a voice storage medium such as the FX812. Components relevant to the external device requirements should be used at this output. See Figures 2 and 4.
9	**(Expanded) Audio In:** The audio input, via SW5, from an external expandor or audio mixing function. This input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor. See Figures 2 and 4.
10	**Tx Mod Out:** The composite Tx audio output to the transmitter modulator from a variable attenuation stage (11_H). This output is set to V_{BIAS} via an internal 1MΩ resistor when set to Powersave or OFF.
11	**LS Audio Out:** An audio output of the Rx Path (or audio selected by SW2 and SW4 Figure 4) for a loudspeaker system. Available for handsfree operation this output is controlled by the Rx Gain and LS Volume Command (12_H) and is internally connected to V_{BIAS} when not required. A driver amplifier may be required at this output.
12	**Ear Audio Out:** An audio output of the Rx Path (or audio selected by SW2 and SW4–Figure 4), available as an output for a handset earpiece. Separate from the LS Audio Out function, this output is controlled by the LF Data Gain and Ear Volume Command (13_H) and is internally connected to V_{BIAS} when not required. A driver amplifier may be required at this output.
13	**Tx LF Data Out:** The output, if required, to the Tx Modulator, of LF (50 baud) filtered and level-adjusted digital data.
14	**V_{SS}:** Negative supply rail. Signal ground.
	Notes on Inputs: *To minimize aliasing effects, lowpass filtering may be required at the inputs to this device (especially those supplied from switched-capacitor-type devices) to ensure the input spectrum is kept below 63kHz.*

Pin Number FX836DW FX836J	Function
15	**Tx LF Data In:** The input of LF (50 baud) digital data for transmission, from an external modem. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
16	**Rx LF Data Out:** The output, to a 50 baud modem, of the received, filtered, LF data. This pin is used with the 50 Baud Data, Slicer In pins and external components to filter and limit the received LF data. See Figure 4.
17	**Slicer In:** The input to the data slicer. Employed as shown in Figure 4 to filter and limit the received LF data.
18	**Rx 50 Baud Data Out:** The output of the received 50 baud data. See Figures 2 and 4.
19	**FFSK Out:** The de-emphasized Rx audio output available for access to the received FFSK data. This output could be directed to an FFSK Modem such as the FX439.
20	**Deviation Limiter In:** Input to the on-chip deviation Limiter. This input should be a.c. coupled to the Pre-Emphasis Out pin. The a.c. coupling is required to achieve the best possible symmetry of limiting as this input has a 1MΩ internal resistor to V_{BIAS}. See Figure 2.
21	**Pre-Emphasis Out:** Audio output from the Tx Input Gain/Pre-Emphasis function. This output should be a.c. coupled to the Deviation Limiter In pin. See Figures 2 and 4.
22	**DTMF In:** To introduce DTMF type audio, at a suitable level for transmission, to the Tx Path, controlled by SW2 (Configuration Command (10_H)). This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
23	**Compression In:** The audio input from an external compression system. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
24	**Compression:** The output to an external audio compression system. Currently available compressor/ expandors have Op-Amps incorporated. The compressor can be by-passed by SW2.
25 26	**Mic.2 In:** **Mic.1 In:** Tx voice (Mic.) inputs, selectable by SW1 available for handsfree mic./handset mic. or any Tx audio input. Pre-amplification may be required prior to these inputs. Each input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
27	**FFSK/Play In:** The Tx FFSK data input via SW2. This can also be used to input (replay) from a voice storage device such as the FX812. This "replayed" audio can be sent to Rx or Tx paths allowing a Messaging/Voice Notepad/Answering facility. Both FX439 FFSK Modem and FX812 VSR Codec outputs can be wired together at this pin (OR'd) if the functions are activated one-at-a-time. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
28	V_{DD}: Positive supply rail. A single +5 volt power supply is required. Levels and voltages within this audio processor are dependent upon this supply. *"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and the relevant Cellular microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController.* *For further details refer to CML Publication No. D/µINT/1 June 1991 or DBS 800 System Information Document.*

Application Information



R_1	=	1.0MΩ	C_4	=	100nF	C_8	=	100nF	C_{12}	=	1.0µF
C_1		100nF	C_5		100nF	C_9		33pF	C_{13}		100nF
C_2		100nF	C_6		100nF	C_{10}		100nF	C_{14}		100nF
C_3		100nF	C_7		100nF	C_{11}		33pF	X_1		4.032MHz

Tolerances – Resistors ±10% Capacitors ±20%

Fig.2 Recommended External Components

1. **Xtal/clock operation**
   Operation of any CML microcircuit without a Xtal or clock input may cause device damage.
   To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail (V_{DD}) is fitted with a current limiting device (resistor or fast-reaction fuse).

2. **FFSK Modem**
   The FX469, a general purpose FFSK Modem could be employed with this NMT system Audio Processor. The FX469 is a non-formatted modem, which with due regard to Xtal/clock frequencies and µProcessor interface, is compatible with both Mobile/Portable and Base Station applications.

Reference Signal Levels

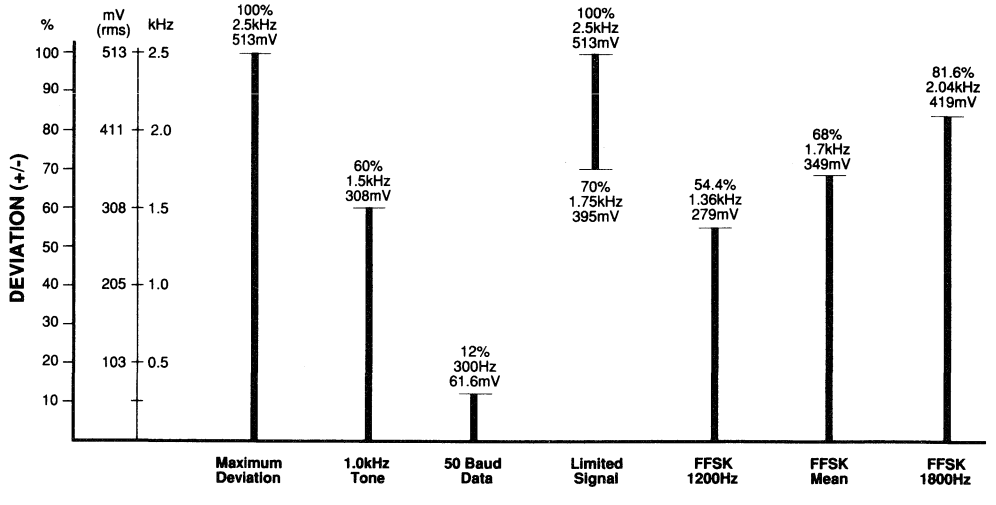


*Fig.3 R2000 Signal Deviation Levels and corresponding **Tx Mod Outputs** with the Mod Level set to 0dB*

R2000 Cellular System Interfaces

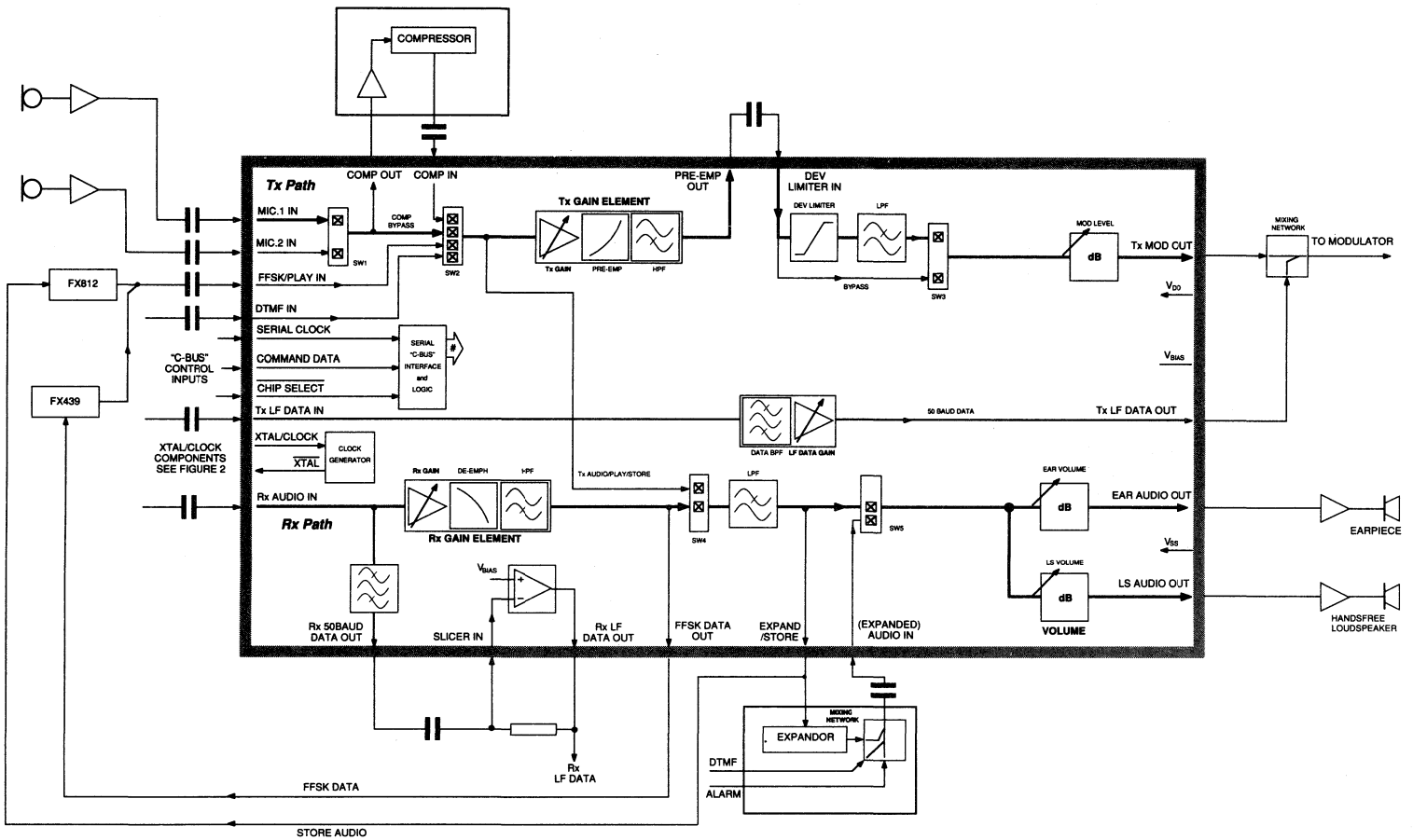


Fig.4 The FX836 within an R2000 Cellular Radio System

The Controlling System

"C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's New Generation microcircuits.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the FX836 R2000 Audio Processor is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the device. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex	Binary MSB							LSB		Command Data	Table
General Reset	01	0	0	0	0	0	0	0	1			
Configuration Command	10	0	0	0	1	0	0	0	0	+	1 byte	2
Tx Gain & Mod. Level	11	0	0	0	1	0	0	0	1	+	1 byte	3
Rx Gain & LS Vol.	12	0	0	0	1	0	0	1	0	+	1 byte	4
LF Data Gain & Ear Vol.	13	0	0	0	1	0	0	1	1	+	1 byte	5

Table 1 "C-Bus" Address/Commands

In "C-BUS" protocol the audio processor is allocated Address/Command (A/C) values 10_H to 13_H. Configuration, Tx/Rx Gains and SAT/Powersave assignments and data requirements are given in Table 1. Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the "C-BUS" interface recognises the first byte after $\overline{\text{Chip Select}}$ (logic "0") as an Address/Command. Function or Level control data, which is detailed in Tables 2,3,4 and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). Therefore a **General Reset Command (01_H)** will be required initially to set all FX836 registers to 00_H.

Configuration Command *(Preceded by A/C 10_H)*

Setting	*Control Bits*
MSB	***Transmitted First***
Bit 7	**Rx Gain Element**
0	Powersave
1	Enable
6	**All Functions** (except Rx Gain Element)
0	Powersave
1	Enable
5	**Sw5 Expandor**
0	Expandor By-Pass
1	Expandor Route
4	**Sw4 Tx/Rx Audio**
0	Tx Store/Audio
1	Rx Store/Audio
3	**Sw3 Dev. Limiter**
0	Dev. Limiter By-Pass
1	Dev. Limiter Route
2	**Sw1 Mic. Inputs**
0	Mic. 1 Input
1	Mic.2 Input
1 ***0***	**Sw2 Tx Function**
0 0	DTMF In
0 1	Compressor In
1 0	Compressor By-Pass
1 1	FFSK/Play In

Note that Bits 6 and 7 can be configured to allow the Rx to "listen for data" whilst powersaved. See Figure 4.

Table 2 Configuration Commands

Tx Gain & Mod. Level *(Preceded by A/C 11_H)*

Setting				*Gain (dBs)*
MSB				***Transmitted First***
7	***6***	***5***	***4***	**Tx Mod. Level**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-5.6
0	0	1	0	-5.2
0	0	1	1	-4.8
0	1	0	0	-4.4
0	1	0	1	-4.0
0	1	1	0	-3.6
0	1	1	1	-3.2
1	0	0	0	-2.8
1	0	0	1	-2.4
1	0	1	0	-2.0
1	0	1	1	-1.6
1	1	0	0	-1.2
1	1	0	1	-0.8
1	1	1	0	-0.4
1	1	1	1	0
3	***2***	***1***	***0***	**Tx Input Gain**
0	0	0	0	-2.65
0	0	0	1	-2.05
0	0	1	0	-1.50
0	0	1	1	-0.95
0	1	0	0	-0.45
0	1	0	1	0
0	1	1	0	0.45
0	1	1	1	0.85
1	0	0	0	1.25
1	0	0	1	1.65
1	0	1	0	2.05
1	0	1	1	2.40
1	1	0	0	2.70
1	1	0	1	3.05
1	1	1	0	3.35
1	1	1	1	3.65

Table 3 Tx Gain & Mod. Commands

The Controlling System .....

Rx Gain & LS Vol. *(Preceded by A/C 12_H)*

Setting				Gain (dBs)
MSB				**Transmitted First**
7	**6**	**5**	**4**	**Rx LS Volume**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-28.0
0	0	1	0	-26.0
0	0	1	1	-24.0
0	1	0	0	-22.0
0	1	0	1	-20.0
0	1	1	0	-18.0
0	1	1	1	-16.0
1	0	0	0	-14.0
1	0	0	1	-12.0
1	0	1	0	-10.0
1	0	1	1	-8.0
1	1	0	0	-6.0
1	1	0	1	-4.0
1	1	1	0	-2.0
1	1	1	1	0
3	**2**	**1**	**0**	**Rx Input Gain**
0	0	0	0	3.75
0	0	0	1	4.30
0	0	1	0	4.80
0	0	1	1	5.30
0	1	0	0	5.80
0	1	0	1	6.20
0	1	1	0	6.65
0	1	1	1	7.05
1	0	0	0	7.40
1	0	0	1	7.80
1	0	1	0	8.15
1	0	1	1	8.50
1	1	0	0	8.80
1	1	0	1	9.10
1	1	1	0	9.40
1	1	1	1	9.70

Table 4 Rx Gain and LS Vol. Command

LF Data Gain & Ear Vol. *(Preceded by A/C 13_H)*

Setting				Gain (dBs)
MSB				**Transmitted First**
7	**6**	**5**	**4**	**Rx Ear Volume**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-28.0
0	0	1	0	-26.0
0	0	1	1	-24.0
0	1	0	0	-22.0
0	1	0	1	-20.0
0	1	1	0	-18.0
0	1	1	1	-16.0
1	0	0	0	-14.0
1	0	0	1	-12.0
1	0	1	0	-10.0
1	0	1	1	-8.0
1	1	0	0	-6.0
1	1	0	1	-4.0
1	1	1	0	-2.0
1	1	1	1	0
3	**2**	**1**	**0**	**LF (50 Baud) Data Gain**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-2.60
0	0	1	0	-2.20
0	0	1	1	-1.80
0	1	0	0	-1.40
0	1	0	1	-1.00
0	1	1	0	-0.70
0	1	1	1	-0.35
1	0	0	0	0
1	0	0	1	0.30
1	0	1	0	0.60
1	0	1	1	0.90
1	1	0	0	1.20
1	1	0	1	1.50
1	1	1	0	1.75
1	1	1	1	2.00

Table 5 LF Data Gain and Rx Ear Volume Command

System Performance

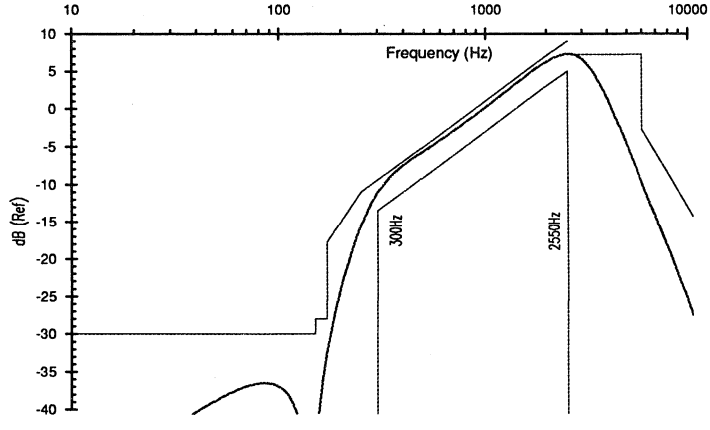


Fig.5 Tx Voiceband Frequency Response

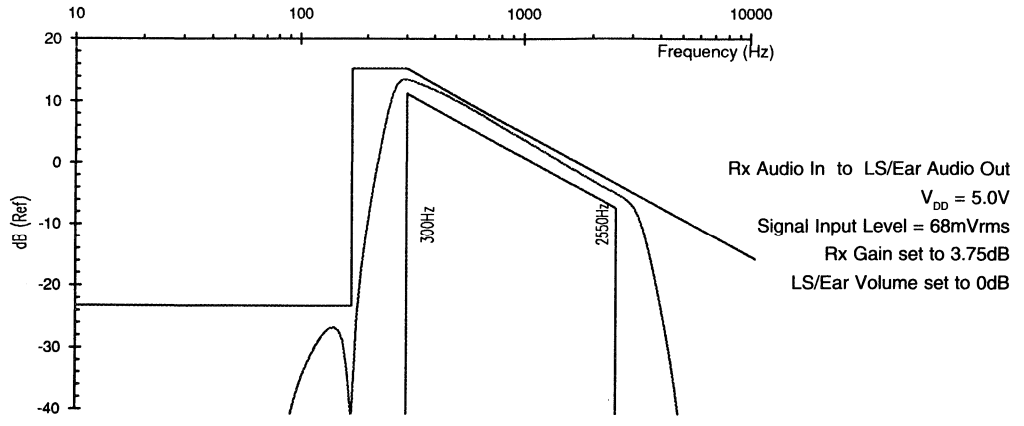


Fig.6 Rx Voiceband Frequency Response

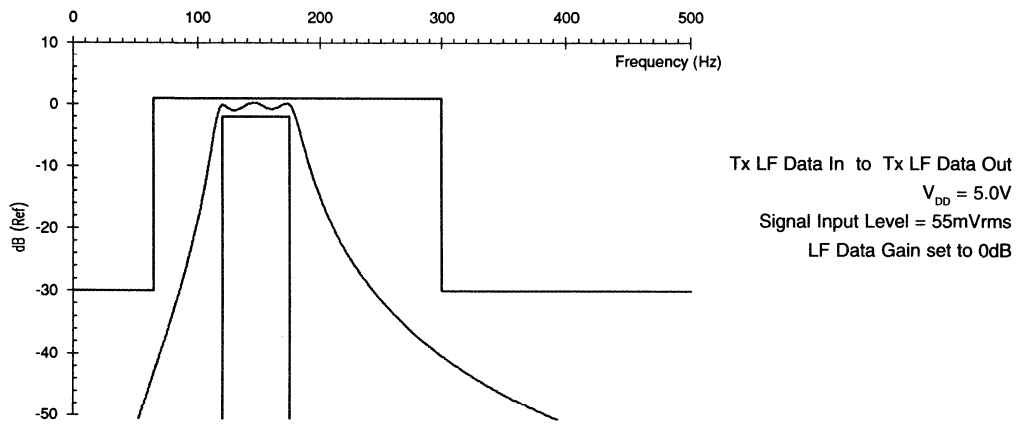


Fig.7 Tx LF Channel Frequency Response

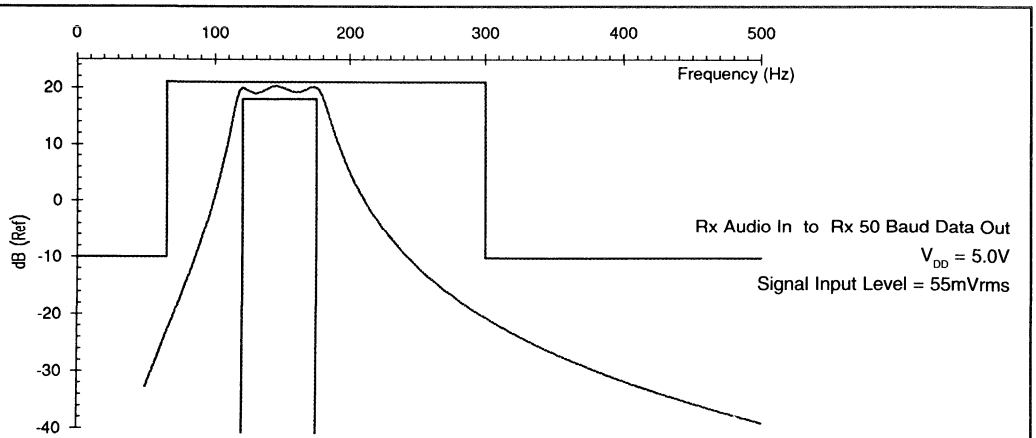


Fig.8 Rx 50-Baud Data Path Frequency Response

Control Timing Information

Timing Specification – Figures 9 and 10

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"	1	2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"	1	4.0	–	–	µs
t_{CSOFF}	"CS-High" Time between transactions	1, 2	2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time	1	2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time	1	4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns

Notes

1. These Minimum Timing values are altered during operation of the FX812 VSR Codec.
2. Chip Select must be taken to a logic "1" between each individual transaction.

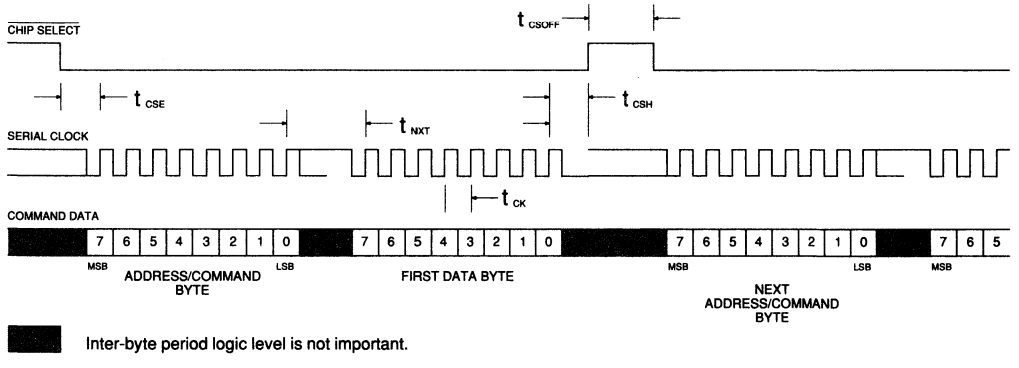


Fig.9 Control Timing Information

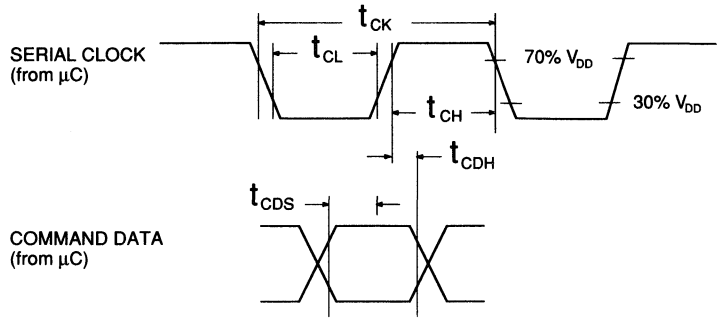


Fig.10 Control Timing Relationships

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref. V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX836DW**	-40°C to +85°C (plastic)
	FX836J	-40°C to +85°C (cerdip)
Storage temperature range:	**FX836DW**	-40°C to +85°C (plastic)
	FX836J	-55°C to +125°C (cerdip)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.032MHz. Audio level 0dB ref. = 308mV rms @ 1.0kHz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
All Operating		–	10.0	–	mA
Rx Data Mode	1	–	2.5	–	mA
Powersave All		–	0.6	–	mA
Alias Frequency		–	63.0	–	kHz
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}		–	10.0	–	kΩ
Inverter Gain		–	10.0	–	V/V
Gain/Bandwidth Product		–	10.0	–	MHz
Analogue Input Impedances					
Mic.1 & 2		–	500	–	kΩ
FFSK/Play		–	500	–	kΩ
Comp In		–	500	–	kΩ
DTMF In		–	500	–	kΩ
Dev. Limiter In		–	100	–	kΩ
(Expanded) Audio In		–	47.0	–	kΩ
Tx LF Data In		–	500	–	kΩ
Slicer In		10.0	–	–	MΩ
Rx Audio In		–	100	–	kΩ
Analogue Output Impedances					
Pre-Emp Out		–	600	–	Ω
Tx Mod Out		–	600	–	Ω
Expand/Store		–	600	–	Ω
LS and Ear Audio		–	1.0	–	kΩ
FFSK Data Out		–	600	–	Ω
Rx LF Data Out		–	2.0	–	kΩ
Tx 50 Baud Data Out		–	600	–	Ω
Switches – ON		–	1.0	–	kΩ
– OFF		10.0	–	–	MΩ
Control Interface Parameters					
Input Logic Levels					
Logic "1"	2	3.5	–	–	V
Logic "0"	2	–	–	1.5	V
I_{IN} (logic "1" or "0")	2	-1.0	–	1.0	µA
Input Capacitance	2	–	–	7.5	pF
Channel Performances					
Tx Path					
Analogue Signal Input Levels					
Mic. 1 and 2	3	–	0	–	dB
FFSK/Play	3	–	0	–	dB
DTMF	3	–	0	–	dB
Comp. In	3	–	0	–	dB
Tx LF Data In		–	0	–	dB

Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
Analogue Signal Output Levels					
Pre-Emp Out	3	–	0	–	dB
Tx Mod Out	3	–	0	–	dB
Tx LF Data Out		–	0	–	dB
Path Gains/Levels					
Tx Gain – 11_H					
Nominal Adjustment Range		-2.65		3.65	dB
Error of any Setting		-0.2	–	0.2	dB
Dev Limiter					
Threshold		–	1375	–	mVp-p
Symmetry		–	7.0	–	%
Mod Level Attenuation – 11_H					
Nominal Adjustment Range		-5.6		0	dB
Step Size		0.2	0.4	0.6	dB
Error of any Setting		-1.0	–	1.0	dB
Tx LF Data Signal Path					
Bandpass Filter					
Passband		120		175	Hz
Gain		–	0	–	dB
LF Data Gain Level – 13_H					
Nominal Adjustment Range		-2.6		2.0	dB
Error of any Setting		-0.2	–	0.2	dB
Overall					
Tx Distortion		–	-40.0	-32.0	dBp
Tx Hum and Noise		–	-40.0	-20.0	dB
Rx Signal Path					
Rx Audio Input Level	3	–	-7.0	–	dB
LS/Ear Audio Output Level	3	–	0	–	dB
Path Gains/Levels					
Rx Gain – 12_H					
Nominal Adjustment Range		3.75		9.70	dB
Error of any Setting		-0.2	–	0.2	dB
De-Emphasis					
Frequency Range		900	–	2100	Hz
Gain at 1kHz		-1.0	0	1.0	dB
Response		–	-6.0	–	dB/oct
LS/Ear Volume – $12_H/13_H$					
Nominal Adjustment Range		-28.0		0	dB
Step Size		1.5	2.0	2.5	dB
Error of any Setting		-1.0	–	1.0	dB
Overall					
Rx Distortion		–	-40.0	-32.0	dBp
Rx Hum and Noise		–	-40.0	-34.0	dB
Rx 50 Baud AudioPath					
Bandpass Filter					
Passband		120		175	Hz
Gain		19.0	20.0	21.0	dB

Notes

1. With reference to the Configuration Command and Figure 3, all functions with the exception of the Rx Gain Element may be powersaved. This will still allow signalling data through the FX836 to activate the system via the µProcessor.
2. Serial Clock, Command Data and Chip Select inputs.
3. Levels equivalent to ±1.5kHz deviation with the settings below:

   Tx Gain = 0dB *Mod Level = 0dB*
   Rx Gain = 7.05dB *LS/Ear Volume = 0dB*

   Other levels can be achieved by adjusting the above variable gain blocks in accordance with Tables 1 to 5.

Package Outlines

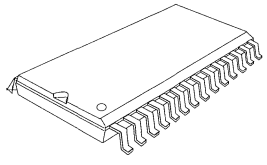
The FX836 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX836 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX836DW 28-pin plastic S.O.I.C. (D1)

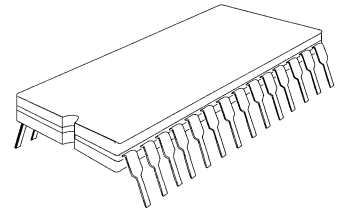
NOT TO SCALE



Max. Body Length 18.05mm
Max. Body Width 7.65mm

FX836J 28-pin cerdip DIL (J5)

NOT TO SCALE



Max. Body Length 37.05mm
Max. Body Width 13.36mm

Ordering Information

FX836DW 28-pin plastic S.O.I.C. (D1)

FX836J 28-pin cerdip DIL (J5)

Integrated Circuits Data Book

Section 4

Military Comms

CML Semiconductor Products

PRODUCT INFORMATION

FX619 'Eurocom' Delta Codec

Publication D/619/4 July 1994

Features/Applications

- Designed to Meet Eurocom D1-IA8
- Military Communications
- Delta MUX, Switch and Phone Applications
- Single Chip Full Duplex Codec
- On-Chip Input and Output Filters
- Programmable Sampling Clocks
- 3 or 4-bit Compand Algorithm
- Forced Idle Facility
- Powersave Facility
- Single 5V CMOS Process
- Full Duplex CVSD* Codec

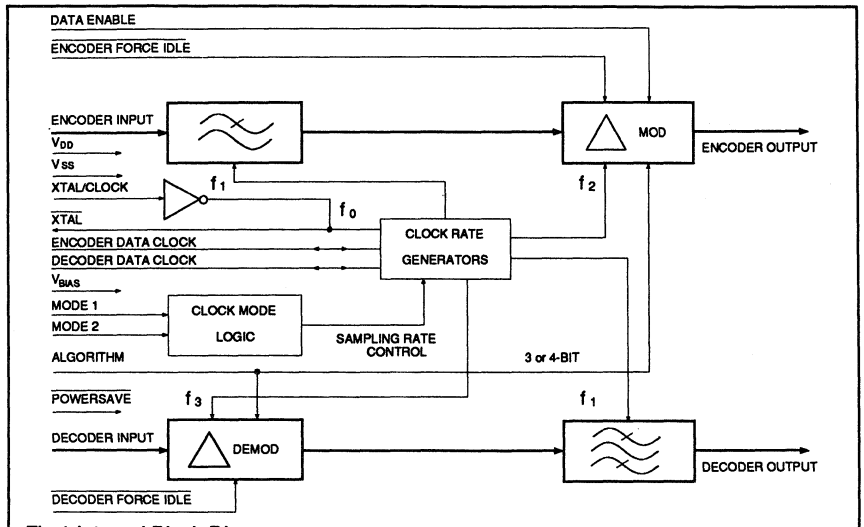


Fig.1 Internal Block Diagram

FX619

Brief Description

The FX619 is an LSI circuit designed as a *Continuously Variable Slope Delta Codec and is intended for use in military communications systems.

Designed to meet Eurocom D1-IA8 with external components, the device is suitable for applications in military Delta Multiplexers, switches and phones.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32 or 64 k bits/second from an internal clock generator or may be externally applied in the range 8 to 64 k bits/second. Sampling clock frequencies are output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. Encoder and Decoder forced idle facilities are provided forcing a 10101010..... pattern in encode and a $V_{DD}/2$ bias in decode. The companding circuits may be operated with a 3 or 4-bit algorithm which is externally selected. The device may be put in the standby mode by selection of the powersave facility. A reference 1.024MHz oscillator uses an external clock or Xtal.

The FX619 is a low-power, 5 volt CMOS device and is available in 22-pin cerdip DIL and 28-lead ceramic leadless SMT packages.

Pin Number		Function
FX619J	FX619M1	
1	1	**Xtal/Clock :** Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 3.
	2	No connection
2	3	**$\overline{\text{Xtal}}$:** Output of clock oscillator inverter. Xtal circuitry shown is in accordance with CML application note D/XT/1 April 1986.
3	4	No connection
4	5	**Encoder Data Clock :** A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependant upon clock mode 1, 2 inputs and Xtal frequency (see Clock Mode pins).
5	6	**Encoder Output :** The encoder digital output, this is a three state output whose condition is set by Data Enable and Powersave inputs as shown :
	7, 8	No connection
6	9	**$\overline{\text{Encoder Force Idle}}$:** When this pin is a logical '0' the encoder is forced to an idle state and the encoder digital output is 0101..., a perfect idle pattern. When this pin is a logical '1' the encoder encodes as normal. Internal 1MΩ Pullup.
7	10	**Data Enable :** Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1MΩ Pullup.
8	11	No connection
9	12	**Bias :** Normally at V_{DD} /2 bias, this pin requires to be externally decoupled by a capacitor, C_4. Internally pulled to V_{SS} when "Powersave" is a logical '0'.
10	13	**Encoder Input :** The analogue signal input. Internally biased at V_{DD} /2, external components are required on this input. The source impedance should be less than 100Ω, output idle channel noise levels will improve with an even lower source impedance. See Fig. 3.
11	14	**V_{SS} :** Negative Supply.

Data Enable	$\overline{\text{Powersave}}$	Encoder Output
1	1	Enabled
0	1	High Z (o/c)
1	0	Vss

Pin Number		Function
FX619J	FX619M1	
12	15,16	No connection
13	17	**Decoder Output :** The recovered analogue signal is output at this pin, it is the buffered output of a bandpass filter and requires external components. During "Powersave" this output is o/c.
14	18,19	No connection
15	20	$\overline{\text{Powersave}}$ **:** A logical '0' at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical '1' the codec operates normally. Internal 1MΩ Pullup.
	21	No connection
16	22	$\overline{\text{Decoder Force Idle}}$ **:** A logical '0' at this pin gates a 0101...pattern internally to the decoder so that the decoder output goes to $V_{DD}/2$. When this pin is at a logical '1' the decoder operates as normal. Internal 1MΩ Pullup.
17	23	**Decoder Input :** The received digital signal input. Internal 1MΩ Pullup.
18	24	**Decoder Data Clock :** A Logic I/O port. External decode clock input or internal data clock output, dependant upon clock mode 1, 2 inputs, see Clock Mode pins.
19	25	**Algorithm :** A logical '1' at this pin sets this device for a 3-bit companding algorithm. A logical '0' sets a 4-bit companding algorithm. Internal 1MΩ Pullup.
20	26	**Clock Mode 2 :**
21	27	**Clock Mode 1 :** Internal 1MΩ Pullups.

Clock Mode 1	Clock Mode 2	Facility
0	0	External clocks
0	1	Internal, 64kb/s = f ÷ 16
1	0	Internal, 32kb/s = f ÷ 32
1	1	Internal, 16kb/s = f ÷ 64

Clock rates refer to f = 1.024 MHz Xtal/clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independant or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode.

22	28	V_{DD} **:** Positive Supply. A single + 5 volt power supply is required.

Codec Integration

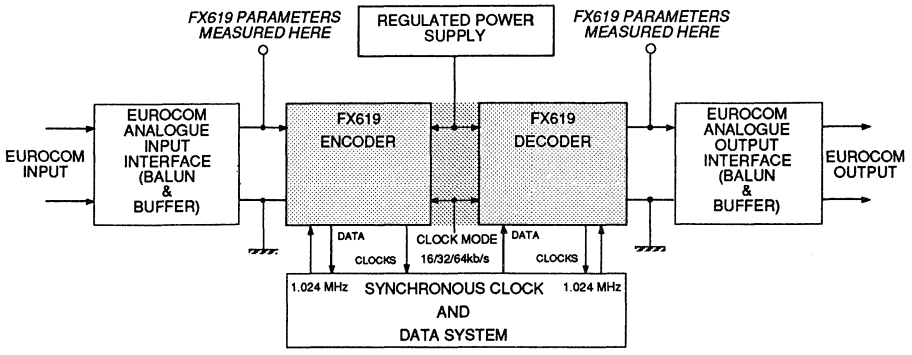


Fig.2 Eurocom System Configuration – showing the FX619, which with the indicated interfacing, will conform to the Eurocom Basic Parameters Specification D1 – IA8.

Component	Unit Value	**Note** – with reference to Figure 3 (below)
R_1	1M	Oscillator Inverter bias resistor.
R_2	Selectable	Xtal Drive limiting resistor.
C_1	33p	Xtal Circuit drain capacitor.
C_2	33p	Xtal Circuit gate capacitor.
C_3	1.0µ	Encoder Input coupling capacitor – The drive source impedance to this input should be less than 100Ω. Output Idle channel noise levels will improve with an even lower source impedance.
C_4	1.0µ	Bias decoupling capacitor.
C_5	1.0µ	V_{DD} decoupling capacitor.
X_1	1.024 MHz	A 1.024 MHz Xtal/clock input will yield exactly 16/32/64 kb/s data clock rates. Xtal circuitry shown is in accordance with CML application note D/XT/1 April 1986.

Tolerance :– Resistors ± 10% Capacitors ± 20%

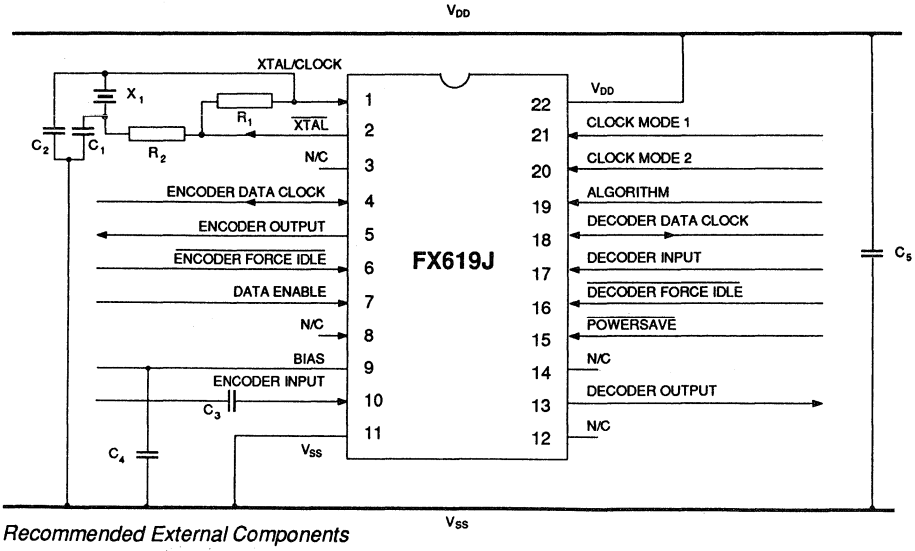
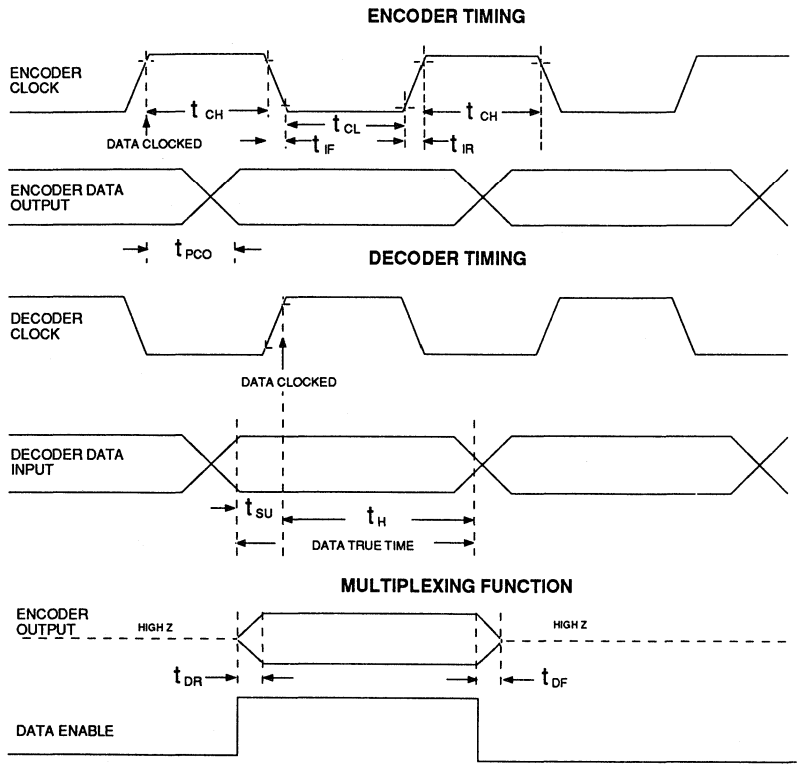


Fig.3 Recommended External Components

Codec Timing Information



TIMING

t_{CH} Clock '1' Pulse Width 1.0µs Min.

t_{CL} Clock '0' Pulse Width 1.0µs Min.

t_{IR} Clock Rise Time 100ns Typ.

t_{IF} Clock Fall Time 100ns Typ.

t_{SU} Data Set-up Time 450ns Min.

t_H Data Hold Time 600ns Min.

$t_{SU} + t_H$ Data True Time.

t_{PCO} Clock to Output Delay time 750ns Max.

t_{DR} Data Rise Time 100ns Typ.

t_{DF} Data Fall Time 100ns Typ.

Xtal Input Frequency 1.024MHz.

Fig.4 Codec Timing Diagrams

Codec Performance Using the Bit Sequence Tests (a to g) at the Decoder Input pin in accordance with the Eurocom Specification D1 – IA8, the decoder output is as shown in Table 1.

Test	Sample Rate	Bit Sequence at Decoder Input	MLA Duty cycle	Typical Output Level
a.	16kbit/s	1011010010010010 1101	0	- 41.5dBm0
	32kbit/s	1011011010101001001001001010101101101	0	- 42.0dBm0
b.	16kbit/s	1101100100100100 1101	0.05	- 25.0dBm0
	32kbits	1011011010101001001000100100101011011011	0.05	- 25.0dBm0
c.	16kbits	1011010100010010 1011	0.1	- 19.0dBm0
	32kbit/s	1101101101010010001000100100101011011101	0.1	- 18.5dBm0
d.	16kbit/s	1101100100000100 11011	0.2	- 11.0dBm0
	32kbit/s	1101110110010100010000100010011010111011	0.2	- 11.5dBm0
e.	16kbit/s	1101101000001001 0111	0.3	- 6.5dBm0
	32kbit/s	1110111011001000100000010001001101110111	0.3	- 6.5dBm0
f.	16kbit/s	1101101000000100 1111	0.4	- 3.0dBm0
	32kbit/s	1111011101010001000000001000101011101111	0.4	- 3.0dBm0
g.	16kbit/s	1110101000000010 1111	0.5	0dBm0
	32kbit/s	1111101110100010000000000100010111011111	0.5	0dBm0

Table 1 Bit Sequence Test Table

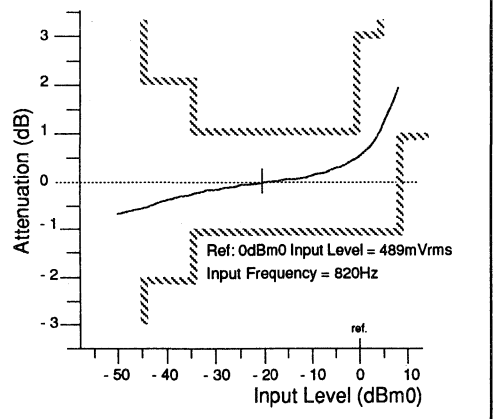


Fig.5 Gain vs Input Level (16kbit/s)

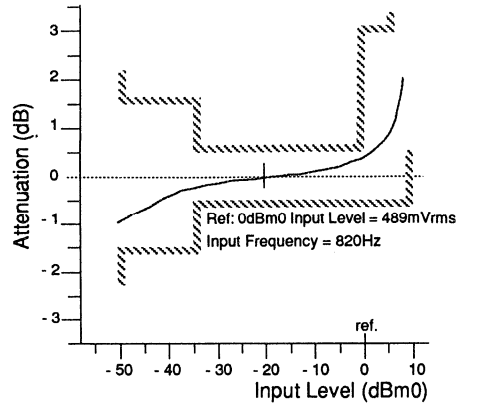


Fig.6 Gain vs Input Level (32kbit/s)

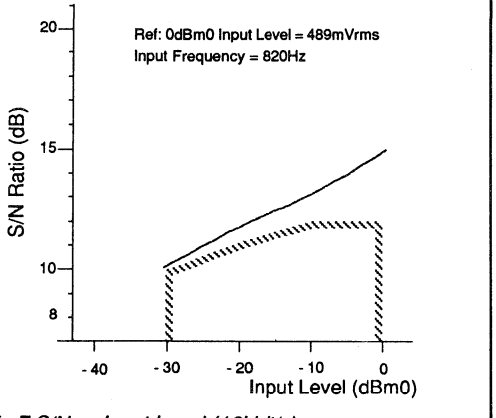


Fig.7 S/N vs Input Level (16kbit/s)

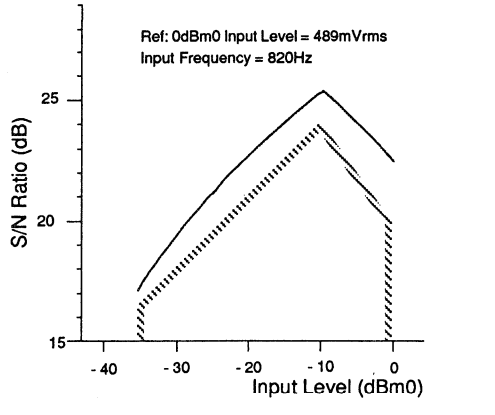


Fig.8 S/N vs Input Level (32kbit/s)

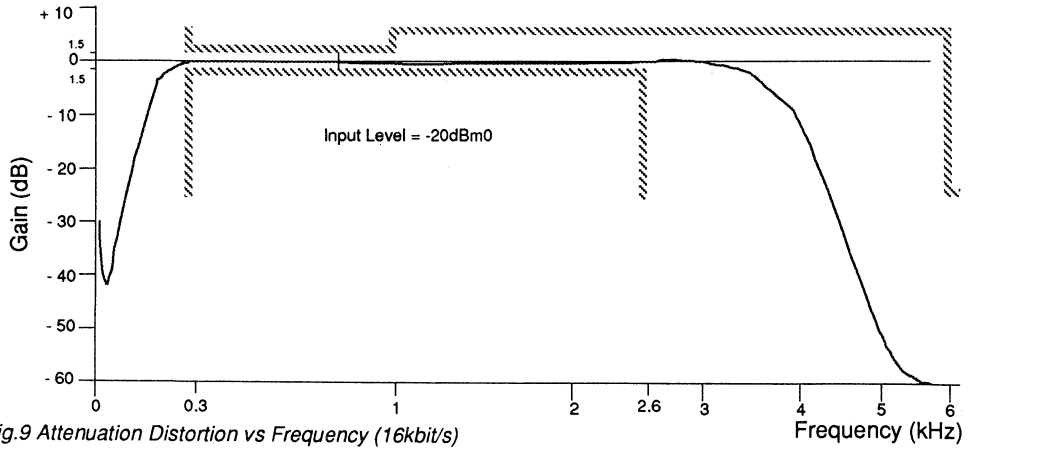


Fig.9 Attenuation Distortion vs Frequency (16kbit/s)

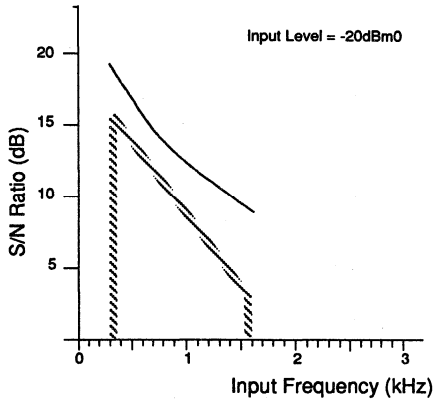


Fig.10 S/N vs Input Frequency (16kbit/s)

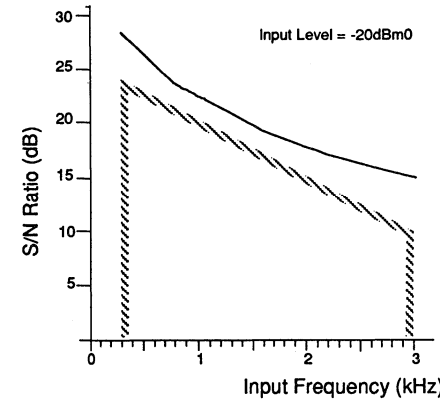


Fig.11 S/N vs Input Frequency (32kbit/s)

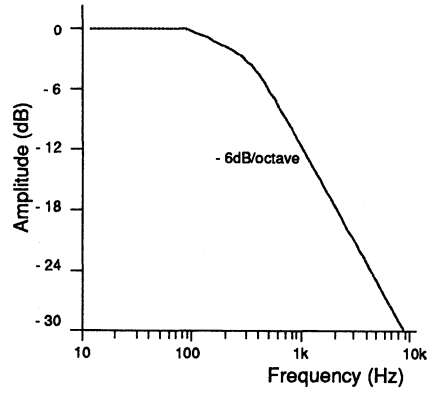


Fig.12 Principal Integrator Response

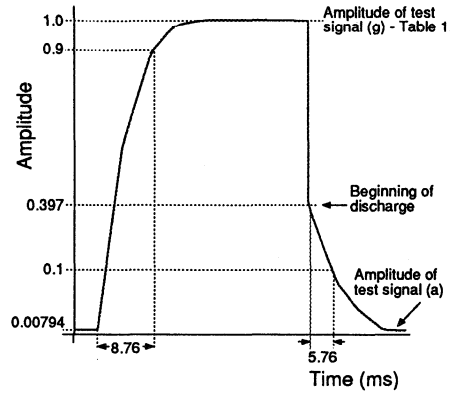


Fig.13 Compand Envelope

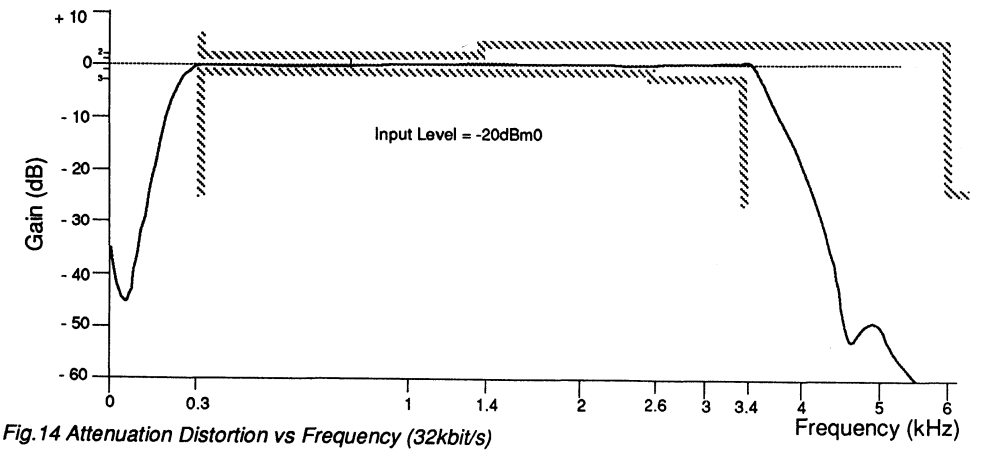


Fig.14 Attenuation Distortion vs Frequency (32kbit/s)

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Source/sink current (supply pins)		± 30mA
(other pins)		± 20mA
Total device dissipation @ 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX619J**	-40°C to +85°C (cerdip)
	FX619M1	-40°C to +85°C (cerquad)
Storage temperature range:	**FX619J**	-55°C to +125°C (cerdip)
	FX619M1	-55°C to +125°C (cerquad)

Operating Limits

All characteristics are measured using the following parameters unless otherwise specified:
V_{DD} = 5.0V, T_{AMB} = 25°C, Xtal/Clock f_0 = 1.024MHz, Audio Level 0dB ref (0dBm0) = 489 mV rms.
Audio Test Frequency = 820 Hz. Sample Clock Rate = 32kb/s. Compand Algorithm = 3-bit.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)		–	4.5	–	mA
Supply Current (Powersave)		–	1.0	–	mA
Inputs Logic '1'	8	3.5	–	–	V
Inputs Logic '0'	8	–	–	1.5	V
Outputs Logic '1'	8	4.0	–	–	V
Outputs Logic '0'	8	–	–	1.0	V
Digital Input Impedance (Logic I/O pins)		1.0	10	–	MΩ
Digital Input Impedance (Logic input pins, pullup resistor)	2	300	–	–	kΩ
Digital Output Impedance		–	–	4	kΩ
Analogue Input Impedance	4		1	–	kΩ
Analogue Output Impedance	7	–	–	800	Ω
Three State Output Leakage Current (output disabled)		-4	–	+4	µA
Insertion Loss	3	-2	–	+2	dB
Dynamic Values	1				
Encoder:					
Analogue Signal Input Levels	5,9	-35	–	+6	dBm0
Principle Integrator Frequency		–	275	–	Hz
Encoder Passband			3400		Hz
Compand Time Constant		–	4	–	ms
Decoder:					
Analogue Signal Output Levels	5,9	-35	–	+6	dBm0
Decoder Passband		300	–	3400	Hz
Encoder Decoder (Full codec):					
Compression Ratio (Cd = 0.5 to Cd = 0.0)		–	50	–	
Passband		300	–	3400	Hz
Stopband		6	–	10	kHz
Stopband Attenuation		–	60	–	dB
Passband Gain		–	0	–	dB
Passband Ripple (300Hz –1400Hz)		-1	–	+1	dB
(1400Hz – 2600Hz)		-1	–	+3	dB
(2600Hz – 3400Hz)		-2	–	+3	dB
Output Noise (Input short circuit)	9	–	–	-62	dBm0p
Perfect Idle Channel Noise (Encoder forced)	9	–	-63	–	dBm0p
Group Delay Distortion	6				
(1000Hz to 2600Hz)		–	–	450	µs
(600Hz to 2800Hz)		–	–	750	µs
(500Hz to 3000Hz)		–	–	1.5	ms
Xtal/Clock Frequency		500	1024	1500	kHz

› › › ›

Specifications

Process Information

The following Table gives details of the process and test controls employed in the manufacture of the FX619 Eurocom Delta Codec.

Function	Reference	Remarks
Hermeticity		
Fine Leak Test –	Mil Std 883C	using Method 1014 – test condition A1.
Coarse Leak Test –	Mil Std 883C	using Method 1014 – test condition C.
Burnin	Mil Std 883C	using Method 1015 – test condition E. 168 Hours @ 85°C with 5v power, and clocks applied.
Temperature Cycling	Mil Std 883C	using Method 1010 – test condition B. 10 cycles -55°C to +125°C.
The following mechanical assembly tests are Qualified to BS9450		
Vibration	BS9450	Section 1.2.6.8.1 55Hz to 500Hz at 98 m/sec acceleration.
Shock	BS9450	Section 1.2.6.6 981 m/sec for 6 msec.
Low Pressure	BS9450	Section 1.2.6.12
Transport and Storage –		225mmHg (altitude 9000m).
Operation –		600mmHg (altitude 2400m).
Humidity	BS9450	Section 1.2.6.4 96 Hours @ 45°C, 95% relative humidity plus condensed water.

Notes:
1. Dynamic characteristics are specified at 5V unless otherwise specified.
2. All logic inputs except, Encoder and Decoder Data Clocks.
3. For an Encoder/Decoder combination, Insertion Loss contributed by a single component is half this figure.
4. Driven with a source impedance of <100Ω.
5. Recommended values – See Figures 5, 6, 7 and 8.
6. Group Delay Distortion for the full codec is relative to the delay with 820Hz, -20dB at the encoder input.
7. An Emitter Follower output stage.
8. 4V = 80% V_{DD}, 3.5V = 70% V_{DD}, 1.5V = 30% V_{DD}, 1V = 20% V_{DD}.
9. Analogue Voltage Levels used in this Data Sheet: 0dBm0 = 489mVrms = - 4dBm = 0dB. - 20dBm0 = 49mVrms = - 24dBm.

Application Recommendations

Due to the very low levels of signal and idle channel noise specified in the Eurocom Basic Parameters Specification D1 – IA8 – a noisy or badly regulated power supply could cause instability putting the overall system performance out of specification. Adherence to the points noted below will assist in minimizing this problem.

(a) Care should be taken on the design and layout of the printed circuit board.

(b) All external components (as recommended in Figure 3) should be kept close to the package.

(c) Tracks should be kept short, particularly the Encoder Input capacitor and the V_{BIAS} capacitor.

(d) Xtal/clock tracks should be kept well away from analogue inputs and outputs.

(e) Inputs and outputs should be screened wherever possible.

(f) A "ground plane" connected to V_{SS} will assist in eliminating external pick-up on the input and output pins.

(g) It is recommended that the power supply rails have less than 1mVrms of noise allowed.

(h) The source impedance to the Encoder Input pin must be less than 100Ω, Output Idle channel noise levels will improve with even lower source impedances.

Package Outlines

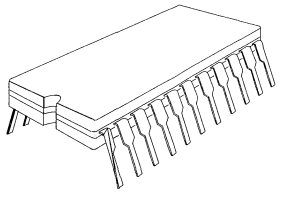
The FX619 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX619 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX619J 22-pin cerdip DIL (J3)

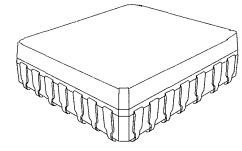
NOT TO SCALE



Max. Body Length	27.38mm
Max. Body Width	9.75mm

FX619M1 28-lead ceramic leaded chip carrier (M1)

NOT TO SCALE



Max. Body Length	11.50mm
Max. Body Width	11.50mm

Ordering Information

FX619J 22-pin cerdip DIL (J3)

FX619M1 28-lead ceramic leaded chip carrier (M1)

CML Semiconductor Products

PRODUCT INFORMATION

FX629 Delta Modulation Codec for Military Applications

Publication D/629/2 July 1994
Provisional Issue

Features/Applications

- Designed to Meet Mil-Std-188-113
- Military Communications
- Delta MUX, Switch and Phone Applications
- Single-Chip Full-Duplex Codec
- On-Chip Input and Output Filters
- Programmable Sampling Clocks
- 3 or 4-bit Compand Algorithm
- Forced Idle Facility
- Powersave Facility
- Single 5V CMOS Process
- Full-Duplex CVSD* Codec

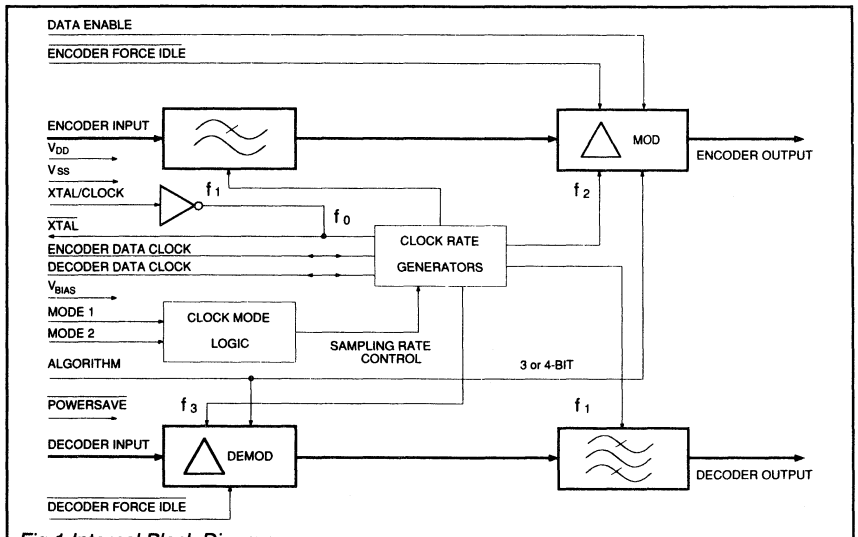


Fig.1 Internal Block Diagram

FX629

Brief Description

The FX629 is an LSI circuit designed as a *Continuously Variable Slope Delta Codec and is intended for use in military communications systems.

Designed to meet Mil-Std-188-113 with external components, the device is suitable for applications in military Delta Multiplexers, switches and phones.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32 or 64 k bits/second from an internal clock generator or may be externally applied in the range 8 to 64 k bits/second. Sampling clock frequencies are output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications.

Encoder and Decoder forced idle facilities are provided, forcing a 10101010..... pattern in encode and a $V_{DD}/2$ bias in decode.

The companding circuits may be operated with a pin-selected 3 or 4-bit algorithm.

The powersave facility puts the device into the standby mode thereby reducing current consumption when not operating.

A reference 1.024MHz oscillator uses an external clock pulse or Xtal input.

The FX629 is a low-power, 5 volt CMOS device and is available in a 22-pin cerdip DIL package.

Pin Number Function

FX629J	
1	**Xtal/Clock :** Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 3.
2	**$\overline{\text{Xtal}}$:** Output of clock oscillator inverter. Xtal circuitry shown is in accordance with CML Application Note D/XT/1 April 1986.
3	No connection
4	**Encoder Data Clock :** A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependant upon clock mode 1, 2 inputs and Xtal frequency (see Clock Mode pins).
5	**Encoder Output :** The encoder digital output, this is a three state output whose condition is set by Data Enable and Powersave inputs as shown :
6	**$\overline{\text{Encoder Force Idle}}$:** When this pin is a logical '0' the encoder is forced to an idle state and the encoder digital output is 0101..., a perfect idle pattern. When this pin is a logical '1' the encoder encodes as normal. Internal 1MΩ Pullup.
7	**Data Enable :** Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1MΩ Pullup.
8	No connection
9	**Bias :** Normally at V_{DD} /2 bias, this pin requires to be externally decoupled by a capacitor, C_4. Internally pulled to V_{SS} when "Powersave" is a logical '0'.
10	**Encoder Input :** The analogue signal input. Internally biased at V_{DD} /2, external components are required on this input. The source impedance should be less than 100Ω, output idle channel noise levels will improve with an even lower source impedance. See Figure 3.
11	**V_{SS} :** Negative Supply.

Data Enable	$\overline{\text{Powersave}}$	Encoder Output
1	1	Enabled
0	1	High Z (o/c)
1	0	Vss

Pin Number Function

FX629J	
12	No connection
13	**Decoder Output :** The recovered analogue signal is output at this pin, it is the buffered output of a bandpass filter and requires external components. During "Powersave" this output is open circuit.
14	No connection
15	$\overline{\text{Powersave}}$ **:** A logical '0' at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical '1' the codec operates normally. Internal 1MΩ Pullup.
16	$\overline{\text{Decoder Force Idle}}$ **:** A logical '0' at this pin gates a 0101...pattern internally to the decoder so that the decoder output goes to $V_{DD}/2$. When this pin is at a logical '1' the decoder operates as normal. Internal 1MΩ Pullup.
17	**Decoder Input :** The received digital signal input. Internal 1MΩ Pullup.
18	**Decoder Data Clock :** A Logic I/O port. External decode clock input or internal data clock output, dependant upon clock mode 1, 2 inputs, see Clock Mode pins.
19	**Algorithm :** A logical '1' at this pin sets this device for a 3-bit companding algorithm. A logical '0' sets a 4-bit companding algorithm. Internal 1MΩ Pullup.
20	**Clock Mode 2 :**
21	**Clock Mode 1 :** Internal 1MΩ Pullups.

Clock Mode 1	Clock Mode 2	Facility
0	0	External clocks
0	1	Internal, 64kb/s = f ÷ 16
1	0	Internal, 32kb/s = f ÷ 32
1	1	Internal, 16kb/s = f ÷ 64

Clock rates refer to f = 1.024 MHz Xtal/clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization.
Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Optimum performance will be achieved when the applied external clocks are synchronous with the master Xtal/clock, and a sub-multiple of 128kHz.

22	V_{DD} **:** Positive Supply. A single + 5 volt power supply is required.

Codec Integration

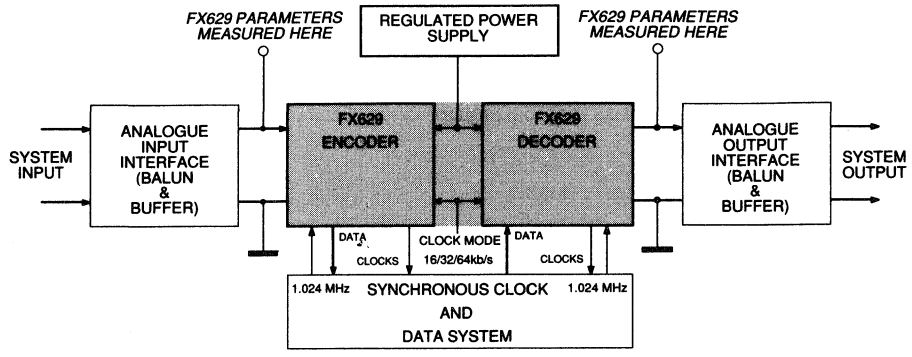


Fig.2 System Configuration Diagram – showing the FX629, which with the indicated interfacing, will conform to the Mil-Std-188-113 Specification

Component	Unit Value	**Note** – with reference to Figure 3 (below)
R_1	1M	Oscillator Inverter bias resistor.
R_2	Selectable	Xtal Drive limiting resistor.
C_1	33p	Xtal Circuit drain capacitor.
C_2	33p	Xtal Circuit gate capacitor.
C_3	1.0µ	Encoder Input coupling capacitor – The drive source impedance to this input should be less than 100Ω. Output Idle channel noise levels will improve with an even lower source impedance.
C_4	1.0µ	Bias decoupling capacitor.
C_5	1.0µ	V_{DD} decoupling capacitor.
X_1	1.024 MHz	A 1.024 MHz Xtal/clock input will yield exactly 16/32/64 kb/s data clock rates. Xtal circuitry shown is in accordance with CML application note D/XT/1 April 1986.

Tolerance :– Resistors ± 10% Capacitors ± 20%

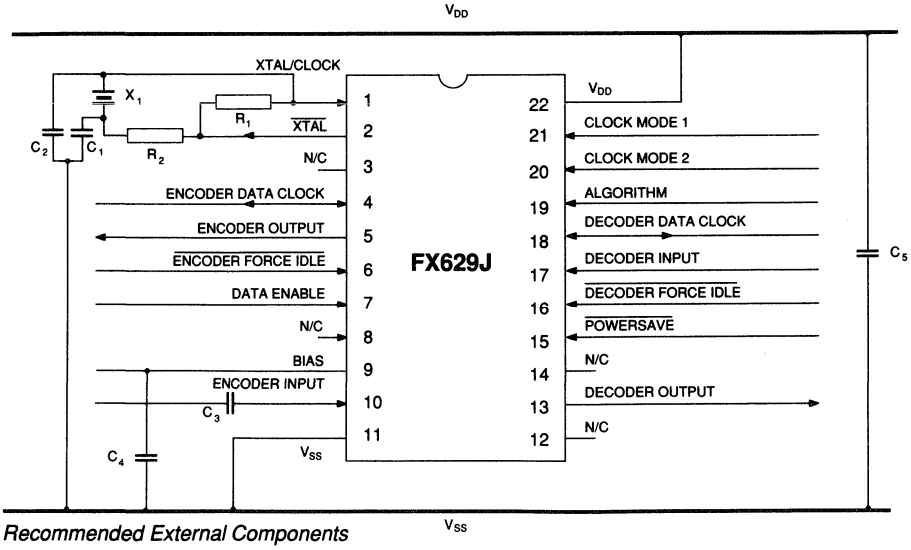
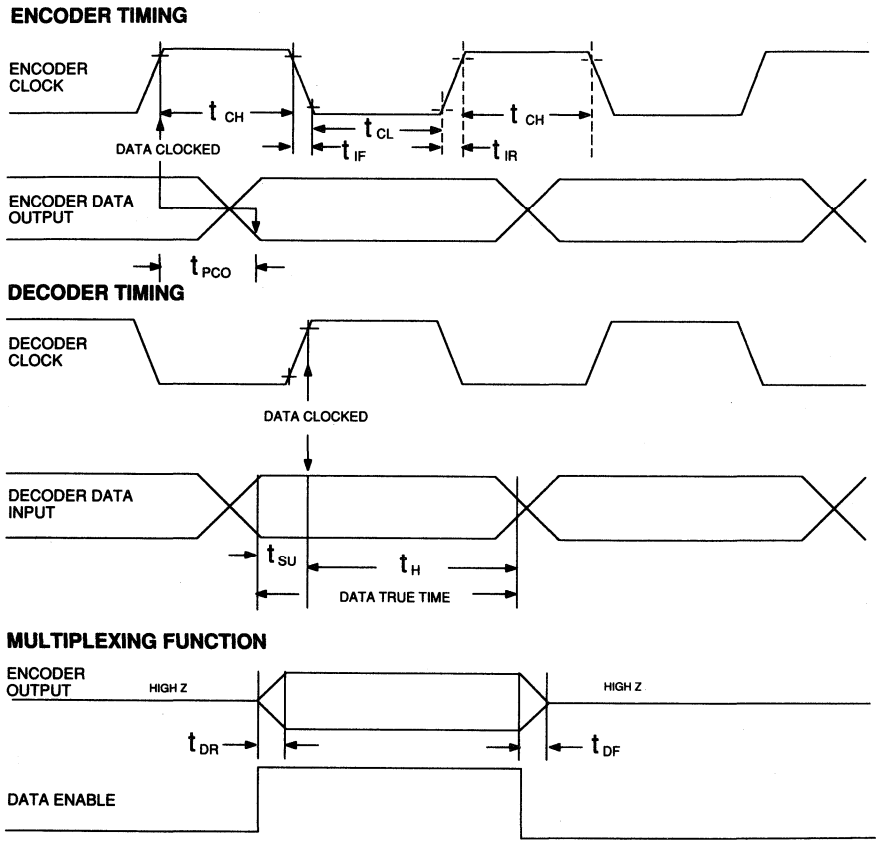


Fig.3 Recommended External Components

Codec Timing Information



TIMING

t_{CH} **Clock '1' Pulse Width** 1.0µs Min.	t_{IR} **Clock Rise Time** 100ns Typ.	t_{SU} **Data Set-up Time** 450ns Min.	$t_{SU} + t_H$ **= Data True Time**
t_{CL} **Clock '0' Pulse Width** 1.0µs Min.	t_{IF} **Clock Fall Time** 100ns Typ.	t_H **Data Hold Time** 600ns Min.	t_{PCO} **Clock to Output Delay Time** 750ns Max.
	t_{DR} **Data Rise Time** 100ns Typ.	t_{DF} **Data Fall Time** 100ns Typ.	**Xtal Input Frequency** 1.024MHz.

Fig.4 Codec Timing Diagrams

Digital to Analogue Performance ..... Using the bit sequence tests shown in Table 1 (below) at the Decoder Input pin, the analogue signals measured at the Decoder Output pin are 800Hz ± 10Hz at the levels described.

Sample Rate	Bit Sequence at Decoder Input	"Run of Threes" *(%)*	Output Level *(dBm0)*
16kbit/s	11011011010010010	0	-29.2 ± 2
32kbit/s	11011011010101001001001001001010101101 10	0	-30.0 ± 2
16kbit/s	11111011010000010010	30	0 ± 1
32kbits	11111101101010100001000000100101010111 10	30	0 ± 1

Table 1 Bit Sequence Tests and Results at 800Hz

Typical Codec Performance ..... relative to the Mil-Std-188-113 Specification

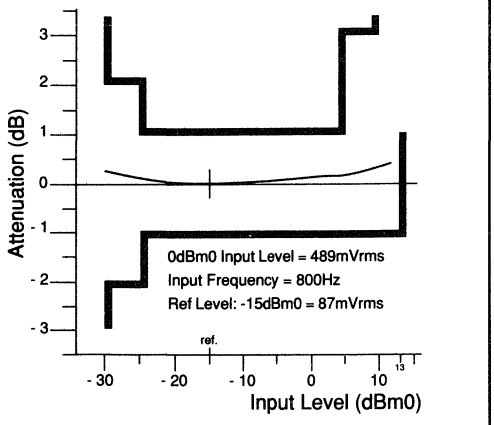


Fig.5 Gain vs Input Level (16kbit/s)

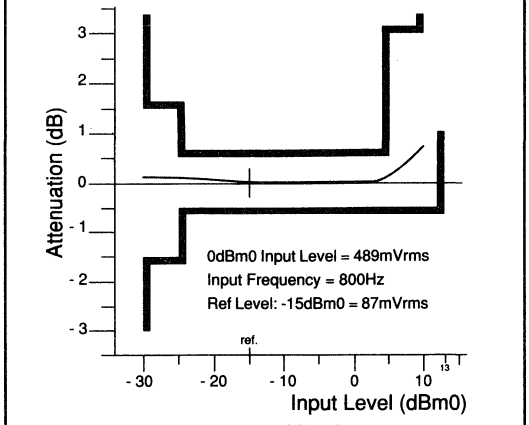


Fig.6 Gain vs Input Level (32kbit/s)

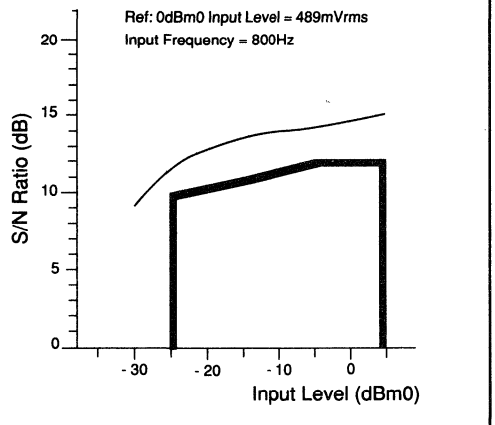


Fig.7 S/N vs Input Level (16kbit/s)

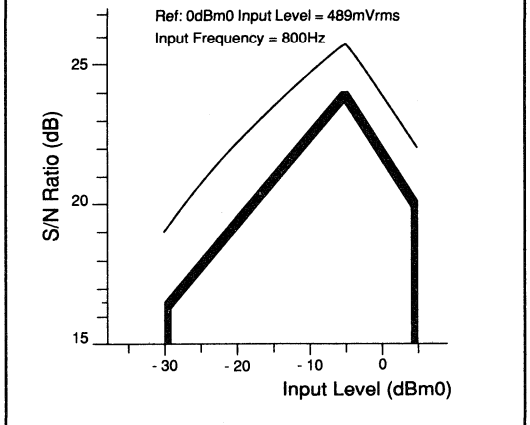


Fig.8 S/N vs Input Level (32kbit/s)

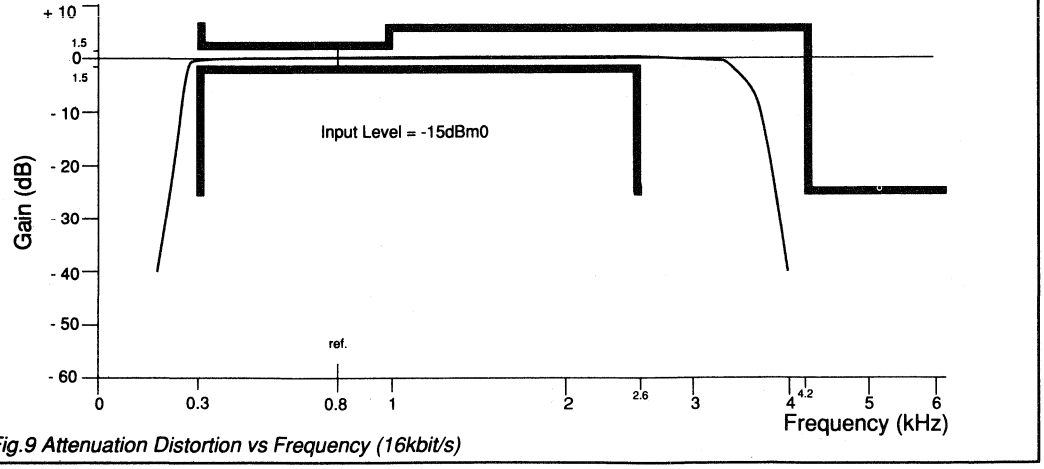


Fig.9 Attenuation Distortion vs Frequency (16kbit/s)

Typical Codec Performance ..... relative to the Mil-Std-188-113 Specification

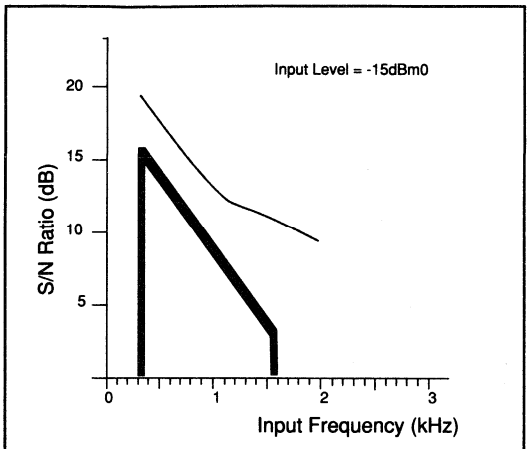


Fig.10 S/N vs Input Frequency (16kbit/s)

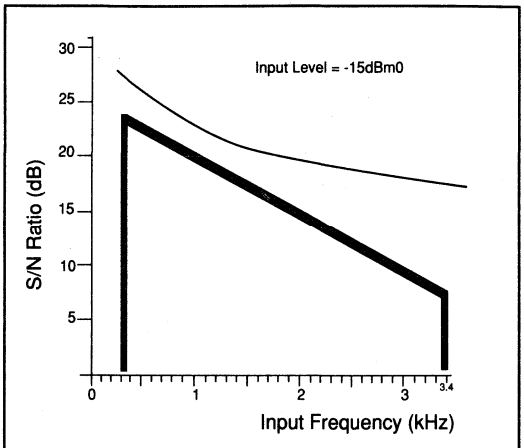


Fig.11 S/N vs Input Frequency (32kbit/s)

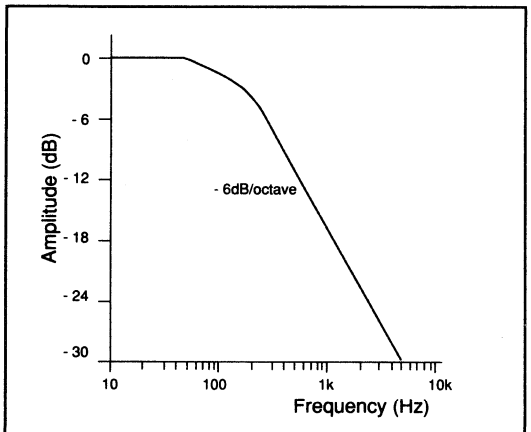


Fig.12 Principal Integrator Response

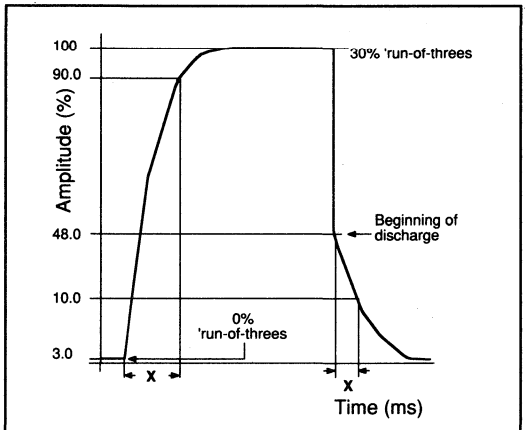


Fig.13 Compand Envelope

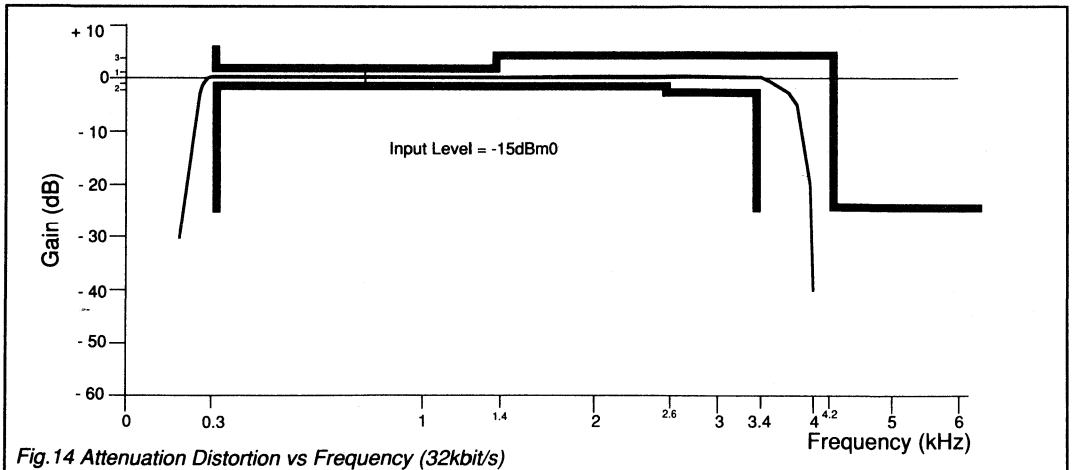


Fig.14 Attenuation Distortion vs Frequency (32kbit/s)

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Source/sink current (supply pins)	± 30mA
(other pins)	± 20mA
Total device dissipation @ 25°C	800mW Max.
Derating	10mW/°C
Operating temperature range: **FX629J**	-40°C to +85°C
Storage temperature range: **FX629J**	-55°C to +125°C

Operating Limits

All characteristics are measured using the following parameters unless otherwise specified:
V_{DD} = 5.0V, T_{AMB} = 25°C, Xtal/Clock f_0 = 1.024MHz, Audio Level 0dB ref (0dBm0) = 489 mV rms.
Audio Test Frequency = 800 Hz. Sample Clock Rate = 32kb/s. Compand Algorithm = 3-bit.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)		–	5.5	–	mA
Supply Current (Powersave)		–	0.4	–	mA
Inputs Logic '1'	8	3.5	–	–	V
Inputs Logic '0'	8	–	–	1.5	V
Outputs Logic '1'	8	4.0	–	–	V
Outputs Logic '0'	8	–	–	1.0	V
Digital Input Impedance (Logic I/O pins)		1.0	10.0	–	MΩ
Digital Input Impedance (Logic input pins, pullup resistor)	2	300	–	–	kΩ
Digital Output Impedance		–	–	4	kΩ
Analogue Input Impedance	4	–	1.0	–	kΩ
Analogue Output Impedance	7	–	–	800	Ω
Three State Output Leakage Current (output disabled)		-4.0	–	+4.0	µA
Insertion Loss	3	-2.0	–	+2.0	dB
Dynamic Values	1,9				
Encoder:					
Analogue Signal Input Levels	5,9	-35.0	–	+12.0	dBm0
Principle Integrator Frequency		127	159	212	Hz
Encoder Passband			3400		Hz
Compand Time Constant		4.0	5.0	6.0	ms
Decoder:					
Analogue Signal Output Levels	5,9	-35.0	–	+12.0	dBm0
Decoder Passband		300	–	3400	Hz
Encoder Decoder (Full codec):					
Compression Ratio (Cd = 0.3 to Cd = 0.0)		–	16:1	–	
Passband		300	–	3400	Hz
Stopband		4.2	–	–	kHz
Stopband Attenuation (4200Hz to 6000Hz)		25.0	–	–	dB
(> 6kHz)		–	60.0	–	dB
Passband Gain		–	0	–	dB
Passband Ripple (300Hz –1400Hz)		-1.0	–	+1.0	dB
(1400Hz – 2600Hz)		-1.0	–	+3.0	dB
(2600Hz – 3400Hz)		-2.0	–	+3.0	dB
Output Noise (Input short circuit)	9	–	-55.0	–	dBm0
Perfect Idle Channel Noise (Encoder forced)	9	–	-57.0	–	dBm0
Group Delay Distortion	6				
(1000Hz to 2600Hz)		–	–	450	µs
(600Hz to 2800Hz)		–	–	750	µs
(500Hz to 3000Hz)		–	–	1.5	ms
Xtal/Clock Frequency		–	1024	–	kHz

Specifications .....

Process Information

The following Table gives details of the process and test controls employed in the manufacture of the FX629 'Mil Std' Delta Codec.

Function	Reference	Remarks
Hermeticity		
Fine Leak Test –	Mil Std 883C	using Method 1014 – test condition A1.
Coarse Leak Test –	Mil Std 883C	using Method 1014 – test condition C.
Burnin	Mil Std 883C	using Method 1015 – test condition E. 168 Hours @ 85°C with 5v power, and clocks applied.
Temperature Cycling	Mil Std 883C	using Method 1010 – test condition B. 10 cycles -55°C to +125°C.
The following mechanical assembly tests are Qualified to BS9450		
Vibration	BS9450	Section 1.2.6.8.1 55Hz to 500Hz at 98 m/sec acceleration.
Shock	BS9450	Section 1.2.6.6 981 m/sec for 6 msec.
Low Pressure	BS9450	Section 1.2.6.12
Transport and Storage –		225mmHg (altitude 9000m).
Operation –		600mmHg (altitude 2400m).
Humidity	BS9450	Section 1.2.6.4 96 Hours @ 45°C, 95% relative humidity plus condensed water.

Notes:
1. Dynamic characteristics are specified at 5V unless otherwise specified.
2. All logic inputs except, Encoder and Decoder Data Clocks.
3. For an Encoder/Decoder combination, insertion loss contributed by a single component is half this figure.
4. Driven with a source impedance of <100Ω.
5. Recommended values – See Figures 5, 6, 7 and 8.
6. Group Delay Distortion for the full codec is relative to the delay with 820Hz, -20dB at the encoder input.
7. An Emitter Follower output stage.
8. 4.0V = 80% V_{DD}, 3.5V = 70% V_{DD}, 1.5V = 30% V_{DD}, 1.0V = 20% V_{DD}.
9. Analogue Voltage Levels used in this Data Sheet: 0dBm0 = 489mVrms = - 4dBm = 0dB. -15dBm0 = 87mVrms. - 20dBm0 = 49mVrms = - 24dBm.

Application Recommendations

Due to the very low levels of signal and idle channel noise required in Military applications – a noisy or badly regulated power supply could cause instability putting the overall system performance out of specification. Adherence to the points noted below will assist in minimizing this problem.

(a) Care should be taken on the design and layout of the printed circuit board.

(b) All external components (as recommended in Figure 3) should be kept close to the package.

(c) Tracks should be kept short, particularly the Encoder Input capacitor and the V_{BIAS} capacitor.

(d) Xtal/clock tracks should be kept well away from analogue inputs and outputs.

(e) Inputs and outputs should be screened wherever possible.

(f) A "ground plane" connected to V_{SS} will assist in eliminating external pick-up on the input and output pins.

(g) It is recommended that the power supply rails have less than 1mVrms of noise allowed.

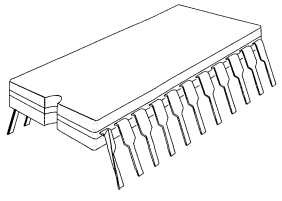
(h) The source impedance to the Encoder Input pin must be less than 100Ω, Output Idle channel noise levels will improve with even lower source impedances.

Package Outlines

The FX629 is available in the package style outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX629J 22-pin cerdip DIL (J3)

NOT TO SCALE



Max. Body Length	27.38mm
Max. Body Width	9.75mm

Handling Precautions

The FX629 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

Ordering Information

FX629J 22-pin cerdip DIL (J3)

Integrated Circuits Data Book

Section 5

Cordless Telephone

CML Semiconductor Products
PRODUCT INFORMATION

FX118 Duplex Frequency Inverter for Cordless Telephones

Publication D/118/3 July 1994

Features/Applications

- **Frequency Inversion Scrambling**
- **Full-Duplex Operation**
- **High Baseband and Carrier Rejection**
- **Audio Lowpass and Bandpass Filtering On-Chip**
- **Xtal Oscillator Stabilty**
- **Low Power Requirement** *(3.0 Volt Minimum)*
- **Cordless Telephones**
- **Base and Handheld Applications**
- **Input Gain Adjustment**
- **Plastic DIL and S.O.I.C. Package Styles**

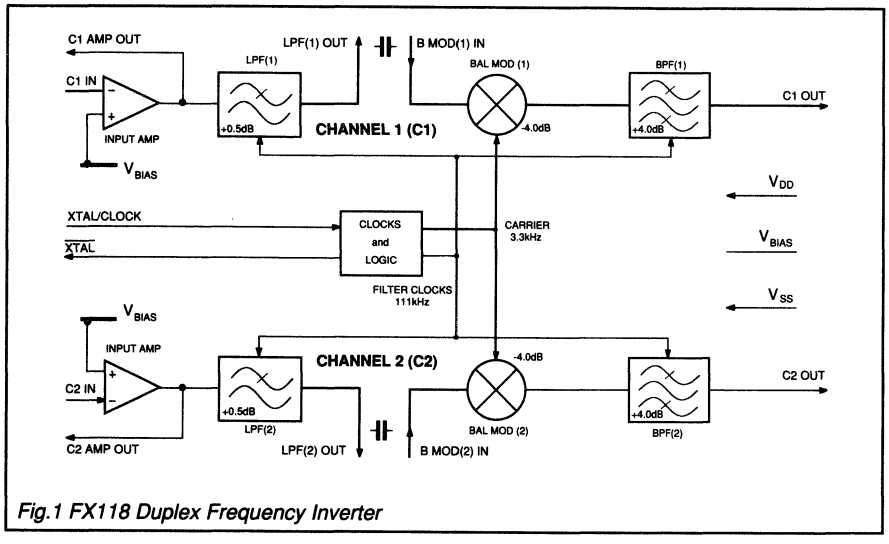


Fig.1 FX118 Duplex Frequency Inverter

FX118

Brief Description

The FX118 is a low-power, full-duplex frequency inverter available to provide voice privacy for cordless telephone systems by mixing the incoming audio with an internally produced carrier frequency (3.3kHz).

This chip contains two completely separate audio channels (C1 and C2) each comprising a "component-adjustable" input amplifier, a 10th-order lowpass filter, a balanced modulator and a 14th-order bandpass filter output.

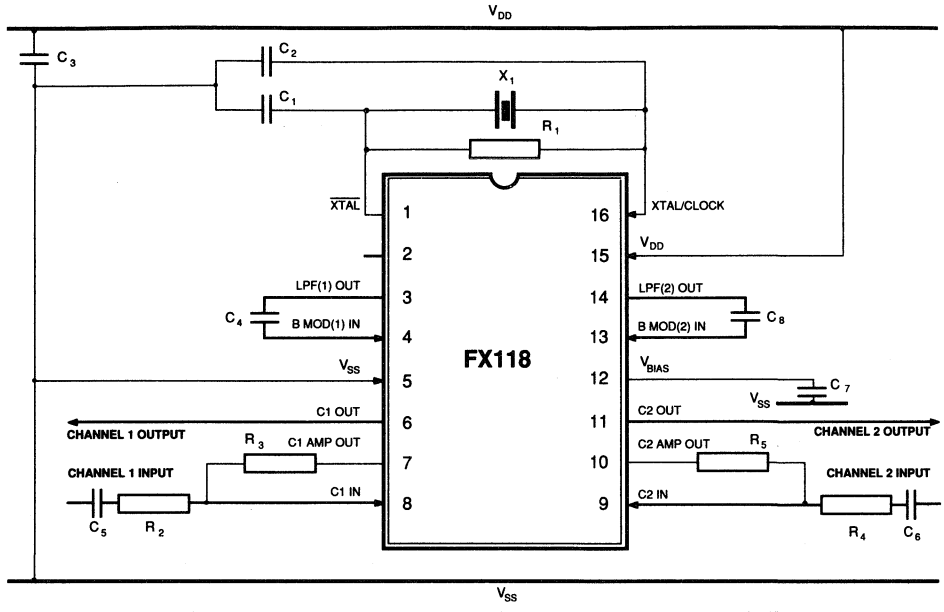
The on-chip modulation process has the properties of high baseband and carrier frequency rejection which when combined with high-order output filtering, produces a high-quality recovered voiceband audio.

The frequency stability of the FX118 is achieved by an on-chip oscillator employing an external 4.433619MHz Xtal or clock input to produce the common carrier frequency and the sampling clocks for the switched capacitor low and bandpass filters.

This microcircuit has a low power requirement of 3.0 volts (min.) and is encapsulated in either 16-pin DIL or small outline SMD (S.O.I.C.) plastic packages both of which are of a physical size suitable for either base or handset type telephone instruments as well as battery-portable and mobile communications systems.

Pin Number FX118DW FX118P	Function
1	**$\overline{\text{Xtal}}$:** Output of clock oscillator inverter.
2	No Internal Connection: It is recommended that, to improve noise conditions, this pin is connected to V_{SS}.
3	**LPF(1) Out:** The output of the Channel 1 Lowpass Filter. It is to be coupled to "B Mod(1) In" via a 1.0µF capacitor – see Figure 2.
4	**B Mod(1) In:** The input to Channel 1 balanced modulator. Internally biased at $V_{DD}/2$ it is to be coupled to "LPF(1)" via a 1.0µF capacitor – see Figure 2.
5	**V_{SS}:** Negative supply (GND).
6	**C1 Out:** The analogue output of Channel 1.
7	**C1 Amp Output:** Channel 1 amplifier with external components (see Figure 2) can be used to provide gain in the signal path.
8	**C1 In:** The negative input of Channel 1 Amplifier. Recommended external components are shown in Figure 2.
9	**C2 In:** The negative input of Channel 2 Amplifier. Recommended external components are shown in Figure 2.
10	**C2 Amp Output:** Channel 2 amplifier with external components (see Figure 2) can be used to provide gain in the signal path.
11	**C2 Out:** The analogue output of Channel 2.
12	**V_{BIAS}:** The internal analogue bias line at $V_{DD}/2$. It should be decoupled to V_{SS} via a 1.0µF or greater capacitor. See Figure 2.
13	**B Mod(2) In:** The input to Channel 2 balanced modulator. Internally biased at $V_{DD}/2$ it is to be coupled to "LPF(2)" via a 1.0µF capacitor – see Figure 2.
14	**LPF(2) Out:** The output of the Channel 2 Lowpass Filter. It is to be coupled to "B Mod(2) In" via a 1.0µF capacitor – see Figure 2.
15	**V_{DD}:** The positive supply rail. A single positive supply voltage (3.0v – 5.0v) is required. Levels and voltages within the Duplex Frequency Inverter are dependent upon this supply.
16	**Xtal/Clock:** 4.433619 MHz Xtal or externally derived clock is injected at this pin. See Figure 2. Operation of the FX118 without a Xtal or clock input may cause device damage.

Application Information



Component		Value						
R_1	=	1.0MΩ	C_2	=	33pF	C_7	=	1.0µF
$R_2 R_3 C_5$		See Note	C_3		0.47µF	C_8		1.0µF
$R_4 R_5 C_6$		See Note	C_4		1.0µF	X_1		4.433619MHz
C_1		47pF						

Tolerances *C = ±20% R = ±10%*

NOTES 1. Configurations R_2, R_3, C_5 and R_4, R_5, C_6 should be chosen with respect to the specific application.
2. Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail (V_{DD}) is fitted with a current limiting device (resistor or fast-reaction fuse).

Fig.2 Recommended External Components

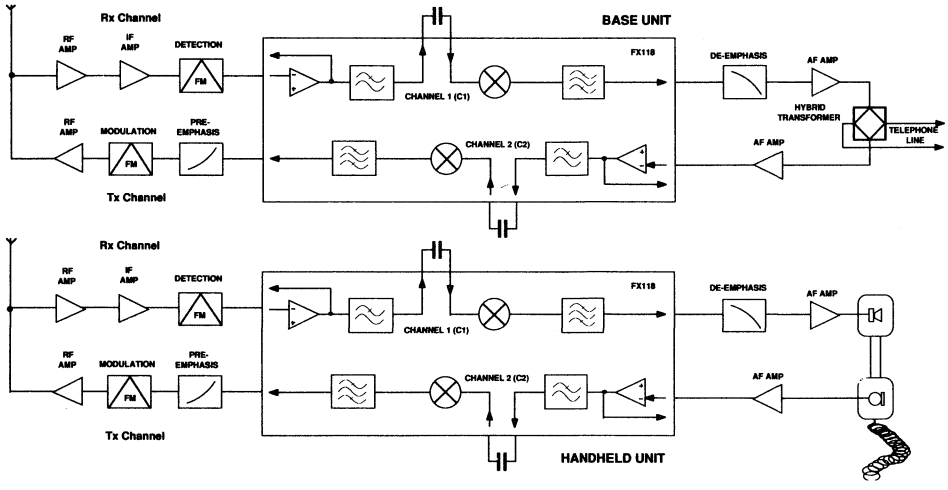


Fig.3 Example of the FX118 Employed in a Cordless Telephone Application

Application Information .....

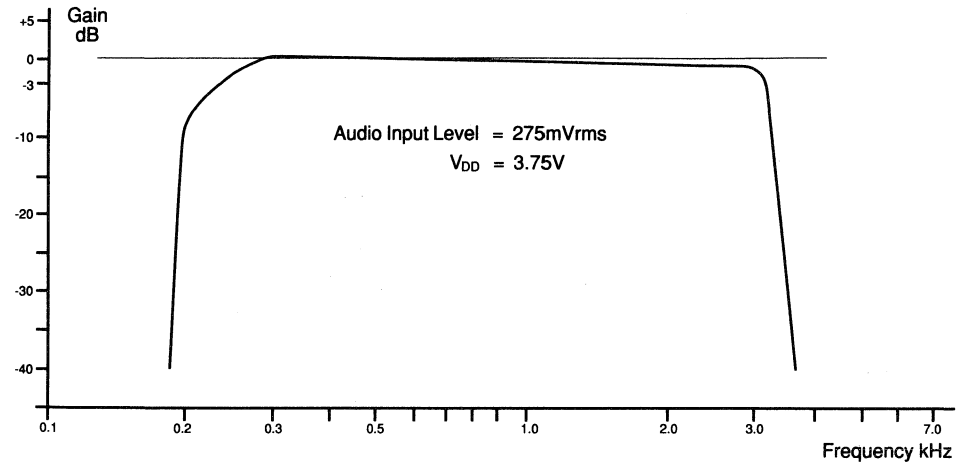


Fig.4 Typical Audio Frequency Response of a Single Scrambled or De-scrambled Channel

System Gains

When calculating the external components for the operation of the FX118 the following points should be considered:

(a) The Input Lowpass Filter has a (typical) gain of 0.5dB.

(b) The Balanced Modulator has a (typical) attenuation of 4.0dB.

(c) The Output Bandpass Filter has a (typical) gain of 4.5dB.

How the Inverter Works

Carrier Frequency *minus* Input Voice Frequency *equals* Scrambled Voice Frequency

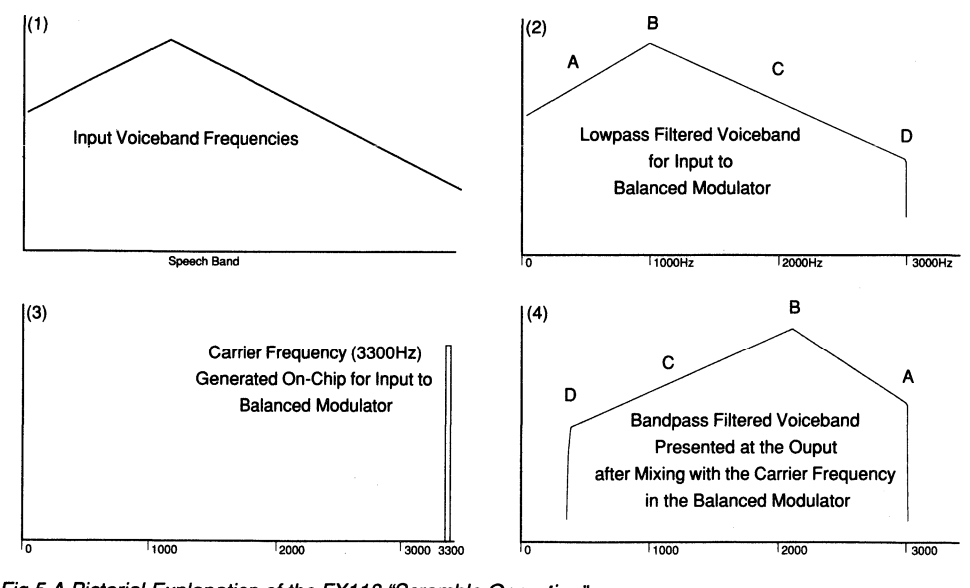


Fig.5 A Pictorial Explanation of the FX118 "Scramble Operation"

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX118DW/P**	-40°C to +85°C
Storage temperature range:	**FX118DW/P**	-40°C to +85°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 3.75V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.433619MHz. Audio level 0dB ref: = 388mV rms @ 1.0kHz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		3.0	3.75	5.5	V
Supply Current		–	4.0	6.0	mA
Input Impedance (Amplifiers)		1.0	10.0	–	MΩ
Output Impedance (LP Filters)		–	2.0	–	kΩ
Output Impedance (C1, C2)		–	200	–	Ω
Output Impedance (C1, C2 Amps)		–	10.0	–	kΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}		–	10.0	–	kΩ
Inverter Gain		–	10.0	–	V/V
Gain/Bandwidth Product		–	10.0	–	MHz
Dynamic Values					
Analogue Signal Input Levels		-16.0	–	4.0	dB
SINAD	6	–	30.0	–	dB
Unwanted Modulation Products	1, 2	–	-40.0	–	dB
Carrier Breakthrough	1, 2	–	-55.0	–	dB
Baseband Breakthrough	1, 2	–	-40.0	–	dB
Carrier Frequency		–	3299	–	Hz
Analogue Output Noise	3	–	-42.0	–	dB
Analogue Output Noise	5	–	-46.0	–	dBp
Filters					
Input Lowpass Filter	1				
Cut-Off Frequency (-3dB)		–	3100	–	Hz
Passband Ripple (300Hz - 3kHz)		–	±1.0	–	dB
Attenuation at 3.3kHz		–	30.0	–	dB
Attenuation at 3.6kHz		–	45.0	–	dB
Passband Gain		–	0.5	–	dB
Output Bandpass Filter	**1, 4**				
Passband Frequencies		300	–	3000	Hz
Passband Ripple		–	±1.0	–	dB
Low Freq. Roll-Off <200Hz		12.0	–	–	dB/oct.
High Freq. – Attenuation at 3.4kHz		–	48.0	–	dB
Passband Gain		3.5	4.5	5.5	dB
Overall Modulated and De-Modulated Channel Response					
Passband Frequencies (Tx and Rx Channel)		300	–	3000	Hz
Passband Ripple		-3.0	–	2.0	dB
Low Freq. Roll-Off <250Hz		18.0	–	–	dB/oct.
High Freq. – Attenuation at 3.4kHz		–	48.0	–	dB
Passband Gain	4	–	0.5	–	dB
Distortion	1	–	3.0	–	%

Notes:

1. Measured with an audio input level of -3.0dB.
2. With respect to a single modulated (scrambling) channel.
3. Measured with a short circuit input, at any analogue output, in a 30.0kHz bandwidth.
4. With Input Amplifier gain at 0dB.
5. Measured psophometrically weighted, at any analogue output.
6. Measured in a 30kHz bandwidth.

Package Outlines

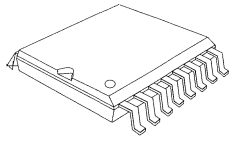
The FX118 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX118 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX118DW 16-pin S.O.I.C. (D4)

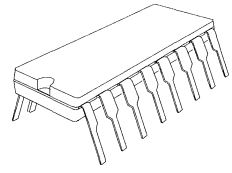
NOT TO SCALE



Max. Body Length 10.31mm
Max. Body Width 7.59mm

FX118P 16-pin plastic DIL (P3)

NOT TO SCALE



Max. Body Length 19.24mm
Max. Body Width 6.41mm

Ordering Information

FX118DW 16-pin S.O.I.C. (D4)

FX118P 16-pin plastic DIL (P3)

Integrated Circuits Data Book

Section 6

Telecoms

CML Semiconductor Products

PRODUCT INFORMATION

FX613 Universal Call Progress Decoder

Publication D/613/2 July 1994
Provisional Issue

Features

- **Covers Worldwide Call Progress Frequencies (300Hz to 2,150Hz)**
- **3 Volt <1mA Requirement**
- **Decodes Single or Modulated Tones**
- **Analogue In/Serial Data Out**
- **Speech Discrimination Ability**
- **µProcessor Compatible Outputs**
- **Telephone/Telecoms, Radio and Fax/Modem Applications**
- **Mixed Analogue/Digital Technology**

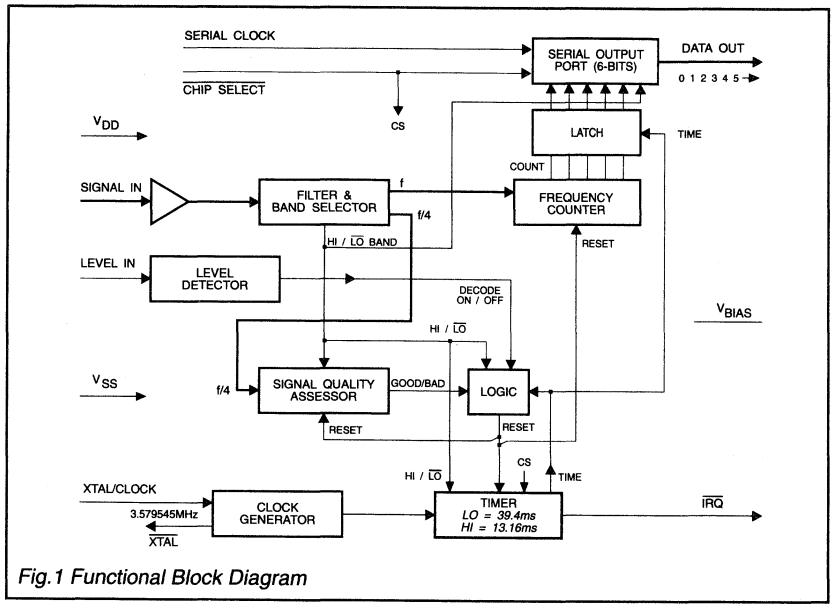


Fig.1 Functional Block Diagram

FX613

Brief Description

The FX613 is a wide-band, 'N-Tone', non-predictive tone decoder to measure telephone system call progress tones in PABX, Pay/Feature-Phone, Fax and Modem systems.

Adhering to Must/Must-Not Decode limits and able to measure inband frequencies in outband modulation, this decoder measures the frequency of input signals in the range 300Hz to 2,150Hz; the result of each measurement is presented to a system µProcessor, as a 6-bit serial word.

The decode frequency range, which covers the World's call progress application spectrum, is processed internally as two bands: LO = 300Hz to 660Hz and HI = 900Hz to 2150Hz. Frequency measurement is achieved by counting the number of cycles in a set time period (LO = 39.47ms or HI = 13.16ms). Bad signal/level quality or NOTONE results in a count-abort, timing-reset and no output from the decoder.

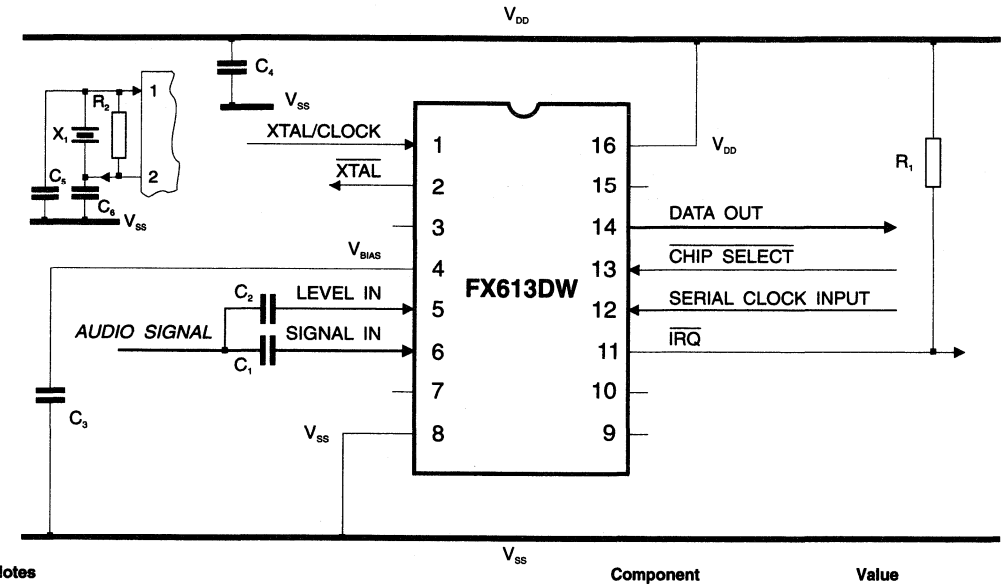
Current frequency information is output for the µProcessor using a Serial Data, Clock and Interrupt interface.

Data from the FX613 should be processed by a µProcessor whose algorithms are able to recognize the frequency, sequence and/or cadence of input signals as national call progress information; e.g.: 'Dial', 'Busy', 'Number-Unobtainable', 'Ringing' and automatic tones employed by Fax, Modem systems. Software can be simply configured to reject speech frequencies.
Due to its 'N-Tone', non-predictive decoding capability, units employing the FX613 can be redeployed under a new national standard by a simple software amendment.

Available in 16-pin plastic S.O.I.C. SMD and 14-pin plastic DIL packages, this low-cost, mixed analogue/digital microcircuit has a typical power requirement of less than 1mA at 3 volts and utilizes a telecom-system clock input of 3.579545MHz to maintain frequency accuracy.

Pin Number		Function
DIL FX611J	Quad FX611LG/LS	
1	1	**Xtal/Clock :** Input to the clock oscillator inverter. A single 4.33619MHz Xtal or external clock pulse is required at this input (see Figure 2).
2	2	**V_{DD} :** The positive supply rail, a single +5-volt supply is required.
3	5	**Detector Input :** "Schmitt Trigger" level detector circuitry, whose input thresholds are set internally. This input must be connected to the Filter Output pin using the external integration components R_7 and C_7, as shown in Figure 2.
4	6	**Amplifier Input (+) :** The positive and negative amplifier inputs. With single or differential inputs the amplifier and its external circuitry are used to provide the gain required to set the device to the user's National Level Specification. The external diodes are used at both inputs (if in use) to provide protection when the line input level exceeds the supply rails (ie above the Absolute Maximum Rating), see Figures 2 and 3.
5	7	**Amplifier Input (–) :**
6	8	**Amplifier Output :** The output of the input stage amplifier and is used with gain setting components as described above (see Figures 2 and 3).
7	11	**Filter Output :** The switched (12kHz/16kHz) bandpass filter output. This output must be connected to the Detector Input pin using the external integration components R_7 and C_7, as shown in Figure 2.
8	12	**V_{SS} :** The negative supply rail, (GND).
9	13	**V_{BIAS} :** The analogue bias point, requires to be externally decoupled to V_{SS} via capacitor C_3.
10	14	**Space Length Time :** Active only in the 'SPM Packet' mode, this input, using an external RC network, sets the minimum valid No-Tone (Space) period for the incoming packet. The minimum valid No-Tone length is set using the formula : $t_S = 0.7 (R_9 \times C_5)$. If the 'SPM Packet' mode is not required, these timing components may be omitted. See Figure 2.
11	17	**Pulse Length Time :** Active only in the 'SPM Packet' mode, this input, using an external RC network, sets the minimum valid Tone period for the incoming packet. The minimum valid Tone length is set using the formula : $t_M = 0.7 (R_8 \times C_4)$. If the 'SPM Packet' mode is not required, these timing components may be omitted. See Figure 2.
12	18	**$\overline{\text{Output Reset}}$:** This input is used only in the 'SPM Packet' mode. Once an SPM Packet has been detected and an output generated (logic "0") from this device the output remains set until this input is set to a logic "0" (note the minimum reset period t_{RESET}, shown on Figure 4). This input has an internal 1MΩ pullup resistor.
13	19	**Mode Select :** A control pin to select either the 'Tone Follower' mode or the 'SPM Packet' mode. A logic "1 " selects 'Tone Follower', a logic "0" selects 'SPM Packet'. This input has an internal 1MΩ pullup resistor (Tone Follower).
14	20	**$\overline{\text{Output}}$:** The digital output of the SPM Detector. In the 'Tone Follower' mode, a valid Tone gives a logic "0" and No-Tone gives a logic "1." Tonebursts and tone dropouts of less than 16 cycles are ignored. In the 'SPM Packet' mode, the output is set to a logic "0" when a valid 'packet' is measured. The output remains so until reset by a logic "0" at the Output Reset function, see Figure 4.
15	23	**System Select :** A control pin to set the device to work on either a 12kHz (logic "1") or 16kHz (logic "0") SPM system. This input has an internal 1MΩ pullup resistor (12kHz).
16	24	**$\overline{\text{Xtal}}$:** The output of the clock oscillator inverter, see Figure 2.
	3, 4, 9, 10, 15, 16, 21, 22.	No internal connection. Leave open circuit.

Application Information



Notes

(1) The Xtal/Clock input may be driven from the host telephone system's 3.579545MHz clock; if a Xtal drive is required, the configuration shown INSET is recommended.

(2) The audio signal should be input to both Signal In and Level In pins via separate coupling capacitors. If it is wished to operate the device with disregard to on-chip level thresholds and permanently enable the FX613, the Level In pin should be held at V_{DD}. To disable the FX613 the Level In pin should be held at V_{SS}. Level thresholds are preset internally.

Component	Value
R_1	22.0kΩ
R_2	1.0MΩ
C_1	0.01µF
C_2	0.1µF
C_3	1.0µF
C_4	1.0µF
C_5	33.0pF
C_6	33.0pF
X_1	3.579545MHz

Tolerances: C = ± 20% R = ± 10%

Fig.2 External Component Connections

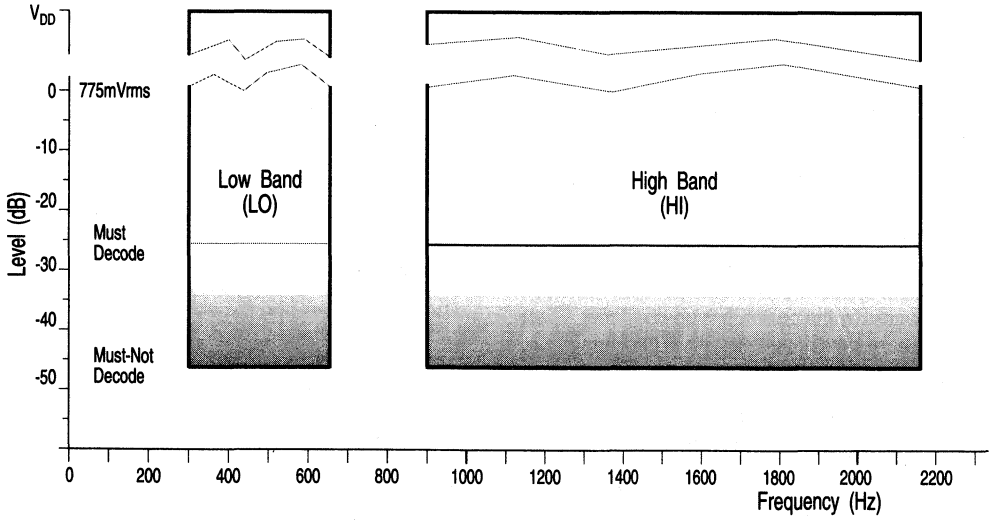


Fig.3 HI/LO Decode Bands

Amplitude and Timing

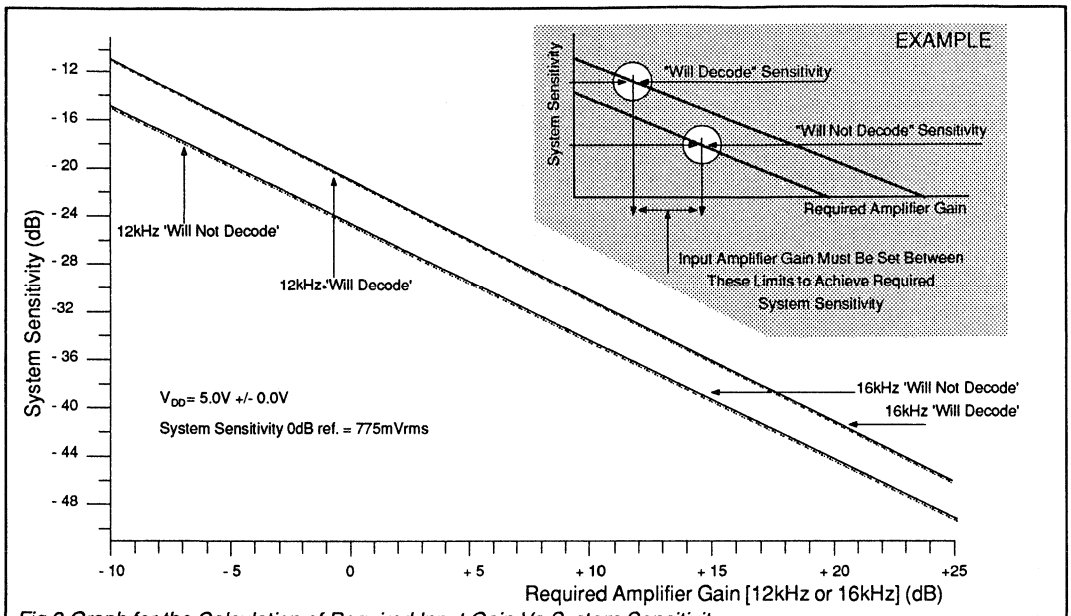


Fig.3 Graph for the Calculation of Required Input Gain Vs System Sensitivity

Input Gain Calculation

Apply the system 'Will' and 'Will-Not' Decode sensitivity values ('Y' axis) to the relevant graph in Figure 3. The 'X' axis indicates the input gain area required.

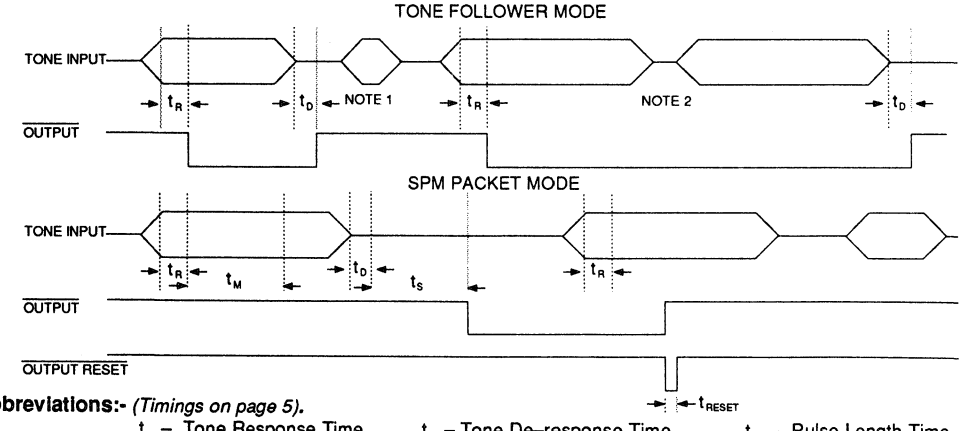
Gain is calculated as :–

$$\frac{Z_{feedback}}{Z_{input}} = \frac{R_6 // X(C_8)}{R_4 + R_5 + X(C_2)}$$

and

$R_3 = R_6$
$R_1 = R_4$
$R_2 = R_5$ — if the differential amplifier is used.
$C_9 = C_8$
$C_1 = C_2$

Input resistor, $R_{protect}$ (R_1 or R_4) is intended to prevent the amplifier input pins going beyond the supply rail voltages, therefore when calculating the input gain the value of $R_{protect}$ must be greater or equal to 0.15 $R_{feedback}$ (R_3 or R_6).
It is recommended that the input time constant is set as a highpass value between audio and the SPM tone frequencies, with C_1 or C_2 being calculated with input resistors to achieve both time and gain requirements.



Abbreviations:- *(Timings on page 5).*

t_R – Tone Response Time
t_D – Tone De–response Time
t_M – Pulse Length Time
t_S – Space Length Time
t_{RESET} – SPM Output Reset Time

Note 1 – No reaction to pulses with periods less than 'Tone Response Time'.
Note 2 – No reaction to drop-outs with periods of less than 'Tone De-response Time'.

Fig.4 Timing Information

Application Information .....

N = int (Frequency x Measurement Period)

Measurement Period = 39.47ms for Low Band (300Hz to 660Hz)
= 13.16ms for High Band (900Hz to 2150Hz)

Note: For input frequencies of between 661Hz and 899Hz the FX613 will give no reliable output.

Bit 5 Output First	Band Bit (5)	MSB (4)	(3)	(2)	(1)	LSB (0)	Bits 0 to 4 = N
	HI-"1"/LO-"0"	Bits 0 to 4 represent the measured frequency in the selected band					

When a 'correct' decode has been allowed and an interrupt generated, a 6-bit data word will be presented at the Serial Output Port. This 6-bit word indicates the input frequency's band and value as described above.

As an example, the following binary-word presented at the Serial Output Port **(1 1 0 1 1 0)** will indicate a frequency in the **HI Band** of between **1680Hz** and **1740Hz (Bit-5 = "1" = HI, 'N' = 22)**.

LO Band	HI Band	N	B_5	B_4	B_3	B_2	B_1	B_0	LO Band	HI Band	N	B_5	B_4	B_3	B_2	B_1	B_0
280	*840*	11	H/L	0	1	0	1	1	505	1515	19	H/L	1	0	0	1	1
285	*855*	11							510	1530	20	H/L	1	0	1	0	0
290	*870*	11							515	1545	20						
295	885	11							520	1560	20						
300	900	11							525	1575	20						
305	915	12	H/L	0	1	1	0	0	530	1590	20						
310	930	12							535	1605	21	H/L	1	0	1	0	1
315	945	12							540	1620	21						
320	960	12							545	1635	21						
325	975	12							550	1650	21						
330	990	13	H/L	0	1	1	0	1	555	1665	21						
335	1005	13							560	1680	22	H/L	1	0	1	1	0
340	1020	13							565	1695	22						
345	1035	13							570	1710	22						
350	1050	13							575	1725	22						
355	1065	14	H/L	0	1	1	1	0	580	1740	22						
360	1080	14							585	1755	23	H/L	1	0	1	1	1
365	1095	14							590	1770	23						
370	1110	14							595	1785	23						
375	1125	14							600	1800	23						
380	1140	14							605	1815	23						
385	1155	15	H/L	0	1	1	1	1	610	1830	24	H/L	1	1	0	0	0
390	1170	15							615	1845	24						
395	1185	15							620	1860	24						
400	1200	15							625	1875	24						
405	1215	15							630	1890	24						
410	1230	16	H/L	1	0	0	0	0	635	1905	25	H/L	1	1	0	0	1
415	1245	16							640	1920	25						
420	1260	16							645	1935	25						
425	1275	16							650	1950	25						
430	1290	16							655	1965	25						
435	1305	17	H/L	1	0	0	0	1	660	1980	26	H/L	1	1	0	1	0
440	1320	17							*665*	1995	26						
445	1335	17							*670*	2010	26						
450	1350	17							*675*	2025	26						
455	1365	17							*680*	2040	26						
460	1380	18	H/L	1	0	0	1	0	*685*	2055	27	H/L	1	1	0	1	1
465	1395	18							*690*	2070	27						
470	1410	18							*695*	2085	27						
475	1425	18							*700*	2100	27						
480	1440	18							*705*	2115	27						
485	1455	19	H/L	1	0	0	1	1	*710*	2130	28	H/L	1	1	1	0	0
490	1470	19							*715*	2145	28						
495	1485	19							*720*	2160	28						
500	1500	19							*725*	*2175*	28						

Table 1 Decode Frequency Data

Application Information .....

Decoder Timing

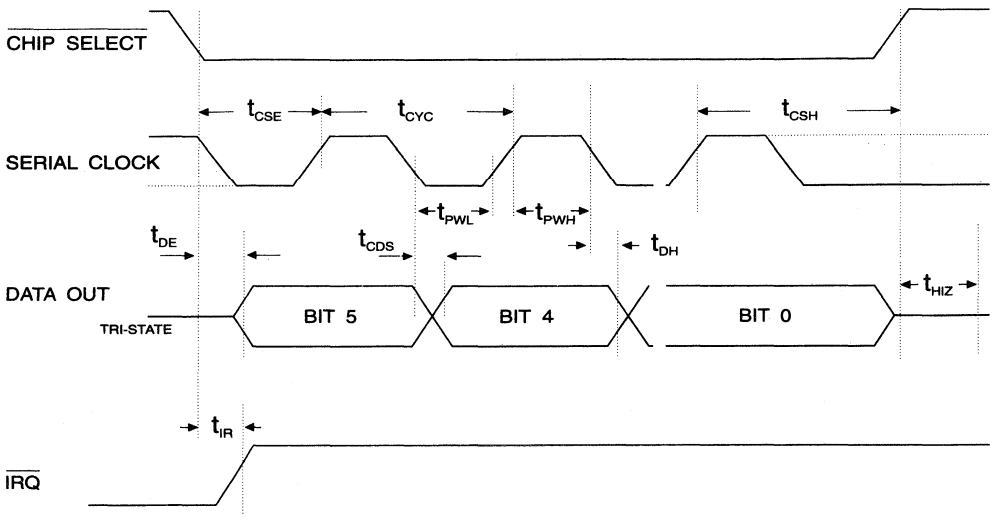


Fig.4 Data-Read Timing

Decoder Timing Characteristics

With reference to Figure 4, *Data-Read Timing.*

	Characteristics	Min.	Typ.	Max.	Unit
t_{PWH}	Serial Clock "High" Pulse Width	250	-	-	ns
t_{PWL}	Serial Clock "Low" Pulse Width	250	-	-	ns
t_{CYC}	Serial Clock-Cycle Time	600	-	-	ns
t_{CSE}	Chip Select Low to Clock "High" Edge	450	-	-	ns
t_{CSH}	Last Clock "High" Edge to CS "High"	600	-	-	ns
t_{DH}	Data Out Hold Time	0	-	-	ns
t_{CDS}	Clock Edge to Data Out Set Time	-	-	200	ns
t_{IR}	Interrupt (IRQ) Reset Time	-	-	200	ns
t_{DE}	Chip Select "Low" to Data Enable	-	-	200	ns
t_{HIZ}	Chip Select "High" to Output Tri-State	-	-	1000	ns

Notes

1 Data is output bit 5 first. Bit 5 can be clocked into the µProcessor by the first Serial Clock rising edge. If 8 Serial Clock pulses are employed the last 2 data-bits will be "0" and should be ignored by the software.

2 Chip Select should be used to react to Interrupts and then returned to a logic "1". If Chip Select stays low there will be no further Interrupts and no Data Output update.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Storage temperature range: **FX613DW/P**	-40°C to +85°C (plastic)

Operating Limits	**Min.**	**Max.**	**Unit**	
Supply Voltage (V_{DD})	3.0	5.5	V	at 25°C
Operating Temperature	-40	+85	°C	

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 3.3V, T_{OP} = -40 to +85 °C. Audio Level 0dB ref: = 775mVrms. Xtal/Clock Frequency = 3.579545MHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Current		-	0.3	1.0	mA
Input Logic "1"		70.0	-	100	% V_{DD}
Input Logic "0"		0	-	30.0	% V_{DD}
Output Logic "1"	1	90.0	-	100	% V_{DD}
Output Logic "0"	1	-	-	10.0	% V_{DD}
Impedances					
Chip Select and Serial Clock Input		10.0	-	-	MΩ
Signal Input		-	50.0	-	kΩ
Level Input		-	210	-	kΩ
IRQ Output (logic "0")		-	-	500	Ω
Data Output (logic "0")		-	500	-	Ω
(Logic "1")		-	-	2.5	kΩ
Dynamic Values					
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}		-	230	825	kΩ
DC Voltage Gain		25.0	42.0	-	V/V
Bandwidth at Unity Gain		5.0	11.0	-	MHz
Single Tone Operation					
Must-Decode Input Level	2	-25.2	-	-	dB
Must-Not Decode Input Level	2	-	-	-46.0	dB
LO Band Frequency Range	4	300		660	Hz
HI Band Frequency Range	4	900		2150	Hz
Frequency Resolution (Table 1)					
LO Band		-	-	25.0	Hz
HI Band		-	-	75.0	Hz
Input Signal/White-Noise Ratio (HI & LO Bands)		-	18.0	-	dB
Interrupt Rate (LO Band)	3	19.0	-	-	/sec
(HI Band)	3	57.0	-	-	/sec
False Decodes Due to Noise	6	-	1.0	-	/2 secs
Outband modulation level limits for correct decode (f_{IN} = 340Hz to 620Hz)	5	-	-	10.0	%

Notes

1. Into a high-impedance load (>1.0MΩ).
2. Must decode signal above -25.2dB; Must Not decode signal below -46.0dB. If a supply other than 3.3 volts is used, levels will change pro-rata.
3. Under 'Pure Tone' input conditions.
4. For input frequencies of between 661Hz and 899Hz the FX613 will provide no reliable output.
5. With an amplitude modulating frequency of between 16.0Hz and 100Hz.
6. Test noise input = 5.0kHz at 100mVrms

Package Outlines

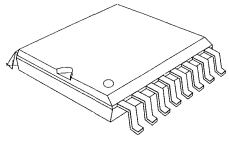
The FX613 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX613 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX613DW 16-pin plastic S.O.I.C. (D4)

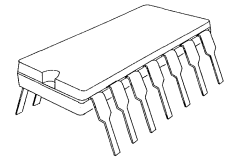
NOT TO SCALE



Max. Body Length 10.31mm
Max. Body Width 7.59mm

FX613P 14-pin plastic DIL (P2)

NOT TO SCALE



Max. Body Length 19.24mm
Max. Body Width 6.41mm

Ordering Information

FX613DW 16-pin plastic S.O.I.C. (D4)

FX613P 14-pin plastic DIL (P2)

CML Semiconductor Products
PRODUCT INFORMATION

FX623 Call Progress Tone Decoder

Publication D/623/3 July 1994
Provisional Issue

Features

- **Measures Call Progress Tone Frequencies ['Busy', 'Dial', 'Fax-Tone' etc.]**
- **Telephone, PABX, Fax and Dial-Up Modem Applications**
- **Low-Power Requirement (600µA at 3.3 Volts$_{TYP}$) for Line-Powered Applications**
- **Custom Tone Decoder [13 Call-Progress Frequencies Recognized]**
- **Operates to a 3.579545MHz Telephone System Clock**
- **Operates Under Simple Logic or µProcessor System Control**

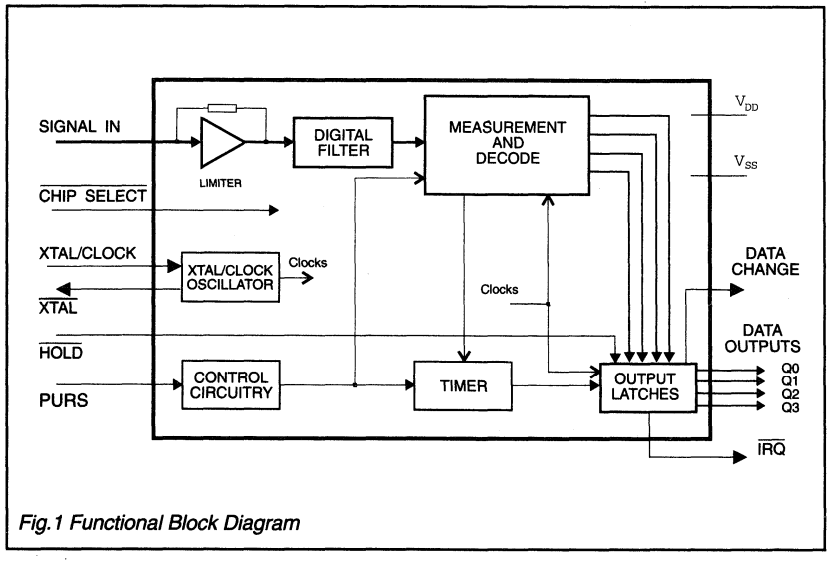


Fig.1 Functional Block Diagram

FX623

Brief Description

The FX623 is a low-power decoding microcircuit that measures the frequency of telephone system call progress tones.

With progress signals input from the telephone line, this single-chip product is programmed to recognize up to thirteen of the World's most commonly used call-progress frequencies, analyze signal quality and present the measured result as a 4-bit parallel data word at the tri-state Data Output.

Using the parallel information from the FX623, the host system suitably configured, can recognize such call progress information as: 'Dial', 'Busy', 'Number Unobtainable', 'Ringing' and Fax/Modem system signals.

This information can then be employed in telephone applications (simple or complex) to control telephone operations. The data output will require a suitable software format to analyze the frequency information from the FX623.

Requiring only a single 3.0$_{[MIN]}$ volt power supply, the FX623 may be line-powered and will operate under simple logic or system µProcessor control using the 'Data-Change, 'Hold' and 'Chip-Select' functions.

The FX623, whose small size and low power consumption makes it ideal for remote applications, requires a 3.579545MHz telephone system clock or Xtal input, is available in a 16-pin plastic DIL package.

Pin Number	Function
FX623P	
1 2 3 4	**Q3:** **Data Outputs:** A 4-bit parallel data word, forming a HEX character representing the **Q2:** decoded tone frequency. This word is output after a successful decode. Table 1 details the **Q1:** Hex character output codes for the relevant decoded tone frequencies. Upon power-up this **Q0:** output is set to 'E_H', but no Data Change pulse generated. These are tri-state outputs.
5	**V_{DD}:** Positive supply rail. A minimum supply voltage of 3.0 volts is required. Levels and voltages within this decoder are dependent upon this supply.
6	**Signal In:** The composite audio input. Signals to this pin should be a.c. coupled. The d.c. bias of the limiter section is set internally; this pin should not be loaded with any other circuitry.
7	No internal connection. Leave open circuit.
8	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter.
9	No internal connection. Leave open circuit.
10	**Xtal/Clock:** The input to the clock oscillator inverter. A 3.579545MHz Xtal or externally derived clock should be connected here (see Figure 2).
11	**V_{SS}:** Negative supply rail (GND).
12	**$\overline{\text{Hold}}$:** An input to control the Output Latch condition; employed in combination with the Data Change output to facilitate, if required, Interrupt and/or handshake operations with a µProcessor. With Hold placed "Low", with a tone input, the Data Change output will be held "High" at the next data change, and the current output code is locked in the Output Latches regardless of any changes to the input signal. The output code remains as held until this input is returned "High" (see Figure 3). Whilst this input is "High" the output data, Q0 - Q3, cycles normally with the input audio. This pin has an internal 1.0MΩ pullup resistor.
13	**PURS:** Power-Up ReSet. To reset internal circuitry at power-up; a logic "1" level is required at this pin for a duration of at least 2.5mS after the Xtal/Clock input and full V_{DD} levels are applied. The component configuration shown in Figure 2 is recommended; for slow-rising power supplies the time constant of components should be increased accordingly.
14	**$\overline{\text{IRQ}}$:** Interrupt Request. An output for µProcessor operation; normally "High" this output is latched "Low" when an internal data change occurs if the Chip Select input is "High". This output is reset ("High") the when Chip Select line is taken "Low". To permit "wire-OR" connection with other peripherals, this output has a low-impedance when "Low" and a high-impedance when "High".
15	**$\overline{\text{CS}}$:** Chip Select- A controlling function. When held "High" the Data Outputs Q0, Q1, Q2 and Q3 and the Data Change output are disabled. When taken "Low" the Data Outputs Q0, Q1, Q2 and Q3 and the Data Change output are enabled; the Interrupt Request (IRQ) is reset ("High") when CS is taken "Low". See Figures 3 and 4.
16	**Data Change:** A positive-going pulse is generated at this output when the data changes (Tone or NOTONE). New tone-data is presented to the Q0, Q1, Q2 and Q3 Data Outputs if the Hold input is set "High". This is a tri-state output.

Application Information

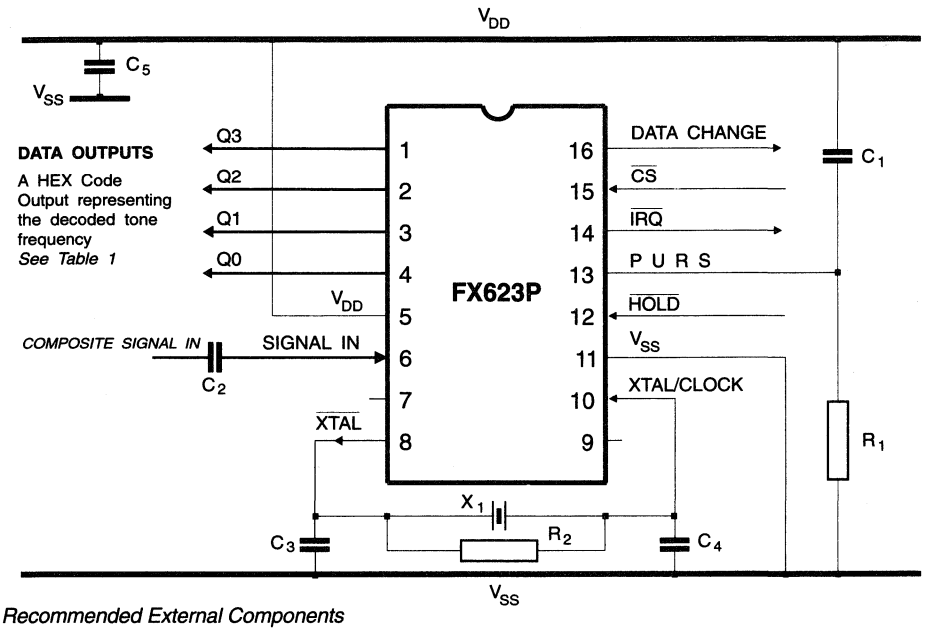


Fig.2 Recommended External Components

Hex Character	Output Code Q3	Q2	Q1	Q0	Band Edges (Hz) Lower Edge	Upper Edge	Nominal Centre Freq.
0	0	0	0	0	364	386	*375*
1	0	0	0	1	488	520	*500*
2	0	0	1	0	520	580	*550*
3	0	0	1	1	580	618	*600*
4	0	1	0	0	386	412	*400*
5	0	1	0	1	412	436	*425*
6	0	1	1	0	436	463	*450*
7	0	1	1	1	463	487	*475*
8	1	0	0	0	900	1008	*950*
9	1	0	0	1	1273	1325	*1300*
A	1	0	1	0	1350	1455	*1400*
B	1	0	1	1	1750	1855	*1800*
C	1	1	0	0	2062	2140	*2100*
D	1	1	0	1	frequency not guaranteed		
E	1	1	1	0	frequency not guaranteed		
F	1	1	1	1	NOTONE		

Table 1 Tone Decode Frequencies

Component	Value
R_1	1.0MΩ
R_2	1.0MΩ
C_1	47.0nF
C_2	4.7nF
C_3	33.0pF
C_4	33.0pF
C_5	1.0µF
X_1	3.579545MHz
Tolerances R = ±10%	*C = ±20%*

Timing Information

With CS Low - Figure 3.

After initial power-up and the Hold input inactive (High), as frequencies are input, with the Data Change output as an active (High) indicator, the data is presented at the Data Outputs.

If/when the Hold input is placed active (Low), the data at the Data Outputs is frozen and the Data Change output held High at its next active excursion -until the Hold input is returned High.

With the Hold input held High - Figure 4.

As frequencies are input a correct decode will produce an active (Low) interrupt level.

This interrupt (IRQ) is serviced and reset by an active (Low) CS input.

Note the 'valid data' period at the Data Outputs.

Application Information
Decoder Timing

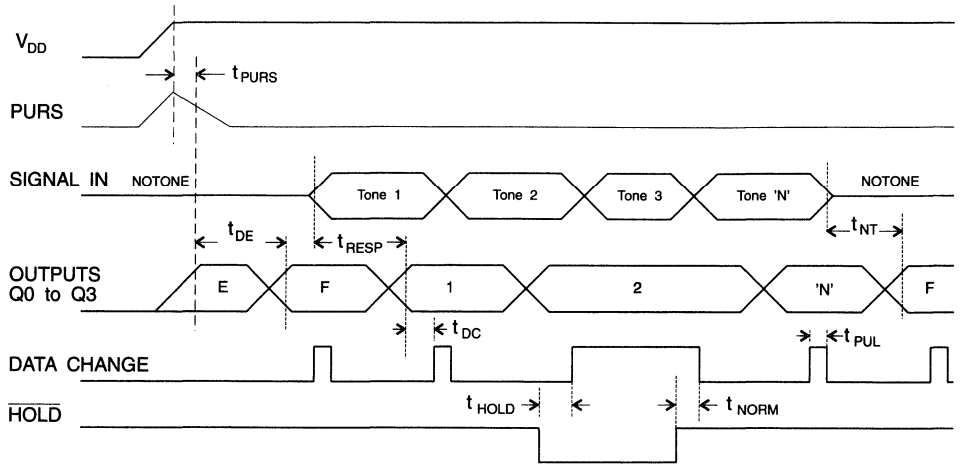


Fig.3 Timing with the Chip Select Input Held "Low"; CS and IRQ are not used

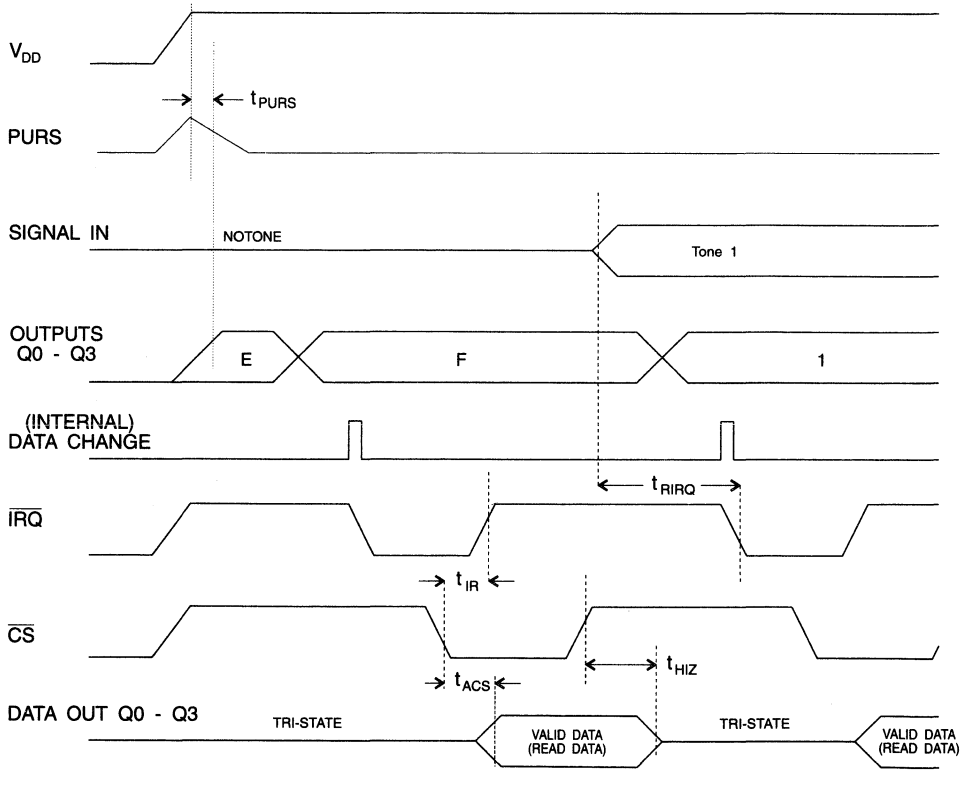


Fig.4 Timing with the HOLD Input Held "High"; CS and IRQ are used

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Storage temperature range: **FX623P**	-40°C to +85°C (plastic)

Operating Limits	**Min.**	**Max.**	**Unit**	
Supply Voltage (V_{DD})	3.0	5.5	V	at 25°C
Operating Temperature	-40	+85	°C	

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 3.3V, T_{OP} = -40 to +85 °C. Audio Level 0dB ref: = 775mVrms. Xtal/Clock Frequency = 3.579545MHz

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Current			-	0.6	1.0	mA
Input Logic "1"			0.7	-	-	$\%V_{DD}$
Input Logic "0"			-	-	0.3	$\%V_{DD}$
Output Logic "1"			0.8	-	-	$\%V_{DD}$
Output Logic "0"			-	-	0.2	$\%V_{DD}$
Impedance						
CS and PURS Input			10.0	-	-	MΩ
Hold Input		1	0.5	-	-	MΩ
Signal Input			0.1	-	-	MΩ
IRQ Output (logic "1")			-	30.0	100	kΩ
IRQ Output (logic "0")			-	175	500	Ω
Q0 - Q3 & Data-Change Outputs (logic "1")			-	0.7	2.0	kΩ
Q0 - Q3 & Data-Change Outputs (logic "0")			-	175	500	Ω
Q0 - Q3 & Data-Change Outputs (high Z)			1.0	-	-	MΩ
Dynamic Values						
Signal Input Range		2, 5	35.0		1,166	mVrms
Decode Bandedge Tolerance		3	-1.0	-	1.0	%
Xtal Inverter						
Voltage Gain			20.0	-	-	V/V
Input Impedance			10.0	-	-	MΩ
Output Impedance			-	-	160	kΩ
Decoder Timing - *Figures 3 and 4*						
Power Up Reset Time	t_{PURS}		2.5	-	-	ms
Data 'E' Time	t_{DE}		31.0	-	-	ms
NOTONE to Tone Response Time	t_{RESP}	4	-	27.0	50.0	ms
Tone to NOTONE Response Time	t_{NT}	4	-	-	60.0	ms
Data to Data-Change Pulse Time	t_{DC}		0.625	-	1.15	ms
Data-Change Pulse Width	t_{PUL}		-	1.25	-	ms
Hold to Data-Change Rise Time	t_{HOLD}		63.0	-	-	µs
HOLD to Data-Change Fall Time	t_{NORM}		-	-	150	µs
IRQ Tone Response Time	t_{RIRQ}		-	29.0	52.0	ms
IRQ Reset Time	t_{IR}		-	-	250	ns
Data Access Time	t_{ACS}		-	-	250	ns
CS High to Output Tri-State Time	t_{HIZ}		-	-	100	ns

Notes

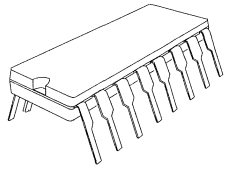
1. This pin has an on-chip 1.0MΩ pullup resistor.
2. An a.c. coupled sine or squarewave.
3. See Table 1, Tone Decode Frequencies.
4. Delay between the change of input (Tone/NOTONE) and the change at the Q0 - Q3 outputs.
5. The signal input maximum value is determined by the formula $V_{DD}/2.83$.

Package Outlines

The FX623 is available in the package style outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX623P 16-pin plastic DIL (P3)

NOT TO SCALE



Max. Body Length	19.24mm
Max. Body Width	6.41mm

Handling Precautions

The FX623 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

Ordering Information

FX623P 16-pin plastic DIL (P3)

CML Semiconductor Products

PRODUCT INFORMATION

FX631 Low-Voltage SPM Detector

Publication D/631/3 July 1994
Provisional Issue

Features

- **Detects 12kHz and 16kHz SPM Frequencies**
- **Low Power (3.0 Volt$_{MIN}$ <1.0mA) Operation**
- **High Speechband Rejection Properties**
- **Tone-Follower and Packet Mode Outputs**
- **Applications**
  - **Complex and/or Simple Telephone Systems**
  - **Call-Charge/-Logging Systems**

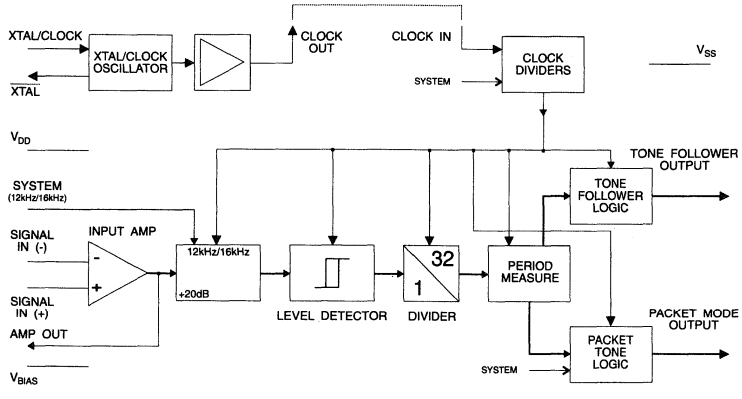


Fig.1 Functional Block Diagram

FX631

Brief Description

The FX631 is a low-power, system-selectable Subscriber Pulse Metering (SPM) detector to indicate the presence, on a telephone line, of both 12kHz and 16kHz telephone call-charge frequencies.

Deriving its input directly from the telephone line, input amplitude/sensitivities are component adjustable to the user's national 'Must/Must-Not Decode' specifications via an on-chip input amplifier, whilst the 12kHz and 16kHz frequency limits are accurately defined by the use of an external 3.579545MHz telephone-system Xtal or clock-pulse input.

The FX631, which demonstrates high 12kHz and 16kHz performance in the presence of both voice and noise, can operate from either a single or differential analogue signal input from which it will produce two individual logic outputs.

1. Tone Follower Output - A 'tone-following' logic output producing a "Low" level for the period of a correct decode and a "High" level for a bad decode or NOTONE.
2. Packet (Cumulative Tone) Mode Output - To respond and de-respond after a cumulative 40ms of good tone (or NOTONE) in any 48ms period.
   This process will ignore small fluctuations or fades of a valid frequency input and is available for µProcessor 'Wake-Up', Minimum tone detection, NOTONE indication or transient avoidance.

This system (12kHz/16kHz) selectable microcircuit, which may be line-powered, is available in 16-pin plastic DIL and small outline surface mount packages.

Pin Number	Function
FX631 DW/P	
1	**Xtal/Clock :** The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the $\overline{\text{Xtal}}$ output (see Figure 2); circuit components are on chip. Using this mode of clock operation, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is employed to the Clock In pin, this pin must be connected directly to V_{DD} (see Figure 2).
2	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter.
3	**Clock Out:** The buffered output of the on-chip clock oscillator inverter. If a Xtal input is employed this output should be connected directly to the Clock In pin.
4	**Clock In:** The 3.579545MHz clock pulse input to the internal clock-dividers. If a clock pulse input is employed, the Xtal/Clock input (Pin 1) should be connected to V_{DD}. See Figure 2.
5	No internal connection, leave open circuit.
6	No internal connection, leave open circuit.
7	**V_{BIAS}:** The output of the on-chip analogue bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} (see Figure 2).
8	**V_{SS}:** Negative supply rail (GND).
9	**Signal In (+):**
10	**Signal In (-):**
11	**Amp Out:**
	The positive and negative signal inputs to, and the output from, the input gain adjusting signal amplifier. Refer to the graph in Figure 4 for guidance on setting level sensitivities to national specifications, and the selection of gain adjusting components.
12	No internal connection, leave open circuit.
13	**Tone Follower Output:** This output provides a logic "0" (Low) for the period of a detected tone, and a logic "1" (High) for NOTONE detection. See Figure 6.
14	**Packet Mode Output:** A logic output that will be available after a cumulation of 40ms of 'good' tone has been received. This packet mode tone follower will only respond when a tone frequency of sufficient quality has been received for sufficient time, i.e. a cumulation of 40ms in any 48ms, short tone bursts or breaks will be ignored. This output provides a logic "0" (Low) for a detected tone and a logic "1" (High) for NOTONE detection. See Figure 6.
15	**System:** The logic input to select device operation to either 12kHz (logic "1" - High) or 16kHz (logic "0" - Low) SPM systems. This input has an internal 1MΩ pullup resistor (12kHz).
16	**V_{DD}:** Positive supply rail. A single, stable power supply is required. Critical levels and voltages within the FX631 are dependant upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin. Note that if this device is 'line' powered, the resulting supply must be stable. See notes on Microcircuit Protection from high and spurious line voltages.

Application Information

External Components

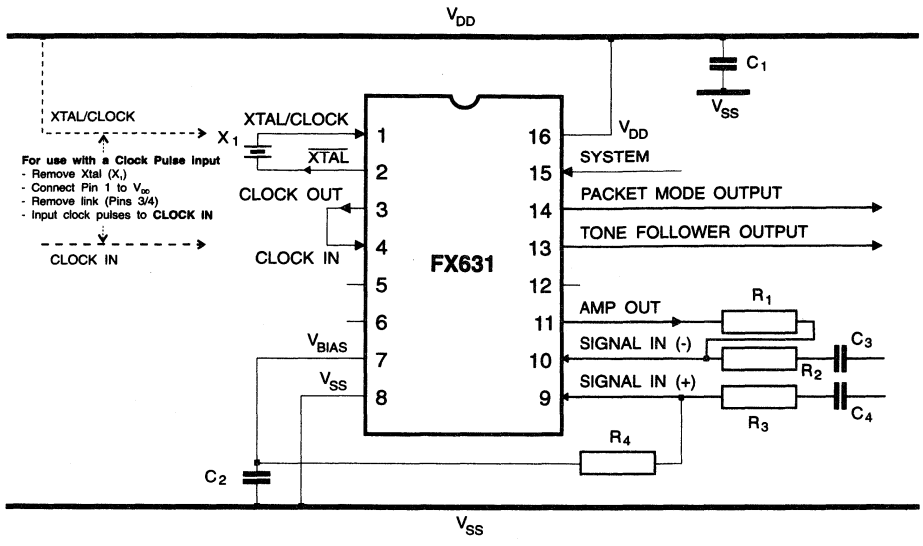


Fig.2 Recommended External Components - Differential Input Mode

Component	Value
R_1	$R_{FEEDBACK}$
R_2	$R_{IN(-)}$
R_3	$R_{IN(+)}$
R_4	R_{BIAS}
C_1	1.0µF ±20%
C_2	1.0µF ±20%
C_3	$C_{IN(-)}$
C_4	$C_{IN(+)}$
X_1	3.579545MHz

External Components

1. The values of the Input Amp gain components illustrated are calculated using the Input Gain Calculation Graph (Figure 4).
   Whilst calculating input gain components, for correct operation, it is recommended that the values of resistors R_1 and R_4 are always greater than, or equal to, 100kΩ.

2. Refer to following pages for advice on Microcircuit Protection from high and spurious line voltages.

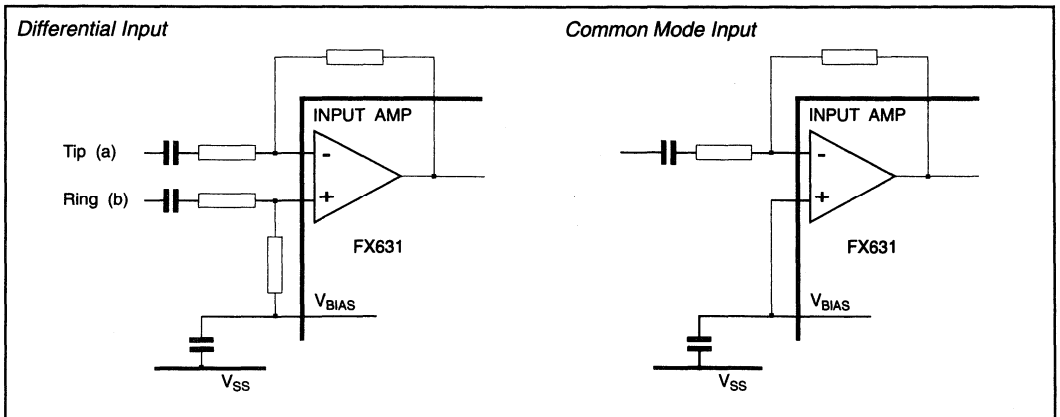


Fig.3 Example Input Configurations

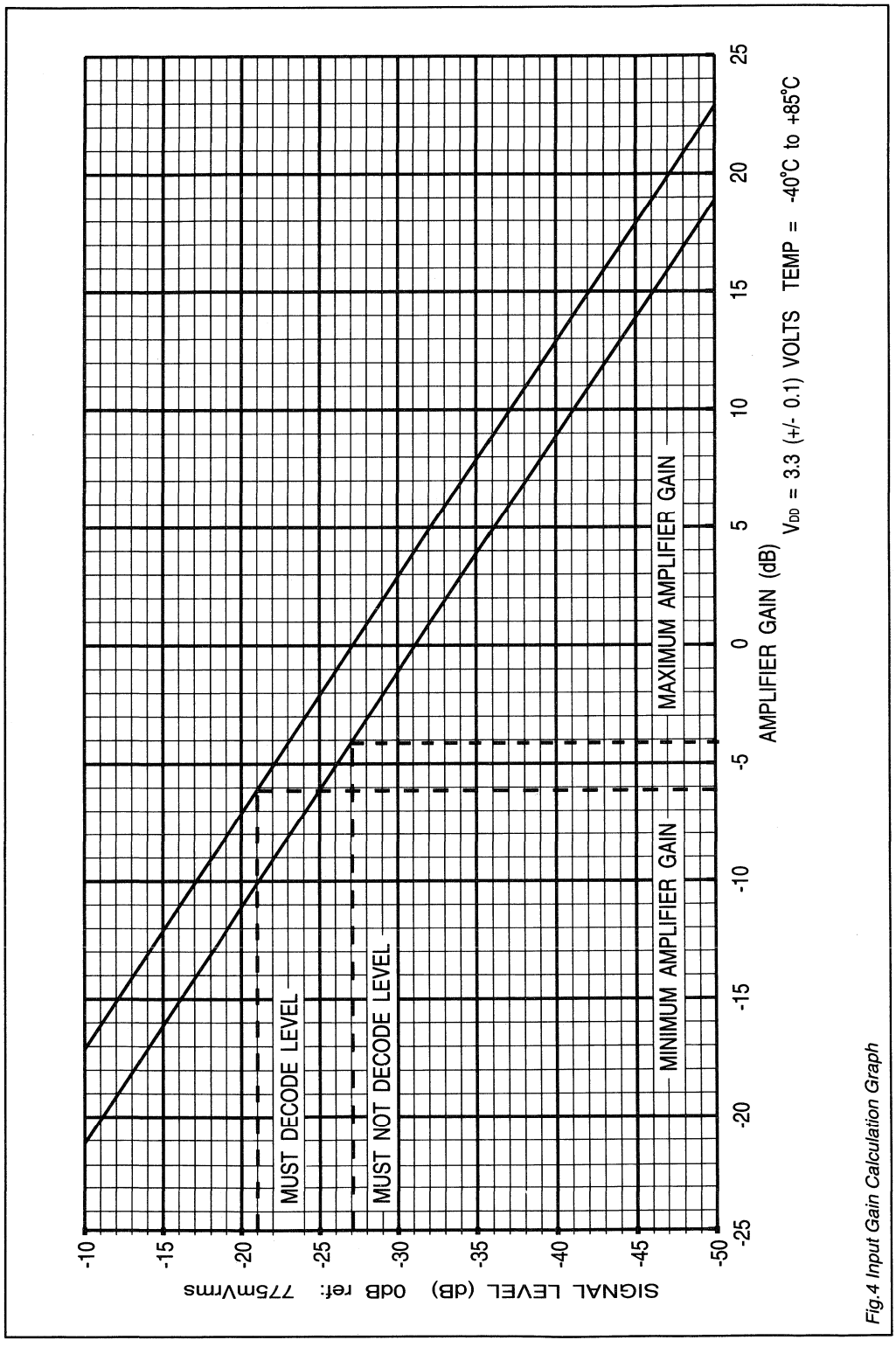


Fig.4 Input Gain Calculation Graph

Application Information .....

Input Gain Calculation

The input amplifier, with its external circuitry, is provided on-chip to set the sensitivity of the FX631 to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels.

With reference to the graph in Figure 4, the following steps will assist in the determination of the required gain/attenuation.

Step 1

Draw two horizontal lines from the Y-axis (Signal Levels (dB)).
The upper line will represent the required 'Must' decode level.
The lower line will represent the required 'Must-Not' decode level.

Step 2

Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis (Amplifier Gain (dB)).
The point where the vertical line meets the X-axis will indicate the MINIMUM Input Amp gain required for reliable decoding of valid signals.

Step 3

Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis.
The point where the vertical line meets the X-axis will indicate the MAXIMUM allowable Input Amp gain.
Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.
Select the gain components as described opposite.

Input Gain Components

With reference to the gain components shown in Figures 2 and 3.

The user should calculate and select external components (R_1, R_2/C_3, R_3/C_4, R_4) to provide an amplifier gain within the limits obtained in Steps 2 and 3.

Component tolerances should not move the gain-figure outside these limits.

It is recommended that the designed gain is near the centre of the calculated range. The graph in Figure 4 is for the calculation of input gain components for an FX631 using a V_{DD} of 3.3 (±0.1) volts.

Use this area to keep a permanent record of your calculated gains and components

Implementation Notes

Aliasing

Due to the switched-capacitor filters employed in the FX631, care should be taken, with the chosen external components, to avoid the effects of alias distortion.

Possible Alias Frequencies:
12kHz Mode = 52kHz
16kHz Mode = 69kHz

If these alias frequencies are liable to cause problems and/or interference, it is recommended that anti-alias capacitors are employed across input resistors R_1 and R_4.

Values of anti-alias capacitors should be chosen so as to provide a highpass cutoff frequency, in conjunction with R_1 (R_4) of approximately 20kHz to 25kHz (12kHz system) or 25kHz to 30kHz (16kHz system).

$$\text{i.e. } C = \frac{1}{2 \times \pi \times f_0 \times R_1}$$

When anti-alias capacitors are used, allowance must be made for reduced gain at the SPM frequency (12kHz or 16kHz).

Microcircuit Protection

Telephone systems may have high d.c. and a.c. voltages present on the line. If the FX631 is part of a host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within V_{DD} + 0.3V and V_{SS} -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the FX631 will require protection diodes at its signal inputs (+ and -). The breakdown voltage of capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the d.c. voltages plus all expected signal peaks.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating Temperature (T_{OP}):	**FX631DW/P**	-40°C to +85°C
Storage temperature range (T_{ST}):	**FX631DW/P**	-40°C to +85°C

Functional Limits .....

	Min.	Max.	Unit	
Supply Voltage (V_{DD})	3.0	5.5	V	at 25°C

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 3.3V T_{OP} = -40 to +85 °C. Audio Level 0dB ref: = 775mVrms. Noise Bandwidth = 50kHz.
Xtal/Clock or 'Clock In' Frequency = 3.579545MHz. 12kHz or 16kHz System Setting.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Current		-	-	1.0	mA
Input Logic "1" (High)		2.3	-	-	V
Input Logic "0" (Low)		-	-	1.0	V
Output Logic "1" (High)		2.9	-	-	V
Output Logic "0" (Low)		-	-	0.4	V
Xtal/Clock or Clock In Frequency		3.558918	–	3.589368	MHz
"High" External Clock Pulse Width		100	-	-	ns
"Low" External Clock Pulse Width		100	-	-	ns
Input Amp					
D.C. Gain		60.0	-	-	dB
Bandwidth (-3dB)		-	100	-	Hz
Input Impedance		-	1.0	-	MΩ
Logic Impedances					
Input (System)		0.7	-	3.8	MΩ
(Clock In)		10.0	-	-	MΩ
Output		-	14.0	30.0	kΩ
Overall Performance					
12kHz Detect Bandwidth	1	11.820		12.180	kHz
12kHz Not-Detect Frequencies (below 12kHz)	1	-	-	11.520	kHz
12kHz Not-Detect Frequencies (above 12kHz)	1	12.480	-	-	kHz
16kHz Detect Bandwidth	1	15.760		16.240	kHz
16kHz Not-Detect Frequencies (below 16kHz)	1	-	-	15.360	kHz
16kHz Not-Detect Frequencies (above 16kHz)	1	16.640	-	-	kHz
Sensitivity	2	7.8	10.0	15.5	mVp-p
Tone Operation Characteristics					
Signal-to-Noise Requirements (Amp Input)	3, 4, 5, 6	22.0	20.0	-	dB
Signal-to-Voice Requirements (Amp Input)	3, 4, 5, 7	-36.0	-40.0	-	dB
Signal-to-Voice Requirements (Amp Output)	5, 6	-25.0	-	-29.0	dB
Tone Follower Output					
Response and De-Response Times	1, 8	-	-	10.0	ms
Packet Mode Output					
Response and De-Response Times	1, 8	40.0	-	48.0	ms

Notes .. ..

Specification .....

Notes

1. With adherence to Signal-to-Voice and Signal-to Noise specifications.
2. With Input Amp gain setting: $15.5dB_{MIN}/18.0dB_{MAX}$.
3. Common Mode SPM and balanced voice signal.
4. Immune to false responses.
5. Immune to false de-responses
6. With SPM and voice signal amplitudes balanced; To avoid false de-responses due to saturation, the peak-to-peak voice+noise level at the output of the Input Amp (12/16kHz Filter Input) should be no greater than the dynamic range of the device.
7. Maximum voice frequencies = 3.4kHz
8. Response, De-Response and Power-up Response Timing.

Application Information .....

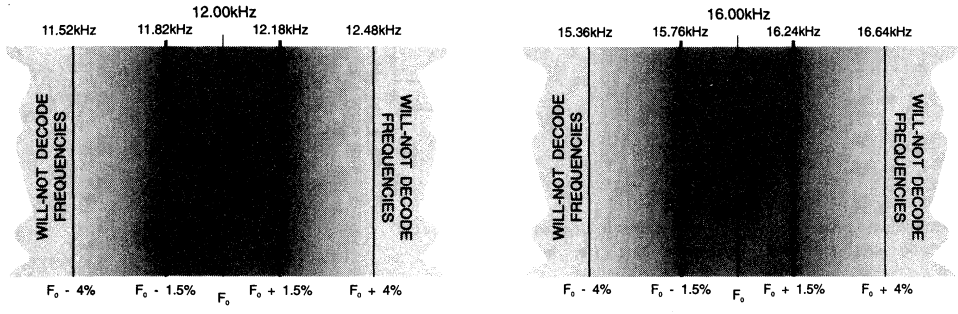


Fig. 5 Will/Will-Not Decode Frequencies

System Timing

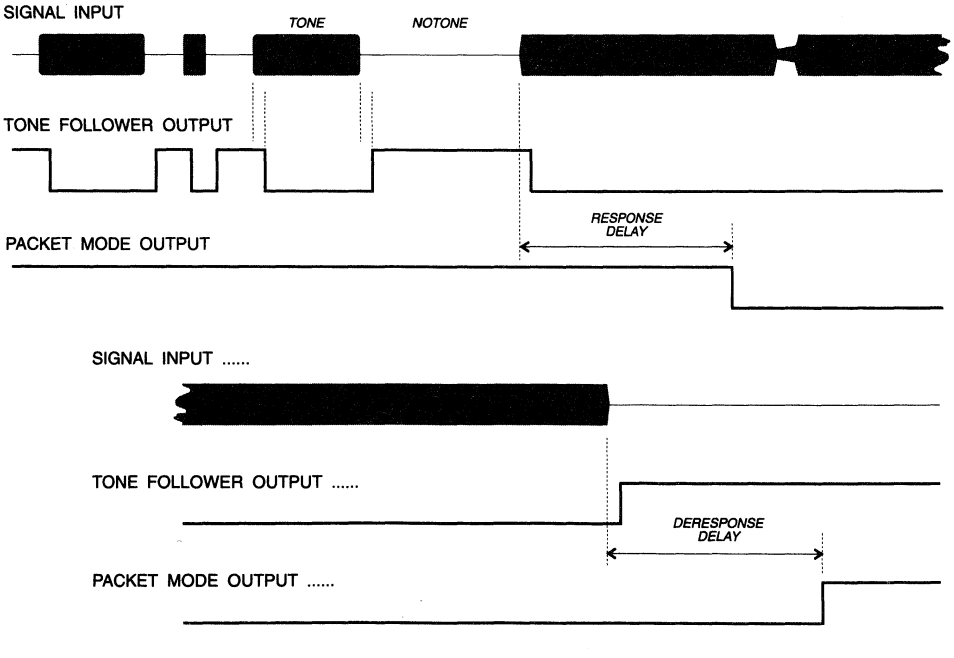


Fig.6 Examples of Input and Output Relationships

Package Outlines

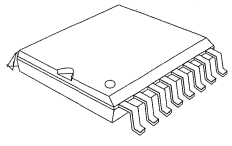
The FX631 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX631 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX631DW 16-pin plastic S.O.I.C. (D4)

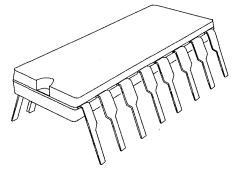
NOT TO SCALE



Max. Body Length 10.31mm
Max. Body Width 7.59mm

FX631P 16-pin plastic DIL (P3)

NOT TO SCALE



Max. Body Length 19.24mm
Max. Body Width 6.41mm

Ordering Information

FX613DW 16-pin plastic S.O.I.C. (D4)

FX613P 16-pin plastic DIL (P3)

CML Semiconductor Products

PRODUCT INFORMATION

FX641 Dual Subscriber Private Metering (SPM) Detector

Publication D/641/2 July 1994
Provisional Issue

Features

- **Two (12kHz/16kHz) SPM Detectors on a Single Chip**
- **Detects 12kHz and 16kHz SPM Frequencies**
- **Xtal Accuracy; Stable Frequency Limits**
- **"Controlled" (µC) and "Fixed" Signal Sensitivity Modes**
- **Selectable Tone Follower or Packet Mode Outputs**
- **High Speech-Band Rejection Properties**
- **"Output Enable" Multiplexing Facility**
- **Call-Charge Applications on PABX Line Cards**

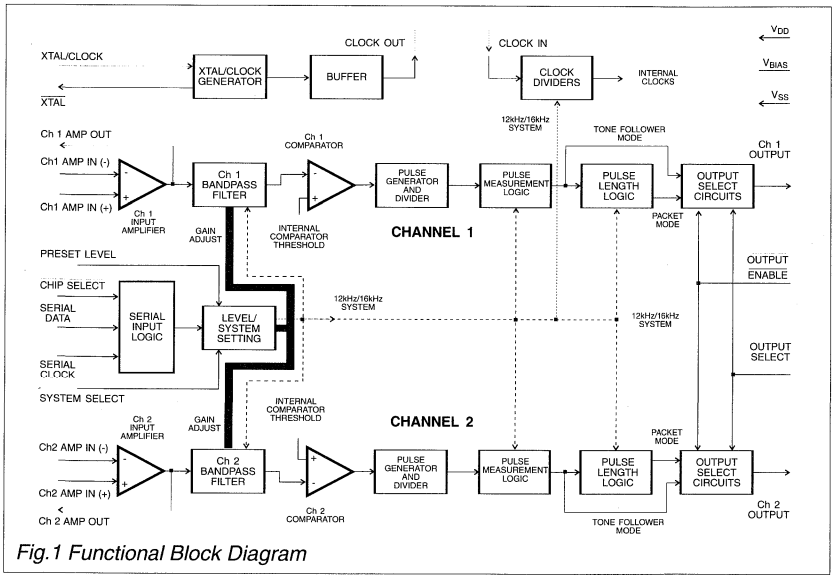


Fig.1 Functional Block Diagram

Brief Description

The FX641 is a low-power, system-selectable Dual Subscriber Private Metering (SPM) Detector *-two detectors on a single chip-* to indicate the presence, on a telephone line, of either 12kHz or 16kHz telephone call-charge frequencies.

Under µProcessor control via a common serial interface, each channel of the FX641 will detect call-charge pulses from a telephone line and provide a digital output for recording, billing or security purposes.

A common set of external components and a stable 3.579545MHz Xtal/clock input ensures that the FX641 adheres accurately to most national "Must and Must-Not" decode band-edges and threshold levels.

The digital output is pin-selectable to one of three modes:

(1) Tone Follower mode -a logic level for the period of a correct decode.

(2) Packet mode -respond/de-respond after a cumulative period of tone or notone in a preset period.

(3) High-impedance output -for device multiplexing.

For non-µProcessor systems a preset sensitivity/system input allows external channel level and system setting.

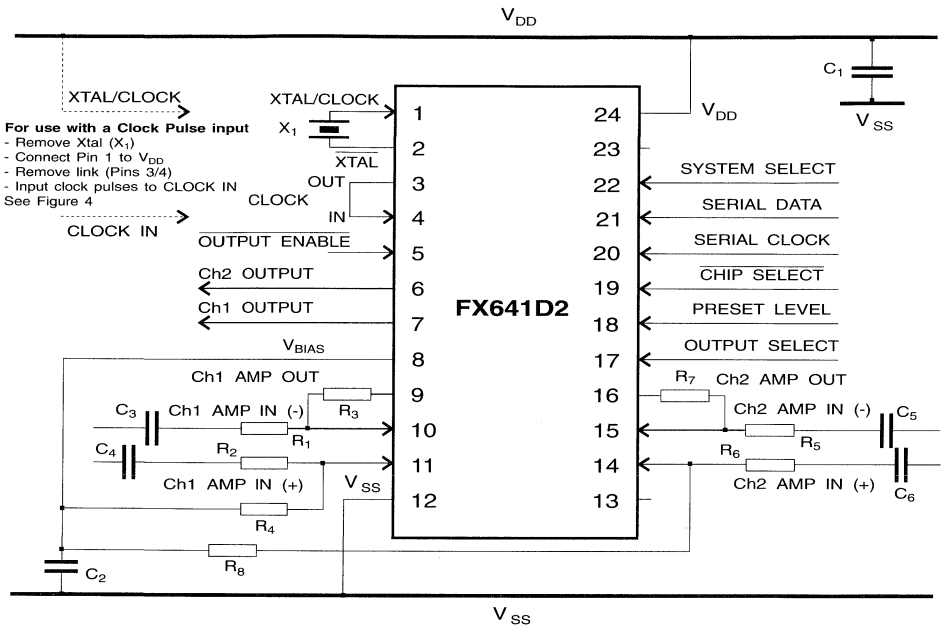
This device, which is suitable for PBX and PABX line-card and remote telephone installations, is available in compact 24-pin plastic DIL and small outline (S.O.I.C.) packages.

The FX641 requires approximately 4.5mA at 5-volts.

Pin Number FX641 D2/P4	Function
1	**Xtal/Clock:** The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the $\overline{\text{Xtal}}$ output; circuit components are on-chip. When using a Xtal input, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is employed to the Clock In pin, this (Xtal/Clock) pin must be connected directly to V_{DD} (see Figure 2). See Figure 4 for details of clock frequency distribution.
2	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter.
3	**Clock Out:** The buffered output of the on-chip-clock oscillator inverter. If a Xtal input is employed, this output should be connected directly to Clock In pin. This output can support up to 3 additional FX641 microcircuits. See Figure 4 for details of clock frequency distribution.
4	**Clock In:** The 3.579545 clock pulse input to the internal clock dividers. If an externally generated clock pulse input is employed, the Xtal/Clock input pin should be connected to V_{DD}.
5	**$\overline{\text{Output Enable}}$:** For multi-chip output multiplexing; controls the state of both Ch1 and Ch2 outputs. When this input is placed high (logic '1') both outputs are set to a high impedance. When placed low (logic '0') both outputs are enabled.
6	**Ch 2 Output:** The digital output of the Channel 2 SPM detector when enabled. The format of the signal at this pin, in common with Ch 1, is selectable to either 'Tone Follower' or 'Packet' mode via the Output Select input.
7	**Ch 1 Output:** The digital output of the Channel 1 SPM detector when enabled. The format of the signal at this pin, in common with Ch 2, is selectable to either 'Tone Follower' or 'Packet' mode via the Output Select input.
8	**V_{BIAS}:** The output of the on-chip analogue bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} (see Figure 2).
9	**Ch 1 Amp Out:** The output of the Channel 1 Input Amplifier. See Figures 2 and 3.
10	**Ch 1 Amp In (-):** The negative input to the Channel 1 Input Amplifier. See Figures 2 and 3.
11	**Ch 1 Amp In (+):** The positive input to the Channel 1 Input Amplifier. See Figures 2 and 3.
12	**V_{SS}:** Negative supply rail (GND).

Pin Number FX641 D2/P4	Function
13	No internal connection; leave open circuit.
14	**Ch 2 Amp In (+):** The positive input to the Channel 2 Input Amplifier. See Figures 2 and 3.
15	**Ch 2 Amp In (-):** The negative input to the Channel 2 Input Amplifier. See Figures 2 and 3.
16	**Ch 2 Amp Out:** The output of the Channel 2 Input Amplier. See Figures 2 and 3.
17	**Output Select:** A logic input to set the Channel 1 and Channel 2 output modes. When high (logic '1'), the outputs are in the Tone Follower mode; when low (logic '0'), the outputs are in the Packet mode.
18	**Preset Level:** A logic input to set the sensitivity mode of the FX641. When high (logic '1'), both channels are in the Fixed Sensitivity mode. The external components govern the input sensitivity; the System Select input selects 12kHz or 16kHz operation. When low (logic '0'), both channels are in the Controlled Sensitivity mode. Device sensitivities and system selection are via the Chip Select/Serial Data/Serial Clock inputs. This input has an internal pullup resistor on chip (Fixed Sensitivity Mode).
19	**$\overline{\text{Chip Select}}$:** The Chip Select input for use in data loading when using the FX641 in the Controlled Sensitivity mode (see Figure 9). The device is selected when this input is set low (logic '0'). When the device is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.
20	**Serial Clock:** The Serial Clock input for use in data loading when using the FX641 in the Controlled Sensitivity mode (see Figure 9). Data is loaded to the FX641 on this clock's rising edge. When the device is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.
21	**Serial Data:** The Serial Data input for use in data loading when using the FX641 in the Controlled Sensitivity mode (see Figure 9 and Table 2). When the device is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.
22	**System Select:** In the Fixed Sensitivity mode this pin selects the system frequency. High (logic '1') = 12kHz; Low (logic '0') = 16kHz. In the Controlled Sensitivity mode this pin is inactive and may be left unconnected. This pin has an internal pullup resistor on chip.
23	No internal connection; leave open circuit.
24	**V_{DD}:** Positive supply rail; a single, stable power supply is required. Critical levels and voltages within the FX641 are dependant upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin.

Application Information



Component	Value	Tolerance			
R_1	68kΩ	± 1%	C_1	1.0µF	±20%
R_2	68kΩ	±1%	C_2	1.0µF	±20%
R_3	750kΩ	±1%	C_3	270pF	±5%
R_4	750kΩ	±1%	C_4	270pF	±5%
R_5	68kΩ	± 1%	C_5	270pF	±5%
R_6	68kΩ	± 1%	C_6	270pF	±5%
R_7	750kΩ	±1%			
R_8	750kΩ	±1%	X_1	3.579545MHz	

Fig.2 Recommended External Components

Fixed Sensitivity Setting

Note that when calculating/selecting gain components, R_3, R_4, R_7 and R_8 should always be greater than or equal to 100kΩ.

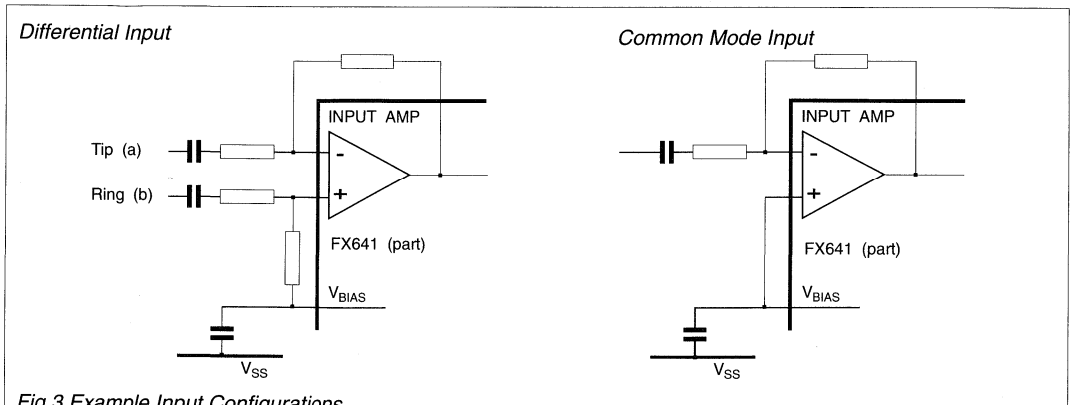
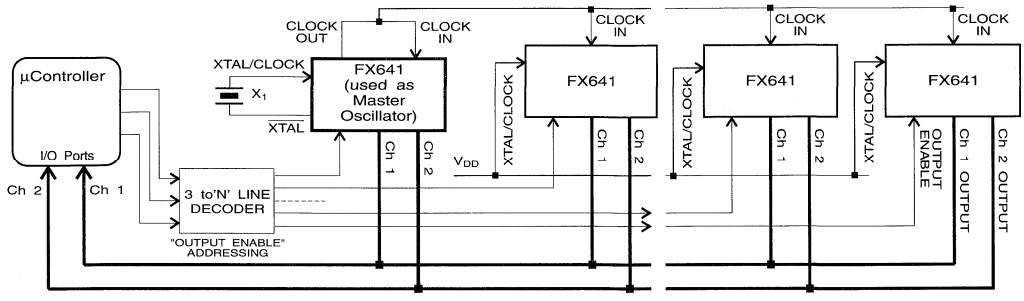


Fig.3 Example Input Configurations

Application Information .....



Maximum number of driven clocks (including Master) = 4
Maximum capacitive load on Clock Out output = 15.0pF

Fig.4 Examples of Xtal/Clock Distribution and Output Multiplexing

Xtal/Clock Distribution

The FX641 requires a 3.579545MHz Xtal or clock pulse input. With the exception of the Xtal, all oscillator components are incorporated on chip. If a Xtal input is employed the Clock Out pin should be directly linked to the Clock In pin.

To reduce component and layout complexity, the clock requirements of up to 3 additional FX641 microcircuits may be supplied from a Xtal-driven FX641 acting as the system master clock. With reference to Figure 4, the clock should be distributed as illustrated and the Xtal/Clock pins of the driven microcircuits should be connected directly to V_{DD}. Note that the maximum load on the master Clock Out pin should not be exceeded.

Channel Outputs

Channels 1 and 2 outputs operate together under the control of the Output Enable and Output Select inputs. Table 3 describes the operations.

The Front Page description describes the output formats.

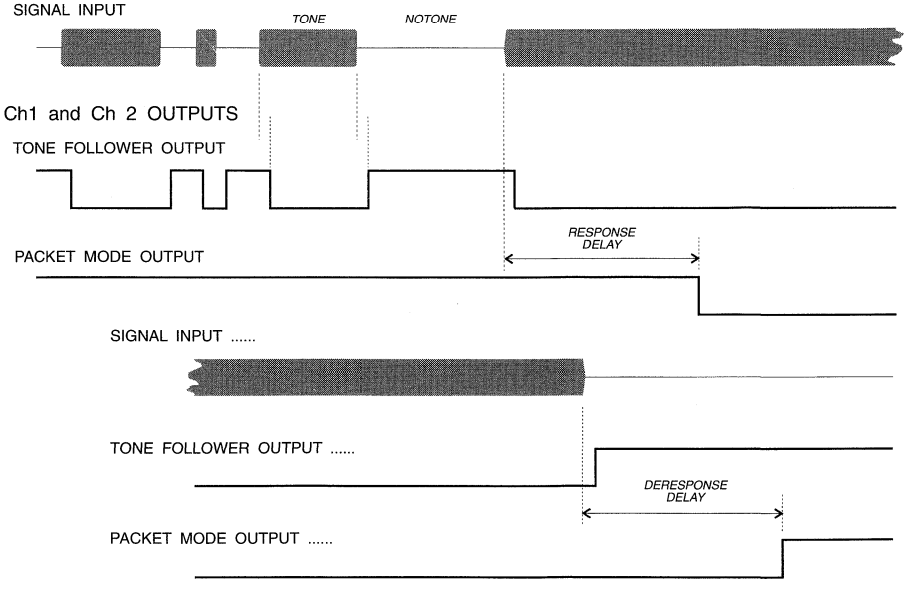


Fig.5 Tone Follower and Packet Mode Outputs

Application Information .....

Sensitivity Setting

To enable the FX641 to operate correctly to most national 12kHz and 16kHz SPM specifications, the input sensitivity can be accurately adjusted and set.

There are two different pin-selectable modes of sensitivity setting available to the FX641: Controlled Sensitivity Mode and Fixed Sensitivity Mode

The Controlled Sensitivity mode allows the sensitivity setting from a µController via a 6-bit serial data input. This same serial input also sets operation (bit 0) to either 12kHz or 16kHz systems. Both channels are set identically.

The Fixed Sensitivity mode allows the sensitivity of each channel to be set to a fixed "gain" by external components at the input amplifiers. Operation to either 12kHz or 16kHz is by the System Select input.

Controlled Sensitivity Setting

Serial Data Bits D_5 - D_1	Bandpass Filter Gain (dB)	12kHz System Bit D_0 = '1' Minimum Sensitivity dB(ref.)	12kHz System Bit D_0 = '1' Nominal Sensitivity dB(ref.)	12kHz System Bit D_0 = '1' Maximum Sensitivity dB(ref.)	16kHz System Bit D_0 = '0' Minimum Sensitivity dB(ref.)	16kHz System Bit D_0 = '0' Nominal Sensitivity dB(ref.)	16kHz System Bit D_0 = '0' Maximum Sensitivity dB(ref.)
0 0 0 0 0	0	-16.2	-17.5	-18.8	-16.9	-18.2	-19.5
0 0 0 0 1	1.0	-17.2	-18.5	-19.8	-17.9	-19.2	-20.5
0 0 0 1 0	2.0	-18.2	-19.5	-20.8	-18.9	-20.2	-21.5
0 0 0 1 1	3.0	-19.2	-20.5	-21.8	-19.9	-21.2	-22.5
0 0 1 0 0	4.0	-20.2	-21.5	-22.8	-20.9	-22.2	-23.5
0 0 1 0 1	5.0	-21.2	-22.5	-23.8	-21.9	-23.2	-24.5
0 0 1 1 0	6.0	-22.2	-23.5	-24.8	-22.9	-24.2	-25.5
0 0 1 1 1	7.0	-23.2	-24.5	-25.8	-23.9	-25.2	-26.5
0 1 0 0 0	8.0	-24.2	-25.5	-26.8	-24.9	-26.2	-27.5
0 1 0 0 1	9.0	-25.2	-26.5	-27.8	-25.9	-27.2	-28.5
0 1 0 1 0	10.0	-26.2	-27.5	-28.8	-26.9	-28.2	-29.5
0 1 0 1 1	11.0	-27.2	-28.5	-29.8	-27.9	-29.2	-30.5
0 1 1 0 0	12.0	-28.2	-29.5	-30.8	-28.9	-30.2	-31.5
0 1 1 0 1	13.0	-29.2	-30.5	-31.8	-29.9	-31.2	-32.5
0 1 1 1 0	14.0	-30.2	-31.5	-32.8	-30.9	-32.2	-33.5
0 1 1 1 1	15.0	-31.2	-32.5	-33.8	-31.9	-33.2	-34.5
1 0 0 0 0	16.0	-32.2	-33.5	-34.8	-32.9	-34.2	-35.5
1 0 0 0 1	17.0	-33.2	-34.5	-35.8	-33.9	-35.2	-36.5
1 0 0 1 0	18.0	-34.2	-35.5	-36.8	-34.9	-36.2	-37.5
1 0 0 1 1	19.0	-35.2	-36.5	-37.8	-35.9	-37.2	-38.5
1 0 1 0 0	20.0	-36.2	-37.5	-38.8	-36.9	-38.2	-39.5
1 0 1 0 1	21.0	-37.2	-38.5	-39.8	-37.9	-39.2	-40.5
1 0 1 1 0	22.0	-38.2	-39.5	-40.8	-38.9	-40.2	-41.5
1 0 1 1 1	23.0	-39.2	-40.5	-41.8	-39.9	-41.2	-42.5
1 1 0 0 0	24.0	-40.2	-41.5	-42.8	-40.9	-42.2	-43.5
1 1 0 0 1	25.0	-41.2	-42.5	-43.8	-41.9	-43.2	-44.5
1 1 0 1 0	26.0	-42.2	-43.5	-44.8	-42.9	-44.2	-45.5
1 1 0 1 1	27.0	-43.2	-44.5	-45.8	-43.9	-45.2	-46.5
1 1 1 0 0 1 1 1 0 1 1 1 1 1 0 1 1 1 1 1	These states should never be used. If senstivities of this order are required (eg. the Swedish Rural SPM Specification), it is recommended that the Controlled Sensitivity setting is set to 20dB (1 0 1 0 0) and external components selected to set the Input Amp gain to a higher figure.						

Table 2 Controlled Sensitivity Setting Information

The figures provided in Table 2 assume:

1. The recommended amplifier components (see Figure 2) are employed providing an amplifier gain at 16kHz of 19.8dB ±0.3dB or at 12kHz of 19.1dB ±0.3dB.
2. A comparator sensitivity of 1.6dB(ref.) ±1dB (the variation being due to filter gain error, filter output offset, comparator input offset or a combination of all 3).
3. The applied V_{DD} is 5.0 volts; 0dB (ref.) = 775mVrms.

Application Information .....

Controlled Sensitivity Setting .....

With the external gain (sensitivity) components employed as shown in Figure 2 the gain of the input stages is 19.8dB (12kHz) or 20.5dB (16kHz). For controlled sensitivity setting the gain of each bandpass filter, and hence the device sensitivity, is adjusted by the applied serial bits D_1 to D_5.

In the Controlled Sensitivity mode the system frequency is selected by bit D_0 ('1' = 12kHz; '0' = 16kHz). Data is loaded Bit 5 (D_5) first.

Table 2 details the serial data input to produce the required sensitivity. Minimum, Nominal and Maximum Sensitivity figures are provided to make complete allowance for internal circuit offsets and component tolerances. 0dB(ref.) = 775mVrms at V_{DD} = 5.0 volts; varies directly with V_{DD}.
Examples are provided as a guide to meeting national specifications.

German FTZ Specification 16kHz

This system has a Must Decode level of -21dB(ref.) and a Must-Not Decode level of -27dB(ref.).
Reference to Table 2 shows that Bandpass Filter Gain settings of 5dB, 6dB or 7dB will enable an FX641 channel to meet this level specification.
Figure 6 illustrates the range of these various settings.

Hence to meet the German FTZ specification, the input data (D_5 to D_0) can be:

	0 0 1 0 1	**0**	**5.0dB**
or	***0 0 1 1 0***	***0***	***6.0dB***
or	**0 0 1 1 1**	**0**	**7.0dB**

Selecting the middle setting would give the greatest noise immunity.

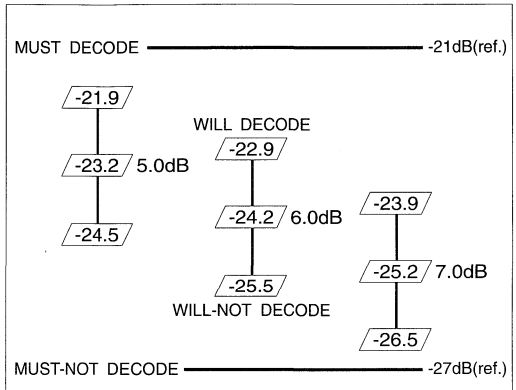


Fig.6 German Specification -Possible Settings

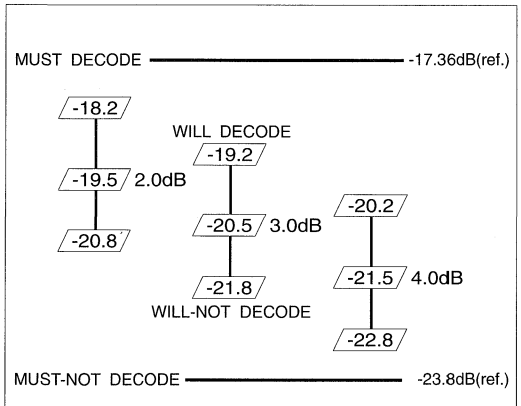


Fig.7 French Specification -Possible Settings

French Specification 12kHz

This system has a Must Decode level of -17.36dB(ref.) and a Must-Not Decode level of -23.8dB(ref.). Reference to Table 2 shows that Bandpass Filter Gain settings of 2dB, 3dB or 4dB will enable an FX641 channel to meet this level specification.
Fig 7 illustrates the range of these various settings.

Hence to meet the French SPM specification, the input data (D_5 to D_0) can be:

	0 0 0 1 0	**1**	**2.0dB**
or	***0 0 0 1 1***	***1***	***3.0dB***
or	**0 0 1 0 0**	**1**	**4.0dB**

Selecting the middle setting would give the greatest noise immunity.

System Select	Preset Level	Output Select	Output Enable	Operating Mode	
X	0	0	0	Packet Mode Output;	Serial Data Control
X	0	1	0	Tone Follower Output;	Serial Data Control
0	1	0	0	Packet Mode Output;	Preset Sensitivity 16kHz
1	1	0	0	Packet Mode Output;	Preset Sensitivity 12kHz
0	1	1	0	Tone Follower Output;	Preset Sensitivity 16kHz
1	1	1	0	Tone Follower Output;	Preset Sensitivity 12kHz
X	X	X	1	Tristate Output	High Z

Table 3 Operating Mode Configurations *X = don't care*

Application Information .....

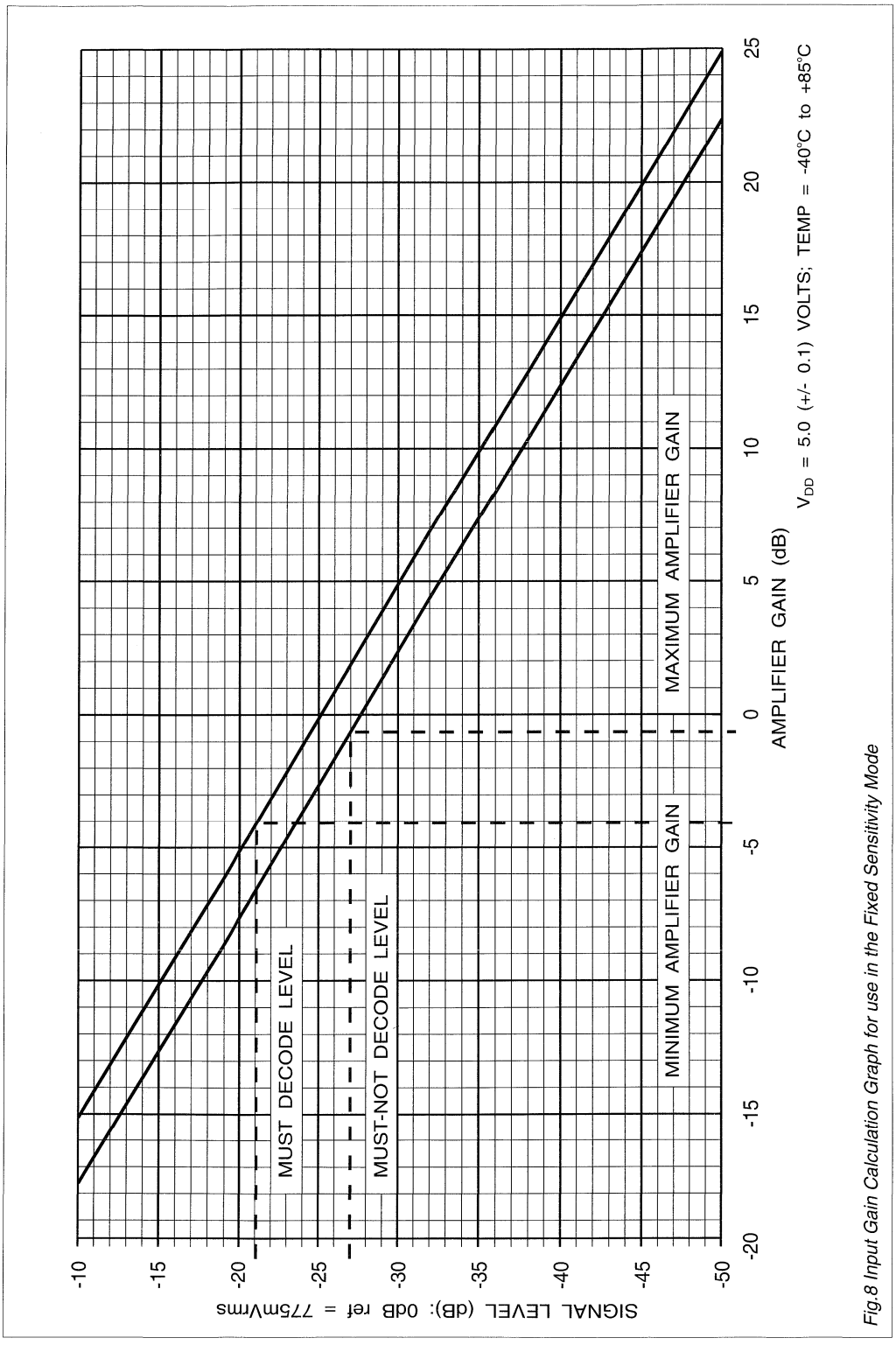


Fig.8 Input Gain Calculation Graph for use in the Fixed Sensitivity Mode

Application Information .....

Fixed Sensitivity Setting

In this mode the sensitivity of each channel is set by the correct selection of the components around the Channel Input Amplifier.
Note that the device sensitivity is directly proportional to the applied power supply (V_{DD}).

Input Gain Calculation

The input amplifier, with its external circuitry, is available to set the sensitivity of the FX641 to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels.

With reference to the graph in Figure 8, the following steps will assist in the determination of the required gain/attenuation.

Step 1

Draw two horizontal lines from the Y-axis (Signal Level (dB)).
The upper line will represent the required 'Must' decode level.
The lower line will represent the required 'Must-Not' decode level.

Step 2

Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis (Amplifier Gain (dB)).
The point where the vertical line meets the X-axis will indicate the MINIMUM Input Amp gain required for reliable decoding of valid signals.

Step 3

Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis.
The point where the vertical line meets the X-axis will indicate the MAXIMUM allowable Input Amp gain.
Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.
Select the *Input Gain Components* as described.

Input Gain Components

With reference to the gain components shown in Figure 2.

The user should calculate and select external components ($R_1/R_3/C_3$, $R_2/R_4/C_4$ and $R_5/R_7/C_5$, $R_6/R_8/C_6$) to provide amplifier gains within the limits obtained in Steps 2 and 3.

Component tolerances should not move the gain-figure outside these limits. The graph in Figure 8 is for the calculation of input gain components for an FX641 using a V_{DD} of 5.0 (±0.1) volts.

It is recommended that the designed gain is near the centre of the calculated range.

Microcircuit Protection Against High Voltages

Telephone systems may have high d.c. and a.c. voltages present on the line. If the FX641 is part of a host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within V_{DD} +0.3V and V_{SS} -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the FX641 will require protection diodes at its signal inputs (+ and -). The breakdown voltage of capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the d.c. voltages plus all expected signal peaks.

Aliasing

Due to the switched-capacitor filters employed in the FX641, care should be taken, with the chosen external components, to avoid the effects of alias distortion.

Possible Alias Frequencies:

12kHz Mode = 52kHz
16kHz Mode = 69kHz

If these alias frequencies are liable to cause problems and/or interference, it is recommended that anti-alias capacitors are employed across input resistors R_3 and R_4 or R_7 and R_8.

Values of anti-alias capacitors should be chosen so as to provide a highpass cutoff frequency, in conjunction with R_3 (R_4) (R_7) (R_8) of approximately 20kHz to 25kHz (12kHz system) or 25kHz to 30kHz (16kHz system).

$$\text{i.e. } C = \frac{1}{2 \times \pi \times f_0 \times R_3}$$

When anti-alias capacitors are used, allowance must be made for reduced gain at the SPM frequency (12kHz or 16kHz).

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating Temperature (T_{OP}):	**FX641D2/P4**	-40°C to +85°C
Storage Temperature range (T_{ST}):	**FX641D2/P4**	-40°C to +85°C

Operating Limits

Correct operation of the device outside these limits is not implied.

Parameter	Min.	Max.	Unit
Supply Voltage (V_{DD})	4.5	5.5	V
Operating Temperature (T_{OP})	-40.0	+85.0	°C
Xtal/Clock/Clock In Frequency	3.558918	3.589368	MHz

Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V T_{AMB} = -40°C to +85°C. Audio Level 0dB(ref.): = 775mVrms. Noise Bandwidth = 50kHz.

Xtal/Clock or 'Clock In' Frequency = 3.579545MHz. System Setting = 12kHz or 16kHz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Current		-	2.0	5.0	mA
Input/Output Parameters					
Clock Out Load		-	-	15.0	pF
Logic Inputs					
Input Logic '1' (High)		3.5	-	-	V
Input Logic '0' (Low)		-	-	1.5	V
Input Leakage Current (V_{IN} = 0 to V_{DD})	13	-5.0	-	5.0	µA
Input Current (V_{IN} = 0)	14	-15.0	-	-	µA
Channel Outputs					
Output Logic '1' (I_{OH}) = 120µA) (Enabled)	1	4.6	-	-	V
Output Logic '0' (I_{OL}) = 360µA) (Enabled)	1	-	-	0.4	V
Output Leakage Current (High-Z Output)	2	-5.0	-	5.0	µA
Input Amplifier					
D. C. Gain		60.0	-	-	dB
Bandwidth (-3dB)		-	100	-	Hz
Input Impedance		1.0	-	-	MΩ
Overall Performance					
12kHz Detect Bandwidth	3	11.82		12.18	kHz
12kHz Not-Detect Frequencies (below 12kHz)	3	-	-	11.52	kHz
12kHz Not-Detect Frequencies (above 12kHz	3	12.48	-	-	kHz
16kHz Detect Bandwidth	3	15.76		16.24	kHz
16kHz Not-Detect Frequencies (below 16kHz)	3	-	-	15.36	kHz
16kHz Not-Detect Frequencies (above 16kHz)	3	16.64	-	-	kHz
Level Sensitivity					
Controlled Sensitivity Mode	3, 4, 12, 15	2.6	1.6	0.6	dB(ref.)
Preset Sensitivity Mode	3, 4, 5, 16	-25.4	-26.4	-27.4	dB(ref.)
Signal Quality Requirements for Correct Operation					
Signal-to-Noise (Amp Input)	4, 8, 9, 10	22.0	20.0	-	dB
Signal-to-Voice (Amp Input)	4, 8, 9, 11	-36.0	-40.0	-	dB
Signal-to-Voice (Amp Output)	4, 8, 10, 11	-1.0	-	-27.0	dB

Continued on next page .....

Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
Channel Outputs (Ch1 and Ch2) Figure 5					
Mode Change Time	6	-	-	500	ns
Tone Follower Mode (Table 3)					
Response and De-Response Time	3, 4, 7	-	-	10.0	ms
Packet Mode (Table 3)					
Response and De-Response Time	3, 4, 7	40.0	-	48.0	ms

Notes

1. Tone Follower or Packet mode enabled; see Table 3.
2. Tristate selected; see Table 3.
3. With adherence to Signal-to-Voice and Signal-to Noise specifications.
4. 12kHz and/or 16kHz system.
5. With Input Amp gain setting = 0dB.
6. Time taken to change between any two of the operational modes: Tone Follower, Packet or Tristate, and with a maximum capacitive load of 30pF on an output.
7. The time delay, after a valid serial data load (or after device powerup), before the condition of the outputs can be guaranteed correct.
8. Immunity to false responses and/or de-responses.
9. Common Mode SPM and balanced voice input signal.
10. With SPM and voice signal amplitudes balanced; to avoid false de-responses due to saturation, the peak-to-peak voice + noise level at the output of the Input Amp should be no greater than the dynamic range of the device. For this reason, the signal-to-voice figure at the Am[Output will vary with the sensitivity setting. The lowest signal-to-voice figure occurs at the highest sensitivity setting (*Table 2,* 27dB).
11. Maximum voice frequencies = 3.4kHz.
12. With the Input Amplifier gain at 0dB and the Bandpass Filter gain set at 0dB (Table 2); subtract 1.0dB from this specification for each extra single dB of Bandpass Filter gain programmed.
    Alternatively, with the input components as recommended in Figure 2, the sensitivity is as defined in Table 2.
13. Logic inputs with no internal pullup; Chip Select, Serial Data, Serial Clock, Output Enable, Output Select and Clock In pins.
14. Logic inputs with an internal pullup; Preset Level and System Select pins.
15. Preset Level= '0', System Select = don't care; Chip Select, Serial Clock and Serial Data inputs active; see Table 3.
16. Preset Level = '1', System Select = input active; Chip Select, Serial Clock and Serial Data inputs inactive; see Table 3.

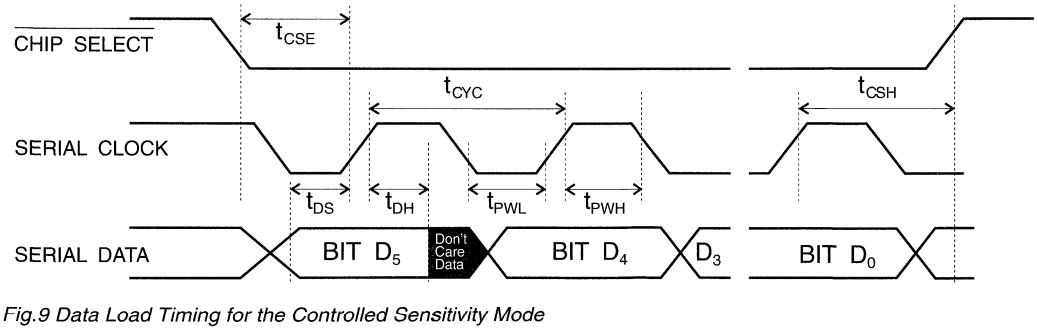


Fig.9 Data Load Timing for the Controlled Sensitivity Mode

Parameter		Min.	Typ.	Max.	Unit
t_{PWH}	Serial Clock 'High' Pulse Width	250	-	-	ns
t_{PWL}	Serial Clock 'Low' Pulse Width	250	-	-	ns
t_{CYC}	Serial Clock Period	600	-	-	ns
t_{CSE}	Chip Select 'Low' to Clock 'High' Edge	450	-	-	ns
t_{DH}	Data Hold Time	50.0	-	-	ns
t_{DS}	Data Setup Time	250	-	-	ns

Package Outlines

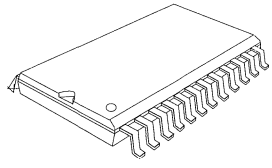
The FX641 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX641 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX641D2 24-pin plastic S.O.I.C.

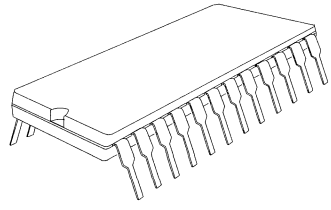
NOT TO SCALE



Max. Body Length	15.70mm
Max. Body Width	7.65mm

FX641P4 24-pin plastic DIL

NOT TO SCALE



Max. Body Length	31.85mm
Max. Body Width	13.82mm

Ordering Information

FX641D2 24-pin plastic S.O.I.C.

FX641P4 24-pin plastic DIL

Integrated Circuits Data Book

Section 7

General Purpose

CML Semiconductor Products

PRODUCT INFORMATION

FX002 Signal to Noise Enhancer

Publication D/002/2 July 1994

Features

- **Up to 8.5dB Signal-to-Noise Improvement**
- **Input Frequency Range: 17Hz to 13kHz** [Sub-Audio and Audio Frequencies]
- **Low-Voltage Operation: 2.5 Volts**
- **10mVrms Minimum Signal Input**
- **Digital Output Signal (f_{IN} x 4)**
- **'Divided-Down' Clock Outputs**

Applications

- **Radio Communications and Paging Systems**
- **Tone Detection**
- **Sonar Detection and Analysis**
- **Slow Data-Rate Communications**
- **Medical Equipment**
- **Interference Investigation**

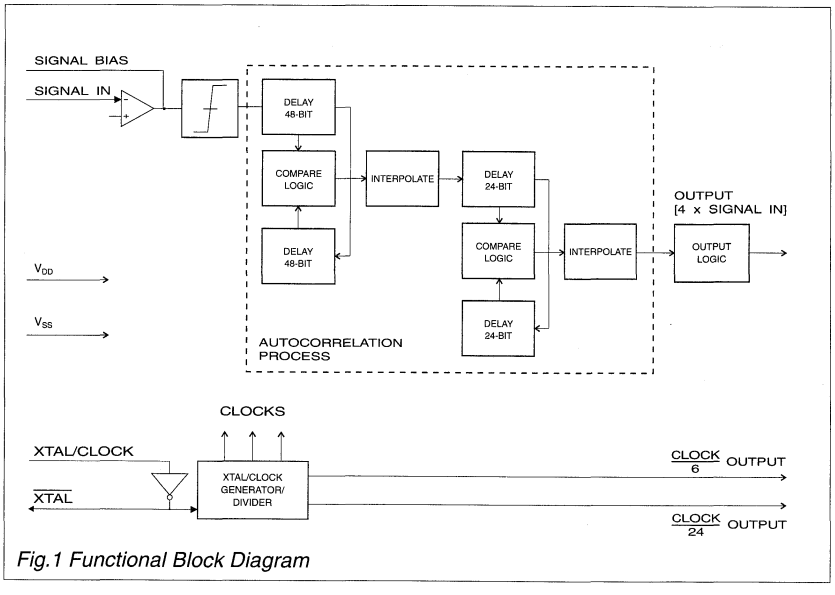


Fig.1 Functional Block Diagram

FX002

Brief Description

The FX002 is a single-chip device to extract single periodic signals from very high random-noise environments.

Using patented autocorrelation techniques the FX002 will enhance the input signal's signal-to-noise ratio by as much as 8.5dB and provide a digital output signal centred at four times (x4) the input frequency.

The amplitude of non-periodic components of the signal is substantially reduced. The patented autocorrelator compares the incoming signal to itself; the more elements of the waveform that are seen as periodic, the higher the energy at the microcircuit output.

The FX002 cascades two autocorrelators, each one improving the signal-to-noise ratio.

With a random noise input the output will swing rail-to-rail at random (peak-limited). The input/output signal delay is fixed by the choice of clock frequency and the length of the internal register. The FX002 will operate at supply voltages of between 2.5 volts and 5.5 volts and with Xtal/clock frequencies from 20kHz to 2.5MHz. Using various Xtal/clock inputs the device can be set to accept input signal frequencies, in bands, from 17.0Hz to 13.0kHz.

Two uncommited clock outputs are available to supply 'divided-down' Xtal/clock frequencies for use in external and peripheral functions.

This low-power signal processing device is available in 16-pin cerdip dual-in-line (DIL) and plastic small outline (S.O.I.C.) surface mount packages.

Pin Number		Function
FX002DW	FX002J	
1	1	**Signal In:** The inverting input to the analogue amplifier/comparator. Used with the Signal Bias pin; external coupling components are required (see Figure 2).
3	3	**Signal Bias:** The output of the analogue amplifier/comparator. Do not load this pin with peripheral circuitry; there is no drive capacity for off-chip signalling. The feedback resistor should be not less than 200kΩ. See Figure 2.
4	4	**V_{DD}:** Positive supply rail. A single, stable power supply is required. Note that this device has two V_{DD} pins; this input is positioned to prevent cross-talk, either or both may be connected to the host circuit's supply line. Do not attempt to draw current from either V_{DD} pin.
5	5	**Clock/24:** A squarewave output clock signal at the rate of $^{Xtal/clock}/_{24}$; provided for peripheral and test purposes.
6	6	**$\overline{Xtal}$:** The output of the on-chip clock oscillator inverter.
8	7	**Xtal/Clock:** The input to the on-chip clock oscillator inverter; this may be a Xtal, resonator or clock pulse input. The selection of this frequency will affect the operational input signal bandwidth (and output frequency) of this device; refer to Table 2. Note that the choice of V_{DD} will determine the maximum Xtal/clock frequency and hence the maximum useable signal input frequency. Operation of any CML microcircuit without an active Xtal or clock input may cause device damage. A clock pulse input is fed directly into this pin; Xtal/clock components are not required. Table 1 provides a guide to maximum usable Xtal/clock frequencies at pre-determined V_{DD} values.
9	9	**V_{SS}:** Negative supply rail (GND).
11	11	**Clock/6:** A squarewave output clock signal at the rate of $^{Xtal/clock}/_{6}$; provided for peripheral and test purposes.
13	13	**Output:** ($f_{OUT} = 4 \times f_{SIGNAL\ IN}$). The auto-correlated output signal at four times (x 4) the input signal (see Figure 4). There is a time delay between input and output signals (see Specifications).
16	16	**V_{DD}:** Positive supply rail. A single, stable power supply is required. Note that this device has two V_{DD} pins; either or both may be connected to the host circuit's supply line. Do not attempt to draw current from either V_{DD} pin. The choice of V_{DD} will determine the maximum Xtal/clock frequency and hence the maximum useable signal input frequency (see Figure 3).
2, 7, 10, 12, 14, 15	2, 8, 10, 12, 14, 15	No internal connection. Leave open-circuit.

V_{DD} (V)	Max. Xtal/Clock Freq. (MHz)
2.5	0.625
3.0	1.0
5.0	2.5

Table 1

Application Information

External Components

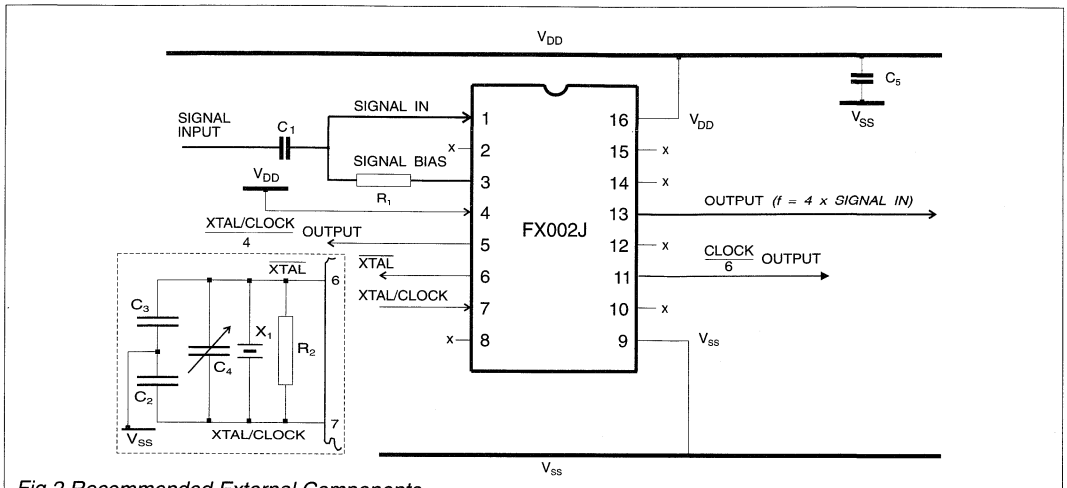


Fig.2 Recommended External Components

Xtal/Clock Freq. (kHz)	Input Freq. (Hz) Min	Max	BW (Hz)
20	17	105	88
100	88	526	443
200	166	1052	886
300	250	1579	1329
400	333	2105	1772
500	416	2632	2216
560	467	2947	2480
600	500	3158	2658
700	583	3684	3101
800	667	4210	3543
900	750	4737	3987
1000	833	5263	4430
2000	1667	10526	8859
2500	2083	13157	11074

Table 2 Input Signal Ranges vs Xtal/Clock Frequency

Component	Value for V_{DD} = 5.0V
R_1	2.2MΩ
R_2	1.0MΩ
C_1	0.01µF
C_2	47.0pF -see below
C_3	47.0pF -see below
C_4	5 - 65pF -see below
C_5	1.0µF
X_1	560kHz resonator
X_1 range	20kHz to 2.5MHz

Table 3 Recommended External Components

Xtal/Clock Components

C_4 is suggested for frequency setting when using a resonator; when a Xtal is used C_4 is omitted. Values of capacitors C_2 and C_3 should be reduced for higher Xtal frequencies and/or lower supply voltages (V_{DD}).

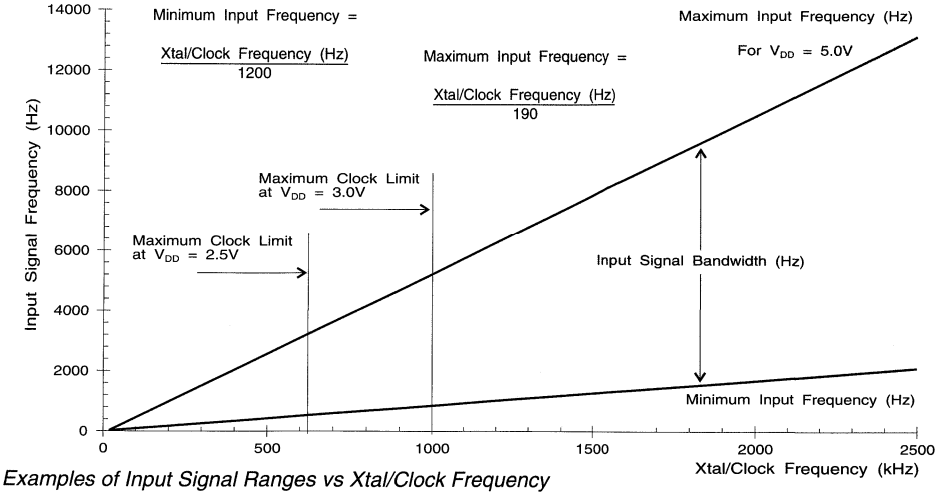


Fig.3 Examples of Input Signal Ranges vs Xtal/Clock Frequency

Application Information .....

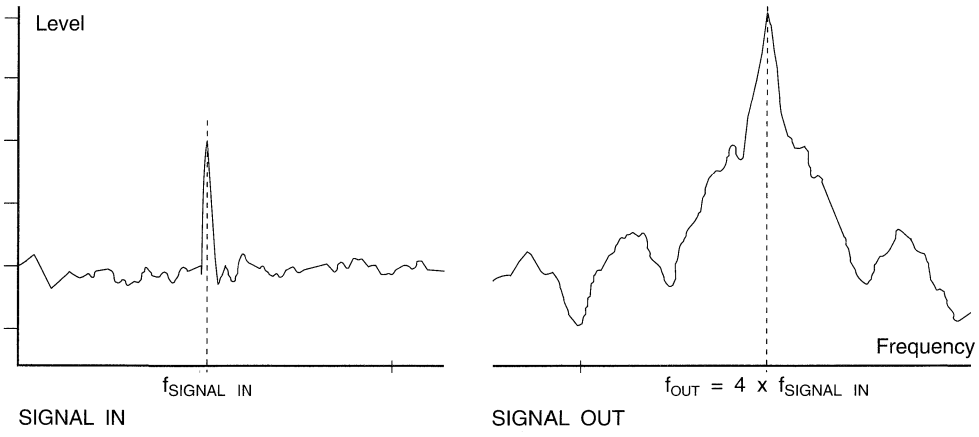


Fig.4 Example FX002 Input/Output Relationships

The diagrams in Figure 4 are example spectrums of the input and output signal conditions of the FX002. Note that the frequency of the output signal is four times (x4) that of the input signal.

The graph shown in Figure 5 illustrates the signal-to-noise enhancement that can be obtained, under varying input conditions, from the FX002.

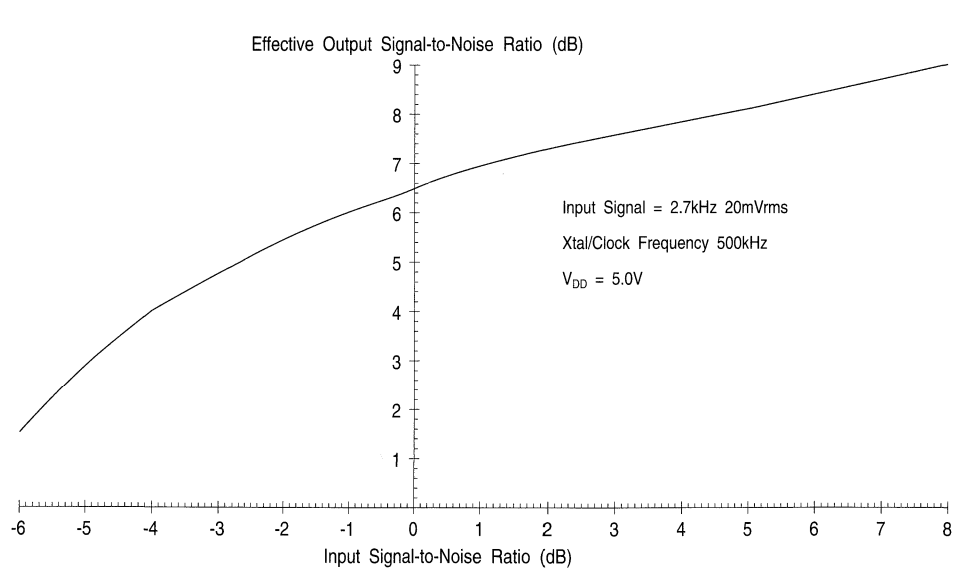


Fig.5 Enhancement of Signal-To-Noise Ratio

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX002DW**	-40°C to +85°C
	FX002J	-40°C to +85°C
Storage temperature range:	**FX002DW**	-40°C to +85°C
	FX002J	-55°C to +125°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Remarks	Min.	Max.	Unit
Supply Voltage (V_{DD})	Note 1	2.5	5.5	V
Operating Temperature		-40.0	+85.0	°C
Xtal/Clock Frequency	(V_{DD} = 2.5V)	20.0	625	kHz
	(V_{DD} = 5.0V)	0.02	2.5	MHz

Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C. Xtal/Clock Frequency = 560kHz. Input Test Signal = 1.0kHz at 200mVrms.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Current (I_{DD})		-	1.0	2.5	mA
	2	-	4.0	-	mA
Output Logic '1'		80%	-	-	V_{DD}
Output Logic '0'		-	-	20%	V_{DD}
Digital Output Impedance		-	4.0	10.0	kΩ
Dynamic Values					
Signal Input Levels	3	10.0	20.0	1000	mVrms
Analogue (Input) Amplifier Gain	4	20.0	-	-	dB
	5	9.0	-	-	dB
	6	10.0	-	-	dB
Recommended Input Signal Mark-to-Space Ratio		35.0	-	-	%
Freq. In/Freq. Out Ratio		4.0		4.0	
Maximum Xtal/Clock Frequency	1	2.5	-	-	MHz
Minimum Xtal/Clock Frequency		-	-	20.0	kHz
Frequency Input Range (Xtal/Clock = 560kHz)		500	-	3000	Hz
(Table 2)	7	1/1200		1/190	Xtal/Clock
Input to Output Delay	8	-	1.4	-	ms
Output Resolution		-	1/6	-	Xtal/Clock

Notes

1. Maximum Xtal/clock frquency allowed varies with applied supply voltage (V_{DD}).
2. I_{DD} requirement for Xtal/clock frequency of 2.24MHz.
3. Signal input level required to provide a constant autocorrelated output.
4. Measured with a 6.0kHz sinewave at the signal input.
5. Measured with V_{DD} = 2.5 volts.
6. Measured with a 12kHz input signal.
7. Recommended input signal frequency range to correlation circuits.
8. Input (Signal In) to output (Output) time with a 2.24MHz Xtal/clock input.

Package Outlines

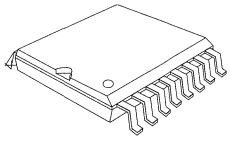
The FX002 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX002 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX002DW 16-pin plastic S.O.I.C. (D4)

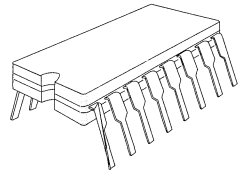
NOT TO SCALE



Max. Body Length 10.31mm
Max. Body Width 7.59mm

FX002J 16-pin cerdip DIL (J2)

NOT TO SCALE



Max. Body Length 19.48mm
Max. Body Width 7.40mm

Ordering Information

FX002DW 16-pin plastic S.O.I.C. (D4)

FX002J 16-pin cerdip DIL (J2)

CML Semiconductor Products

PRODUCT INFORMATION

FX009A Low-Noise Digitally Controlled Amplifier Array

Publication D/009A/3 July 1994

Features/Applications

- **8 Digitally Controlled Low-Noise Amplifiers**
- **15 Gain/Attenuation Steps**
- **7 Trimmers, with a ± 3dB Range in 0.43dB Steps**
- **1 'Volume' Trimmer, with a ± 14dB Range in 2.0dB Steps**
- **8-Bit Serial Data Control**
- **Output Mute/Powersave Function**
- **Audio and Data Gain Control Applications**
- **Cellular, PMR, PABX Applications**

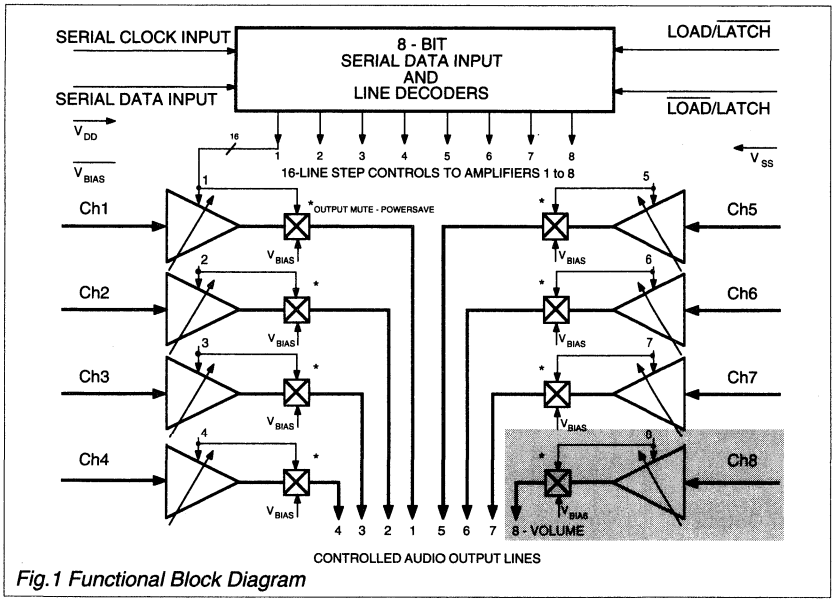


Fig.1 Functional Block Diagram

FX009A

Brief Description

The FX009A Digitally Adjustable Amplifier Array is intended to replace trimmer potentiometers and volume controls in Cellular, PMR, Telephony and Communications applications where d.c., voice or data signals need adjustment.

The FX009A is a low-noise single-chip LSI consisting eight digitally controlled amplifier stages, each with 15 distinct gain/attenuation steps. Control of each individual amplifier is by an 8-bit serial data stream. Seven of the amplifier stages offer a +/-3dB range in steps of 0.43dB, whilst the remaining amplifier offers a +/-14dB range in steps of 2dB, and is intended for volume control applications. Each amplifier includes a 16th 'Mute' state which sets the output to bias ($V_{DD}/2$) and powersaves the entire section. Minimum current drain may be achieved by muting all eight sections.

This product replaces the need for manual trimming of audible signals by using the host microprocessor to digitally control the set-up of all audio levels.

Applications include:

(i) Control, adjustment and set-up of communications equipment by an Intelligent ATE without manual intervention – eg. Deviation, Microphone and L/S Level, Rx Audio Level etc.

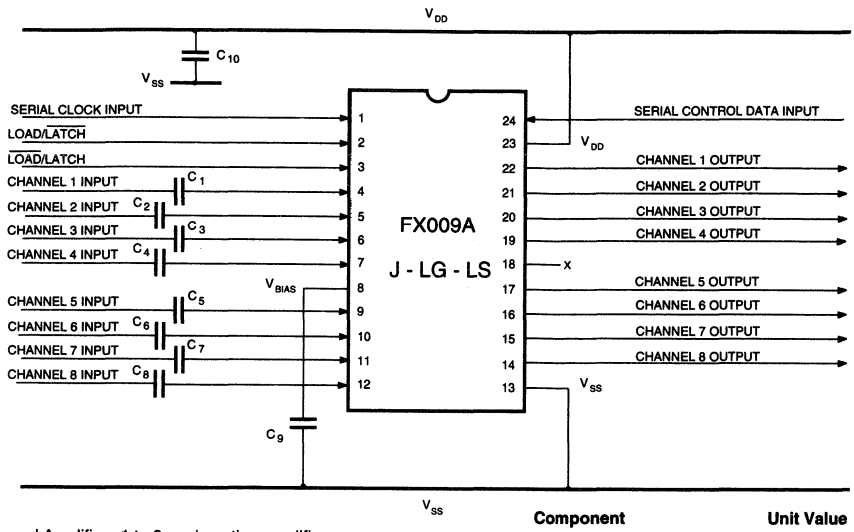
(ii) Automatic Dynamic Compensation of drift caused by variations in temperature, linearity, etc.

(iii) Fully automated servicing and re-alignment.

The FX009A is a low-power, single 5-volt CMOS device available in both 24-pin DIL and SMD package versions.

Pin Number		Function
FX009A J	FX009A LG/LS	
1	1	**Serial Clock :** This external clock pulse input is used to "clock in" the Control Data. See Figure 4, Data Load Timing. This input has an internal 1MΩ pullup resistor.
2	2	**Load/$\overline{\text{Latch}}$:** Governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '0' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '0' ⇒ '1' ⇒ '0' to latch the new data in. Data is executed on the falling edge of the strobe. If the Load/$\overline{\text{Latch}}$ input is used this pin should be left open circuit. This input has an internal 1MΩ pullup resistor.
3	3	**$\overline{\text{Load}}$/Latch :** The inverted Load/$\overline{\text{Latch}}$ input. This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '1' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '1' - '0' - '1' to latch the new data in. Data is executed on the rising edge of the strobe. If the Load/$\overline{\text{Latch}}$ input is used this pin should be left open circuit. This input has an internal 1MΩ pulldown resistor.
4	4	**Ch1 Input :** **Analogue Inputs :**
5	5	**Ch2 Input :** These individual amplifier inputs are self-biasing, a.c. input analogue signals must be capacitively coupled to these pins, as shown in Figure 2.
6	6	**Ch3 Input :** In the powersave modes the inputs are biased at $V_{DD}/2$.
7	7	**Ch4 Input :** Note that amplifiers Ch1 to Ch8 are 'inverting amplifiers.'
8	8	**V_{BIAS} :** The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} as shown in Figure 2.
9	9	**Ch5 Input :** **Analogue Inputs :**
10	10	**Ch6 Input :**
11	11	**Ch7 Input :**
12	12	**Ch8 Input :**
13	13	**V_{SS} :** Negative supply rail (GND).
14	14	**Ch8 Output :** **Analogue Outputs :**
15	15	**Ch7 Output :** The individual "Gain Controlled" amplifier outputs.
16	16	**Ch6 Output :** Ch1 to Ch7 range from -3dB to +3dB in 0.43dB steps, Ch8 could be utilized as a volume control, ranging from -14dB to +14dB in 2.0dB steps.
17	17	**Ch5 Output :** In the powersave mode the selected output is biased at $V_{DD}/2$.
18	18	No internal connection. Do not use.
19	19	**Ch4 Output :** **Analogue Outputs**
20	20	**Ch3 Output :** Note that amplifiers Ch1 to Ch8 are 'inverting amplifiers.'
21	21	**Ch2 Output :**
22	22	**Ch1 Output :**
23	23	**V_{DD} :** Positive supply rail. A single +5-volt power supply is required.
24	24	**Control Data Input :** Operation of the 8 amplifier channels (Ch1 – Ch8) is controlled by the 8 bits of data entered serially at this pin . The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1, 2 and Figure 4. This input has an internal 1MΩ pullup resistor.

Application Notes



Notes

(1) Channel Amplifiers 1 to 8 are inverting amplifiers.

(2) Analogue input capacitors C_1 to C_8 are only required for a.c. input signals, d.c. input signals do not require these components.

Component	Unit Value
C_1 to C_8	0.1µ
C_9	1.0µ
C_{10}	1.0µ

Tolerances: C = ± 20%

Fig.2 External Component Connections

Application Recommendations

To avoid excess noise and instability in the final installation it is recommended that the following points be noted.

(a) A noisy or badly regulated power supply can cause instability and/or variance of selected gains.

(b) Care should be taken on the design and layout of the printed circuit board.

(c) All external components (Figure 2) should be kept close to the FX009A package.

(d) Inputs and outputs should be screened wherever possible.

(e) Tracks should be kept short.

(f) Analogue tracks should not run parallel to digital tracks.

(g) A "Ground Plane" connected to V_{SS} will assist in eliminating external pick-up on the channel input and output pins.

(h) Do not run high-level output tracks close to low-level input tracks.

(i) Input signal amplitudes should be applied with due regard to Figure 3.

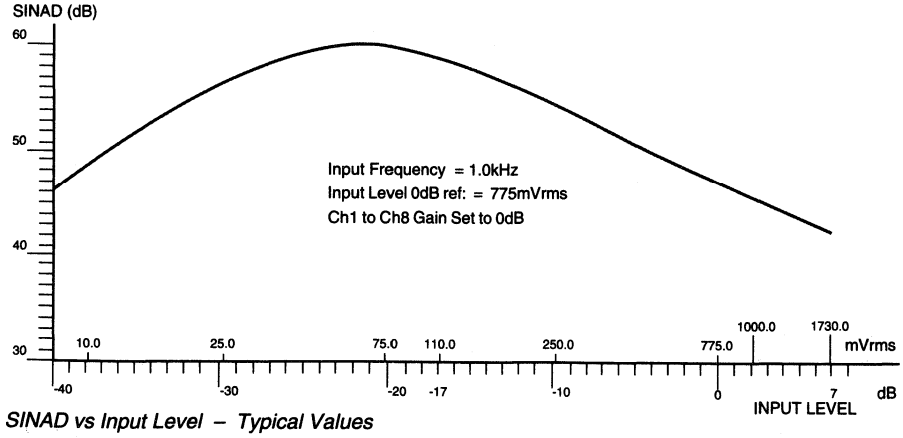


Fig.3 SINAD vs Input Level – Typical Values

The gain of each amplifier block (Channel 1 to Channel 8) in the FX009A is set by a separate 8-bit data word (bit 7 to bit 0). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0), is loaded to the Control Data Input in serial format using the external data clock.

Data is loaded to the FX009A on the rising edge of the Serial Clock. Loaded data is executed on the falling (rising) edge of the Load/Latch (Load/Latch) pulse. Table 1 shows the format of each 4-bit Address word, Table 2 shows the format of each Gain Control word with Figure 4 describing the data loading operation and timing.

Table 1 Address Word Format

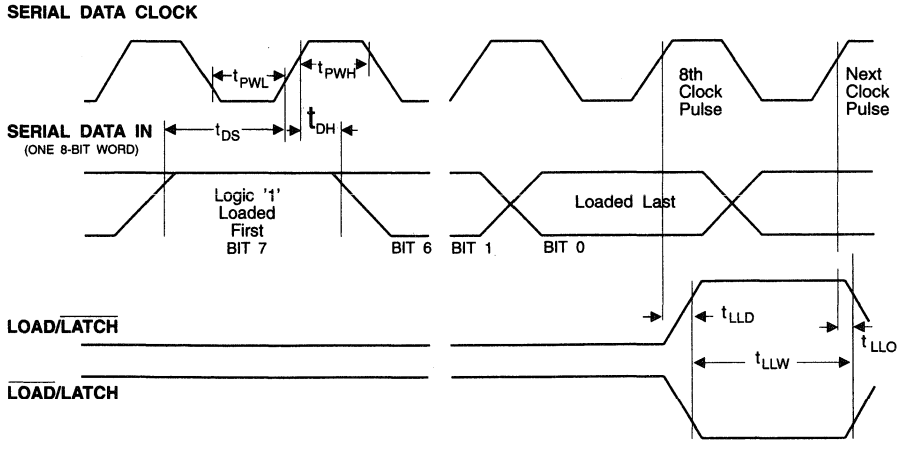
Bit 7 MSB	Bit 6	Bit 5	Bit 4 LSB	Channel Selected
1	0	0	0	1
1	0	0	1	2
1	0	1	0	3
1	0	1	1	4
1	1	0	0	5
1	1	0	1	6
1	1	1	0	7
1	1	1	1	8

Data Loading

The 8-bit data word is loaded *bit 7 first and bit 0* last.
Bit 7 must be a logic "1" to address the chip.
If bit 7 in the word is a logic "0" that 8-bit word will not be executed. Figure 4 (below) shows the timing information required to load and operate this device.

Table 2 Gain Control Word Format

Bit 3 MSB	Bit2	Bit 1	Bit 0 LSB	Stage 1 to 7 (0.43dB)	Stage 8 (2.0dB)
0	0	0	0	Powersave	Powersave
0	0	0	1	-3.0	-14.0 dB
0	0	1	0	-2.571	-12.0 dB
0	0	1	1	-2.143	-10.0 dB
0	1	0	0	-1.714	-8.0 dB
0	1	0	1	-1.286	-6.0 dB
0	1	1	0	-0.857	-4.0 dB
0	1	1	1	-0.428	-2.0 dB
1	0	0	0	0	0 dB
1	0	0	1	0.428	2.0 dB
1	0	1	0	0.857	4.0 dB
1	0	1	1	1.286	6.0 dB
1	1	0	0	1.714	8.0 dB
1	1	0	1	2.143	10.0 dB
1	1	1	0	2.571	12.0 dB
1	1	1	1	3.0	14.0 dB



Timing

t_{PWH}
Serial Clock "High" Pulse Width

t_{PWL}
Serial Clock "Low" Pulse Width

t_{DS}
Data Set-up Time

t_{DH}
Data Hold Time

t_{LLD}
Load/Latch Delay

t_{LLW}
Load/Latch Pulse Width

t_{LLO}
Load/Latch Over Time

Fig.4 Serial Control Data Loading Diagram

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX009A J**	-30°C to +85°C (cerdip)
	FX009A LG/LS	-30°C to +70°C (plastic)
Storage temperature range:	**FX009A J**	-55°C to +125°C (cerdip)
	FX009A LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C. Audio Level 0dB ref: = 775mVrms. Amplifier Gain Set = 0dB.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply Current –					
– All Stages Quiescent		–	0.16	–	mA
– All Stages Operating		–	3.75	–	mA
Dynamic Values					
Control Functions					
Input Logic '1'		3.5	–	–	V
Input Logic '0'		–	–	1.5	V
Digital Input Impedances		0.5	1.0	–	MΩ
Amplifier Stages (General)					
Bandwidth (-3dB)		15.0	–	–	kHz
Output Impedance		–	0.8	3.0	kΩ
Total Harmonic Distortion	1	–	0.35	0.5	%
Output Noise Level (per stage)	2	–	65.0	-	µVrms
Onset of Clipping	3	–	1.73	–	Vrms
Gain Variation	4	–	–	0.1	dB
Interstage Isolation		–	60.0	–	dB
"Trimmer" Stages (Ch1 – Ch7)					
Gain		-3.0		+3.0	dB
Gain per Step (15 in No.)		–	0.43	–	dB
Step Error	5	–	–	±0.2	dB
Input Impedance		100.0	–	–	kΩ
"Volume" Stage (Ch8)					
Gain		-14.0		+14.0	dB
Gain per Step (15 in No.)		–	2.0	–	dB
Step Error	5	–	–	±0.4	dB
Input Impedance		50.0	–	–	kΩ
Timing (Figure 4)					
Serial Clock "High" Pulse Width (t_{PWH})		250	–	–	ns
Serial Clock "Low" Pulse Width (t_{PWL})		250	–	–	ns
Data Set-up Time (t_{DS})		150	–	–	ns
Data Hold Time (t_{DH})		50	–	–	ns
Load/Latch Over Time (t_{LLO})		–	–	50.0	ns
Load/Latch Delay (t_{LLD})		200	–	–	ns
Load/Latch Pulse Width (t_{LLW})		150	–	–	ns
Serial Data Clock Frequency		–	–	2.0	MHz

Notes

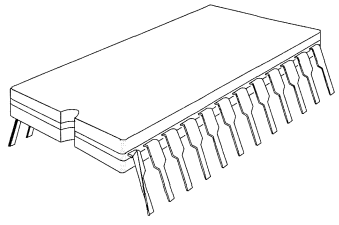
1. Gain Set 0dB, Input Level 1kHz -3.0dB (549mVrms).
2. a.c short-circuit input, measured in a 30kHz bandwidth.
3. See Figure 3.
4. Over temperature and supply voltage range.
5. With reference to a 1.0kHz signal.

Package Outlines

The FX009A is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX009AJ 24-pin cerdip DIL (J4)

NOT TO SCALE



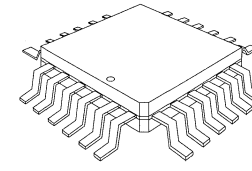
Max. Body Length 32.03mm
Max. Body Width 14.81mm

Handling Precautions

The FX009A is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX009ALG 24-pin quad plastic encapsulated bent and cropped (L1)

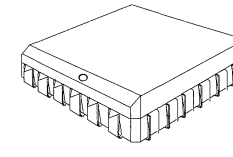
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX009ALS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX009AJ 24-pin cerdip DIL (J4)

FX009ALG 24-pin quad plastic encapsulated bent and cropped (L1)

FX009ALS 24-lead plastic leaded chip carrier (L2)

CML Semiconductor Products

PRODUCT INFORMATION

FX019 Digitally Controlled Quad Amplifier Array

Publication D/019/3 July 1994
Provisional Issue

Features

- 4 Digitally Controlled Amplifiers
- 15 Gain/Attenuation Steps
- 3 Amplifiers, with a ± 3dB Range in 0.43dB Steps
- 1 'Volume' Amplifier, with a ± 14dB Range in 2dB Steps
- 8-Bit Serial Data Control
- Output Mute Function
- Audio and Data Gain Control Applications
- Telecoms, Radio and Industrial Applications

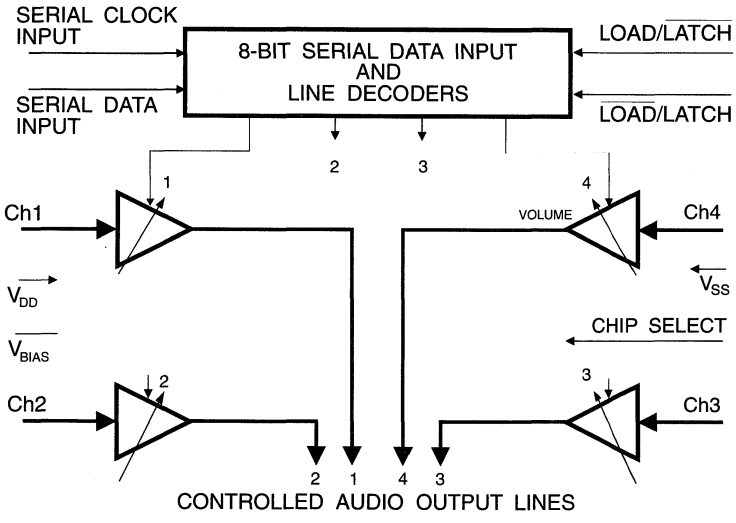


Fig.1 Functional Block Diagram

Brief Description

The FX019 Digitally Adjustable Amplifier Array is available to replace trimmer potentiometers and volume controls in Cellular, PMR, Telephony and Communications applications where d.c., voice or data signals need adjustment.

The FX019 is a single-chip LSI consisting of four digitally controlled amplifier stages, each with 15 distinct gain/attenuation steps. Control of each individual amplifier is by an 8-bit serial data stream. Three of the amplifier stages offer a +/-3dB range in steps of 0.43dB, whilst the remaining amplifier offers a +/-14dB range in steps of 2dB, and is suggested for volume control applications. Each amplifier includes a 16th 'Off' state which when applied, mutes the output audio from that channel. This array uses a Chip Select input to select one of two

This product replaces the need for manual trimming of audible signals by using the host microprocessor to digitally control the set-up of all audio levels during development, production/calibration and operation.

Applications include:

(i) Control, adjustment and set-up of communications equipment by an Intelligent ATE without manual intervention – eg. Deviation, Microphone and L/S Levels, Rx Audio Level etc.

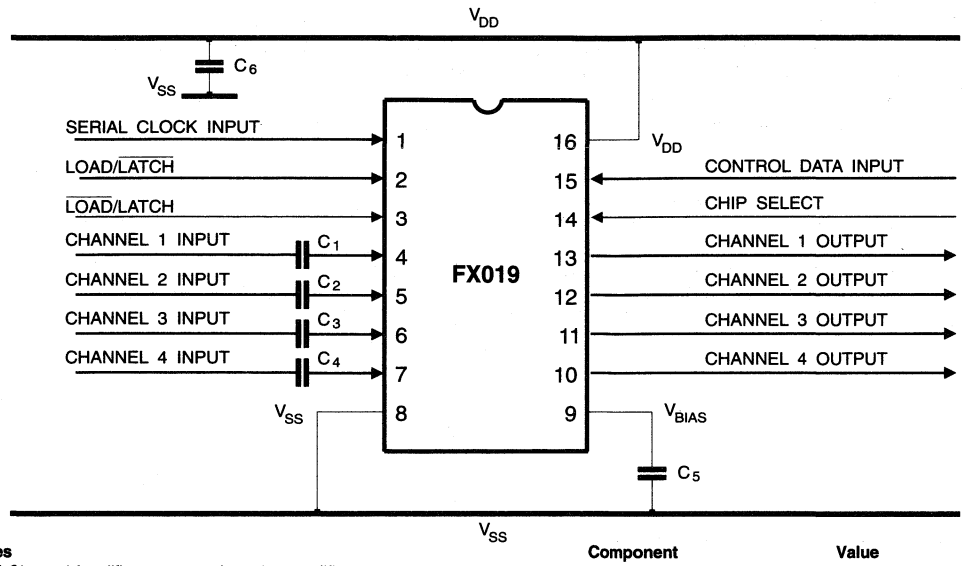
(ii) Automatic Dynamic Compensation of drift caused by variations in temperature, linearity, etc.

(iii) Fully automated servicing and re-alignment.

The FX019 is a low-power, single 5-volt CMOS device available in plastic DIL and Small Outline (S.O.I.C.) package versions.

Pin Number FX019DW FX019P	Function
1	**Serial Clock :** This external clock pulse input is used to "clock in" the Control Data. See Figure 4, Serial Control Data Load Timing. This input has an internal 1MΩ pullup resistor.
2	**Load/$\overline{\text{Latch}}$:** Governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '0' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '0' - '1' - '0' to latch the new data in. Data is executed on the falling edge of the strobe. If the Load/Latch input is used this pin should be left open circuit. This input has an internal 1MΩ pullup resistor.
3	**$\overline{\text{Load}}$/Latch :** The inverted Load/$\overline{\text{Latch}}$ input. This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '1' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '1' - '0' - '1' to latch the new data in. Data is executed on the rising edge of the strobe. If the Load/$\overline{\text{Latch}}$ input is used this pin should be left open circuit. This input has an internal 1MΩ pulldown resistor.
4	**Ch1 Input :** **Analogue Inputs :**
5	**Ch2 Input :** These individual amplifier inputs are self-biasing, a.c. input analogue signals must be capacitively coupled to these pins, as
6	**Ch3 Input :** shown in Figure 2.
7	**Ch4 Input :** Note that amplifiers Ch1 to Ch4 are 'inverting amplifiers.'
8	**V_{SS} :** Negative supply rail (GND).
9	**V_{BIAS} :** The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} as shown in Figure 2.
10	**Ch4 Output :** **Controlled Analogue Outputs :**
11	**Ch3 Output :** The individual "Gain Controlled" amplifier outputs.
12	**Ch2 Output :** Ch1 to Ch3 range from -3dB to +3dB in 0.43dB steps, Ch4 could be utilized as a volume control, ranging from -14dB to +14dB in 2.0dB steps.
13	**Ch1 Output :** In the "OFF" mode there is no output from the selected amplifier.
14	**Chip Select :** A logic input to select one of two FX019 microcircuits in a system, see Table 1. This input has an internal 1MΩ pulldown resistor.
15	**Control Data Input :** Operation of the 4 amplifier channels (Ch1 – Ch4) is controlled by the 8 bits of data entered serially at this pin. The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1, 2 and Figure 4. This input has an internal 1MΩ pullup resistor.
16	**V_{DD} :** Positive supply rail. A single +5-volt power supply is required.

Application Notes



Notes

(1) Channel Amplifiers 1 to 4 are inverting amplifiers.

(2) Analogue input capacitors C_1 to C_4 are only required for a.c. input signals, d.c. input signals do not require these components.

Component	Value
C_1 to C_4	0.1µF
C_5	1.0µF
C_6	1.0µF

Tolerances: C = ± 20%

Fig.2 External Component Connections

Application Recommendations

To avoid excess noise and instability in the final installation it is recommended that the following points be noted.

(a) A noisy or badly regulated power supply can cause instability and/or variance of selected gains.

(b) Care should be taken on the design and layout of the printed circuit board.

(c) All external components (Figure 2) should be kept close to the FX019 package.

(d) Inputs and outputs should be screened wherever possible.

(e) Tracks should be kept short.

(f) Analogue tracks should not run parallel to digital tracks.

(g) A "Ground Plane" connected to V_{SS} will assist in eliminating external pick-up on the channel input and output pins.

(h) Do not run high-level output tracks close to low-level input tracks.

(i) Input signal amplitudes should be applied with due regard to Figure 3.

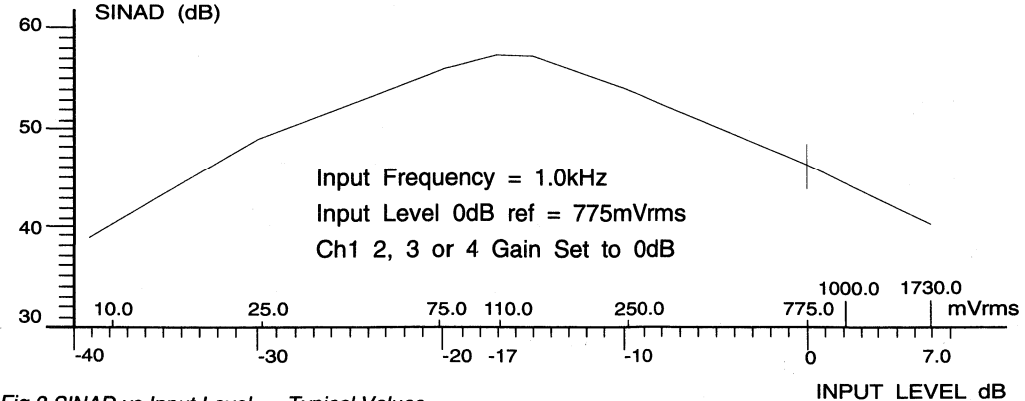


Fig.3 SINAD vs Input Level – Typical Values

Control Data and Timing

The gain of each amplifier block (Channel 1 to Channel 4) in the FX019 is set by a separate 8-bit data word (bit 7 to bit 0). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0), is loaded to the Control Data Input in serial format using the external data clock.

Data is loaded to the FX019 on the rising edge of the Serial Clock. Loaded data is executed on the falling (rising) edge of the Load/Latch (Load/Latch) pulse. Table 1 shows the format of each 4-bit Address word, Table 2 shows the format of each Gain Control word with Figure 4 describing the data loading operation and timing.

Table 1 Address Word Format

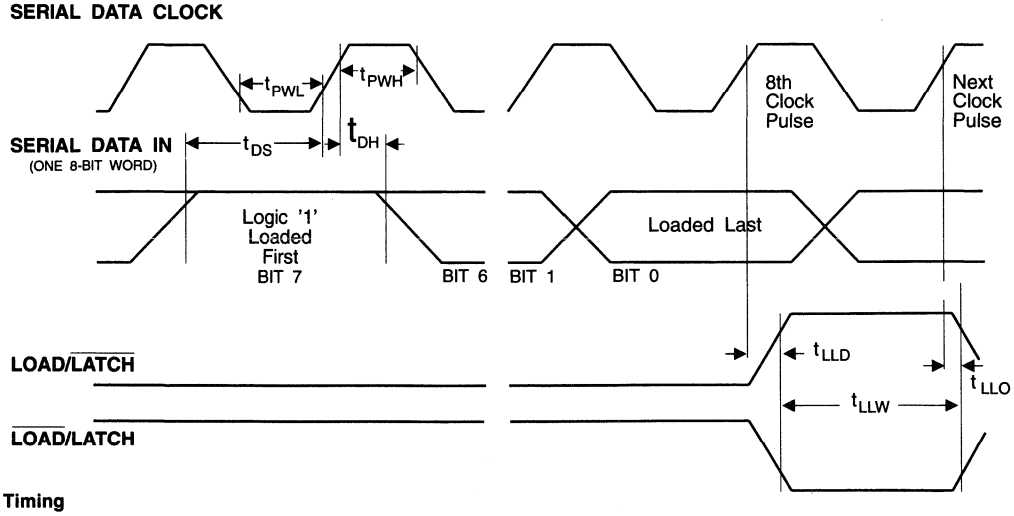
Bit 7 MSB	Bit 6	Bit 5	Bit 4 LSB	Channel Selected	Chip Select	Chip Number
1	0	0	0	1	0	
1	0	0	1	2	0	Chip
1	0	1	0	3	0	1
1	0	1	1	4	0	
1	1	0	0	1	1	
1	1	0	1	2	1	Chip
1	1	1	0	3	1	2
1	1	1	1	4	1	

Table 2 Gain Control Word Format

Bit 3 MSB	Bit2	Bit 1	Bit 0 LSB	Stage 1, 2, 3 (0.43dB)	Stage 4 (2.0dB)
0	0	0	0	OFF	OFF
0	0	0	1	-3.0	-14.0dB
0	0	1	0	-2.571	-12.0
0	0	1	1	-2.143	-10.0
0	1	0	0	-1.714	-8.0
0	1	0	1	-1.286	-6.0
0	1	1	0	-0.857	-4.0
0	1	1	1	-0.428	-2.0
1	0	0	0	0	0
1	0	0	1	0.428	2.0
1	0	1	0	0.857	4.0
1	0	1	1	1.286	6.0
1	1	0	0	1.714	8.0
1	1	0	1	2.143	10.0
1	1	1	0	2.571	12.0
1	1	1	1	3.0	14.0

Data Loading

The 8-bit data word is loaded *bit 7 first and bit 0* last. Bit 7 must be a logic "1" to address the chip. If bit 7 in the word is a logic "0" that 8-bit word will not be executed. The Chip Select input permits the use of two devices in a system; To facilitate this, Bit 6 can be either a logic "0" or "1." Figure 4 (below) shows the timing information required to load and operate this device.



Timing

t_{PWH} Serial Clock "High" Pulse Width

t_{PWL} Serial Clock "Low" Pulse Width

t_{DS} Data Set-up Time

t_{DH} Data Hold Time

t_{LLD} Load/Latch Delay

t_{LLW} Load/Latch Pulse Width

t_{LLO} Load/Latch Over Time

Fig.4 Serial Control Data Loading Diagram

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating temperature range: **FX019DW/P**	-40°C to +85°C (plastic)
Storage temperature range: **FX019DW/P**	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C. Audio Level 0dB ref: = 775mVrms. Amplifier Gain Set = 0dB.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply Current		-	1.5	-	mA
Dynamic Values					
Control Functions					
Input Logic '1'		3.5	–	–	V
Input Logic '0'		–	–	1.5	V
Digital Input Impedances		0.5	1.0	–	MΩ
Amplifier Stages (General)					
Bandwidth (-3dB)		20.0	–	–	kHz
Output Impedance		–	1.0	-	kΩ
Total Harmonic Distortion	1	–	0.35	0.5	%
Output Noise Level (per stage)	2	–	180.0	400.0	µVrms
Onset of Clipping	3	–	1.73	–	Vrms
Gain Variation	4	–	–	0.1	dB
Interstage Isolation		–	60.0	–	dB
"Trimmer" Stages (Ch1 – Ch3)					
Gain		-3.0		+3.0	dB
Gain per Step (15 in No.)		–	0.43	–	dB
Step Error	5	–	–	±0.2	dB
Input Impedance		100.0	–	–	kΩ
"Volume" Stage (Ch4)					
Gain		-14.0		+14.0	dB
Gain per Step (15 in No.)		–	2.0	–	dB
Step Error	5	–	–	±0.4	dB
Input Impedance		50.0	–	–	kΩ
Timing (Figure 4)					
Serial Clock "High" Pulse Width (t_{PWH})		250	–	–	ns
Serial Clock "Low" Pulse Width (t_{PWL})		250	–	–	ns
Data Set-up Time (t_{DS})		150	–	–	ns
Data Hold Time (t_{DH})		50.0	–	–	ns
Load/Latch Pulse Width (t_{LLW})		150	–	–	ns
Load/Latch Delay (t_{LLD})		200	–	–	ns
Load/Latch Over (t_{LLO})		–	–	50.0	ns
Serial Data Clock Frequency		–	–	2.0	MHz

Notes

1. Gain Set 0dB, Input Level 1kHz -3.0dB (549mVrms).
2. With an a.c short-circuit input, measured in a 30kHz bandwidth.
3. See Figure 3.
4. Over the temperature and supply voltage range.
5. With reference to a 1.0kHz signal.

Package Outlines

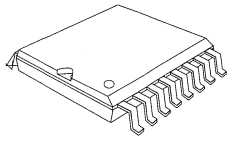
The FX019 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX019 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX019DW 16-pin plastic S.O.I.C. (D4)

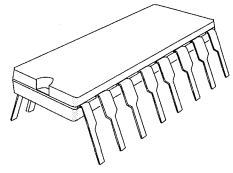
NOT TO SCALE



Max. Body Length 10.31mm
Max. Body Width 7.59mm

FX019P 16-pin plastic DIL (P3)

NOT TO SCALE



Max. Body Length 19.24mm
Max. Body Width 6.41mm

Ordering Information

FX019DW 16-pin plastic S.O.I.C. (D4)

FX019P 16-pin plastic DIL (P3)

CML Semiconductor Products

PRODUCT INFORMATION

FX029 Dual Digitally Controlled Amplifier Array

Publication D/029/1 July 1994
Provisional Issue

Features

- 2 Digitally Controlled Amplifiers
- Gain/Attenuation Range of ±48dB + Output Mute, in 2dB Steps
- Gain/Attenuation Levels Set by Serial Interface
- Separate Fixed-Gain Uncommitted Amplifier
- 5 Volt Low-Power Operation

Applications

- Cellular and PMR Communications Systems
- Automatic and Manual Test Equipment
- Remote Gain Adjustments
- Telephone Audio Settings
- Medical Equipment
- Audio and Data Gain Setting Applications

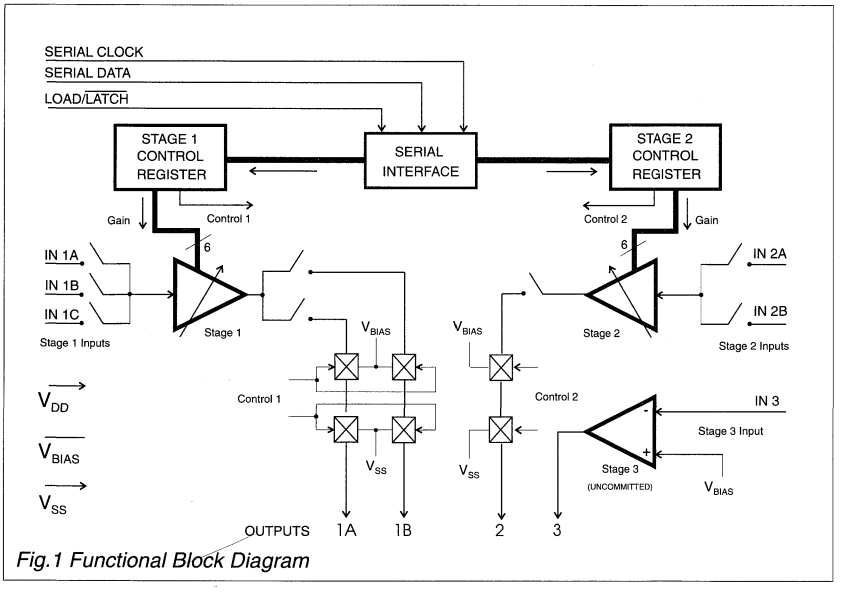


Fig.1 Functional Block Diagram

Brief Description

The FX029 single-chip Dual Digitally Controlled Amplifier Array can replace manual audio-level controls in most electronic applications including radio and line communications systems.

The FX029 comprises two digitally controlled gain and attenuation stages, with each stage having 48 distinct gain steps (range; between -48dB and +48dB in 2dB steps) plus a MUTE state to powersave the addressed section. Minimum current drain results from muting both sections.

Both gain stages have selectable inputs. This switching allows for selection of three different input signals to stage 1 and two to stage 2.

Stage 1 also provides output switching.

In addition to the two digitally controlled gain stages, there is a general purpose, uncommitted inverting amplifier; the gain of this particular amplifier is component controlled externally using negative feedback.

Control of each gain stage section is accomplished through the serial interface. All switching is accomplished using controlled rise and fall times, thereby ensuring no annoying transients (clicks or pops).

The FX029 requires a single 5 volt supply and is available in compact cerdip and small outline packages.

Pin Number FX029	Function
1	**Serial Clock:** This external clock input is used to "clock in" the control data. See Figure 4 for timing information. This input has an internal 1MΩ pullup resistor.
2	**Serial Data:** Operation of the two amplifier stages (1 and 2) is controlled by the data entered serially at this pin. The data is entered (bit 13 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1-3 and Figure 4. This input has an internal 1MΩ pullup resistor.
3	**Load/$\overline{\text{Latch}}$:** Governs the loading and execution of the serial control data. During serial data loading this input should be kept at a logical "1" to ensure that data rippling past the latches has no effect. When all 14 bits have been loaded this input should be strobed "1" to "0" to "1" to latch the new data in. Data is executed on the rising edge of this strobe.
4	**IN 1A** (Stage 1 Input 1): Analogue Input.
5	**IN 1B** (Stage 1 Input 2): Analogue Input.
6	**IN 2A** (Stage 2 Input 1): Analogue Input.
7	**IN 2B** (Stage 2 Input 2): Analogue Input.
8	**V_{SS}:** Negative supply rail (GND).
9	**V_{BIAS}:** The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} as shown in Figure 2.
10	**IN 1C** (Stage 1 Input 3): Analogue Input. Normally used for FSK data.
11	**OUT 2** (Stage 2 Output): Analogue Output.
12	**OUT 1A** (Stage 1 Output 1): Analogue Output.
13	**OUT 1B** (Stage 1 Output 2): Analogue Output.
14	**OUT 3** (Uncommitted Amplifier Output): Output from the general purpose uncommitted amplifier.
15	**IN 3** (Uncommitted Amplifier Input): Inverting input to general purpose uncommitted amplifier.
16	**V_{DD}:** Positive supply rail. A single +5-volt power supply is required.

Application Information

External Components

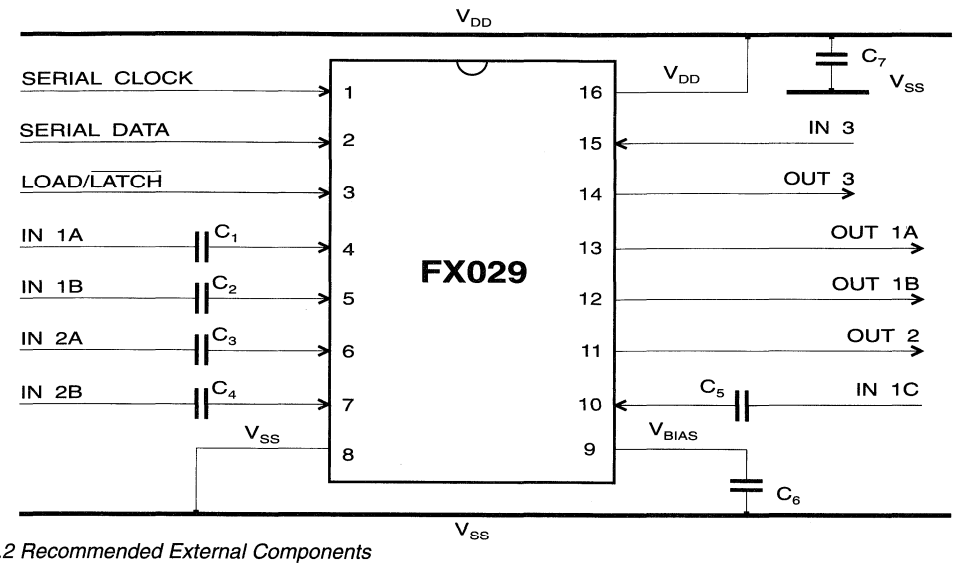


Fig.2 Recommended External Components

Component Recommendations

Component	Value
C_1	0.1mF
C_2	0.1mF
C_3	0.1mF
C_4	0.1mF
C_5	0.1mF
C_6	1.0mF
C_7	1.0mF

Tolerances 20%

Input capacitors C_1 to C_5 are only required for ac input signals; dc input signals do not require these components.

The gain of the uncommitted stage (3) is set by external components employed around the input and output pins (see Specification page).

Application Recommendations

To avoid noise and instability the following practices are recommended:

(a) Use a clean, well-regulated power supply.

(b) Keep tracks short.

(c) Inputs and outputs should be shielded wherever possible.

(d) Analogue tracks should not run parallel to digital tracks.

(e) A "Ground Plane" connected to V_{SS} will assist in eliminating external pick-up on the channel input and output pins.

(f) Avoid running high level outputs adjacent to low level inputs.

(g) The serial clock should not be running consecutively when not in the process of actually loading data.

Serial Interface Timing

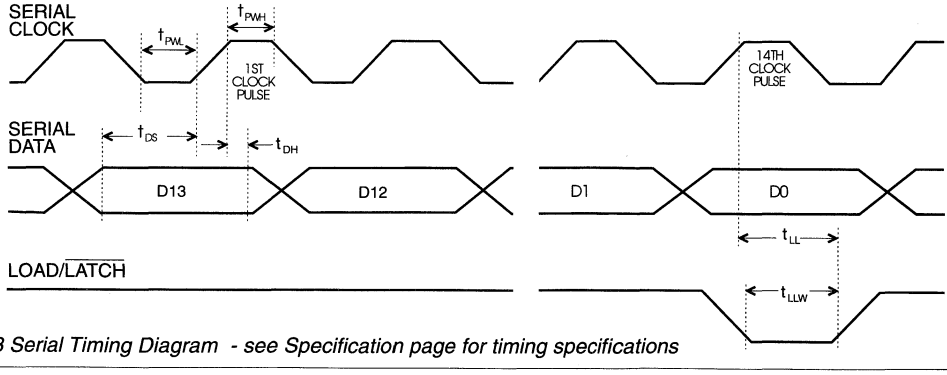


Fig.3 Serial Timing Diagram - see Specification page for timing specifications

Control Data and Timing

The gain and I/O signal path for each section (Channels 1 and 2) is set individually by a 14-bit data word (D0 to D13). Data is loaded on the rising edge of the Serial Clock. Loaded data is executed on the rising edge of the Load/ Latch pulse.The 14-bit word consists of 1 channel address bit (D7) for selection of the channel to be programmed, 6 bits for setting the amplification/attenuation level (D8-D13), 3 bits for input selection (D4 and D6), and 4 bits for output settings (D0-D3). This format is illustrated below in Figure 4.
Tables 1-3 show how the data word is used to control channel selection, amplification/attenuation, input selection and output settings, respectively.

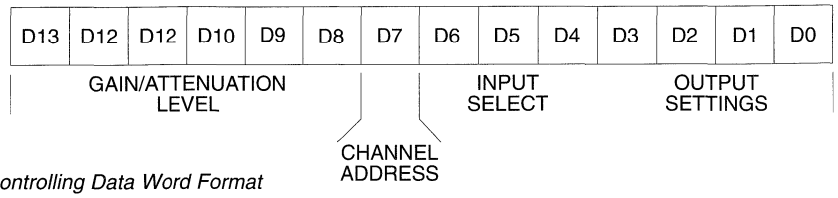


Fig.4 Level-Controlling Data Word Format

D13	D12	D11	D10	D9	D8	Gain Set (dB)	D13	D12	D11	D10	D9	D8	Gain Set (dB)
0	*0*	*0*	*0*	*0*	*0*	*MUTE*	*0*	*1*	*1*	*0*	*0*	*1*	*0*
0	0	0	0	0	1	-48	0	1	1	0	1	0	2
0	0	0	0	1	0	-46	0	1	1	0	1	1	4
0	0	0	0	1	1	-44	0	1	1	1	0	0	6
0	0	0	1	0	0	-42	0	1	1	1	0	1	8
0	0	0	1	0	1	-40	0	1	1	1	1	0	10
0	0	0	1	1	0	-38	0	1	1	1	1	1	12
0	0	0	1	1	1	-36	1	0	0	0	0	0	14
0	0	1	0	0	0	-34	1	0	0	0	0	1	16
0	0	1	0	0	1	-32	1	0	0	0	1	0	18
0	0	1	0	1	0	-30	1	0	0	0	1	1	20
0	0	1	0	1	1	-28	1	0	0	1	0	0	22
0	0	1	1	0	0	-26	1	0	0	1	0	1	24
0	0	1	1	0	1	-24	1	0	0	1	1	0	26
0	0	1	1	1	0	-22	1	0	0	1	1	1	28
0	0	1	1	1	1	-20	1	0	1	0	0	0	30
0	1	0	0	0	0	-18	1	0	1	0	0	1	32
0	1	0	0	0	1	-16	1	0	1	0	1	0	34
0	1	0	0	1	0	-14	1	0	1	0	1	1	36
0	1	0	0	1	1	-12	1	0	1	1	0	0	38
0	1	0	1	0	0	-10	1	0	1	1	0	1	40
0	1	0	1	0	1	-8	1	0	1	1	1	0	42
0	1	0	1	1	0	-6	1	0	1	1	1	1	44
0	1	0	1	1	1	-4	1	1	0	0	0	0	46
0	1	1	0	0	0	-2	1	1	0	0	0	1	48
0	*1*	*1*	*0*	*0*	*1*	*0*	1	1	0	0	1	0	48
							1	1	0	0	1	1	48

Table 1 - Amplification/Attenuation Level

D7	Stage Selected	D6	D5	D4	Inputs Selected
0	1	0	0	0	none
1	2	0	0	1	1
		0	1	0	2
		0	1	1	1 and 2
		1	0	0	3
		1	0	1	1 and 3
		1	1	0	2 and 3
		1	1	1	1, 2 and 3

Table 2 Stage and Input Selection

D3	D2	Output 1B	D1	D0	Outputs 1A & 2
0	0	high Z	0	0	high Z
0	1	enabled	0	1	enabled
1	0	V_{SS}	1	0	V_{SS}
1	1	V_{BIAS}	1	1	V_{BIAS}

Table 3 Stage Output Selection

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref. V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating temperature range: **FX029DW/J**	-40°C to +85°C
Storage temperature range: **FX029DW/J**	-55°C to +125°C

Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:
V_{DD} = 5.0V, T_{AMB} = 25°C. External components as Figure 2. Audio 0dB ref. = 775mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Voltage		4.5	5.0	5.5	V
Current (All Stages Mute)		-	0.10	-	mA
(All Stages Operating)		-	3.0	-	mA
Digital Inputs	4				
Input Logic "1"		3.5	-	-	V
Input Logic "0"		-	-	1.5	V
Digital Input Impedances		0.5	1.0	-	MΩ
Gain Control Amplifier Stages (Stages 1 and 2)					
Bandwidth (-3dB)	1	3.3	-	-	kHz
Output Impedance		-	1.0	2.0	kΩ
Total Harmonic Distortion	2	-	0.35	0.5	%
Interstage Isolation		-	60.0	-	dB
Gain		46.0	48.0	-	dB
Attenuation		46.0	48.0	-	dB
Gain/Attenuation Step Size		-	2.0	-	dB/step
Step Error		-	-	0.4	dB
Input Impedance		50.0	-	-	kΩ
Input Referred Offset Voltage (V_{IOS})		-	10.0	-	mV
Uncommitted Amplifier (Stage 3)					
Bandwidth (-3dB)	3	10.0	-	-	kHz
Output Impedance		-	1.0	2.0	kΩ
Total Harmonic Distortion	3	-	0.35	0.5	%
Open Loop DC Gain		-	60	-	dB
Timing (See Figure 3)					
Serial Clock "High" Pulse Width (t_{PWH})		250	-	-	ns
Serial Clock "Low" Pulse Width (t_{PWL})		250	-	-	ns
Data Set-up Time (t_{DS})		150	-	-	ns
Data Hold Time (t_{DH})		50.0	-	-	ns
Load/Latch Set-up Time (t_{LL})		250	-	-	ns
Load/Latch Pulse Width (t_{LLW})		150	-	-	ns
Serial Data Clock Frequency		-	-	2.0	MHz

Notes

1. Gain set to maximum (+48.0dB).
2. Gain Set 0dB. Input Level 1.0kHz, -3.0dB (549mVrms).
3. Gain externally set to 10.0dB.
4. Serial Clock, Serial Data and Load/Latch inputs.

Package Outlines

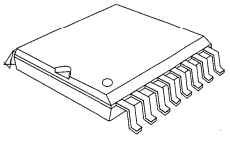
The FX029 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX029 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX029DW 16-pin plastic S.O.I.C. (D4)

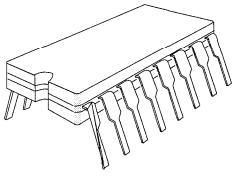
NOT TO SCALE



Max. Body Length	10.31mm
Max. Body Width	7.59mm

FX029J 16-pin cerdip DIL (J2)

NOT TO SCALE



Max. Body Length	19.48mm
Max. Body Width	7.40mm

Ordering Information

FX029DW 16-pin plastic S.O.I.C. (D4)

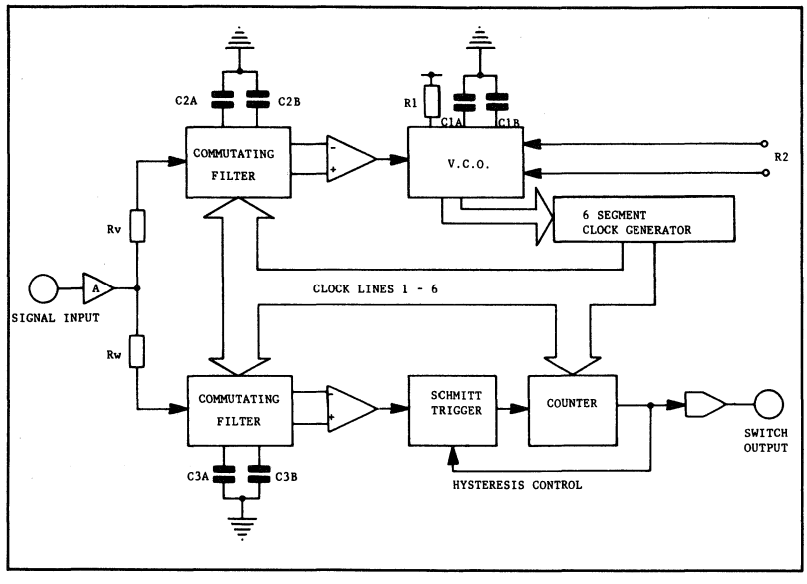
FX029J 16-pin cerdip (J2)

CML Semiconductor Products

PRODUCT INFORMATION

FX105P Tone Detector

Publication D/105/4 July 1994



FX105P

FEATURES

- OPERATES IN HIGH NOISE CONDITIONS
- ⩾40dB SIGNAL INPUT RANGE
- SIMULTANEOUS TONE DETECTION
- ADJUSTABLE BANDWIDTH
- HERMETICALLY SEALED CERAMIC PACKAGE
- WIDE FREQUENCY RANGE

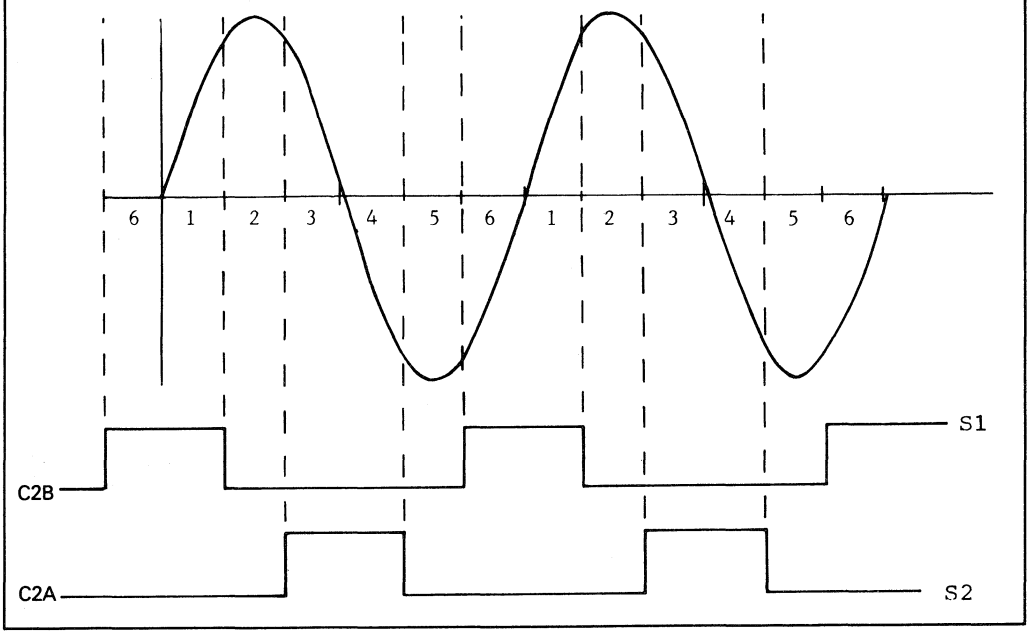
DESCRIPTION

The FX-105 is a monolithic tone operated switch, designed for tone decoding in single and multitone signalling systems.

The device employs decoding techniques which allow tones to be recognised in the presence of high noise levels or strong adjacent channel tones.

Tone channel centre frequency and channel bandwidth can each be adjusted independently. The circuit has a high noise immunity against harmonic and sub-harmonic responses and is able to maintain a constant bandwidth and high noise immunity over a wide range of input signal levels.

V.C.O. SAMPLING WAVEFORMS FIG. 2



METHOD OF OPERATION

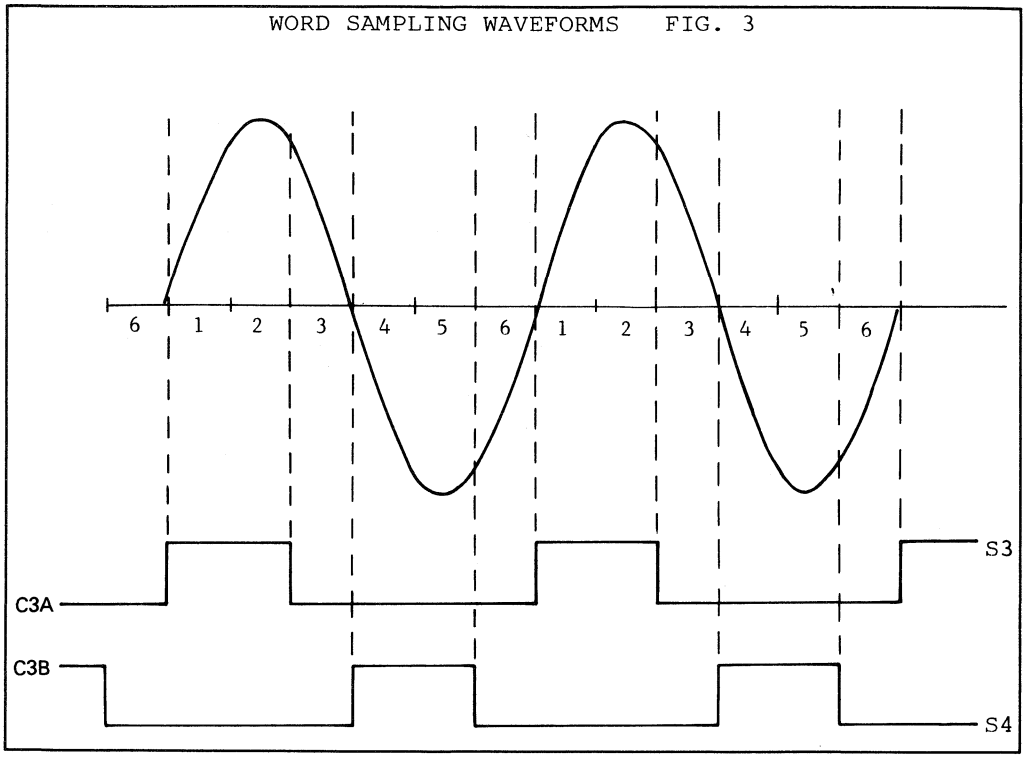
Input signals are A.C. coupled to the buffer input, which is internally biased at 50% of supply voltage, the signal appears at the output of the buffer as an A.C. voltage superimposed on the D.C. bias level. The signal is then coupled via RV and RW to the voltage controlled oscillator and word sampling switches, which sequentially connect C2 and C3 into circuit to form four sample and hold RC integrators.

With no input signal, each capacitor charges to the D.C. bias level and differential voltages are zero. When an input signal is applied, each capacitor receives an additional charge according to the integrated average of the signal waveform during the interval the capacitor is switched into circuit.

Figure 2 above shows the operating sequence of the V.C.O. sampling switches and their phase relationship to a locked on inband signal. As can be seen from Figure 2 C2A and C2B should not receive any additional charge as they always sample the input as it crosses the D.C. bias level. Should the signal not be locked to the V.C.O. then a positive or negative charge voltage will appear on C2A or C2B, this voltage when differentially amplified is applied to the V.C.O. as an error correcting signal to enable the V.C.O. to achieve lock.

Figure 3 shows the operating sequence of the 'Word' sampling switches and their relationship to a locked on inband signal. As can be seen from Figure 3 the charge being applied to C3A should always be positive and the charge applied to C3B should always be negative with respect to the common bias level.

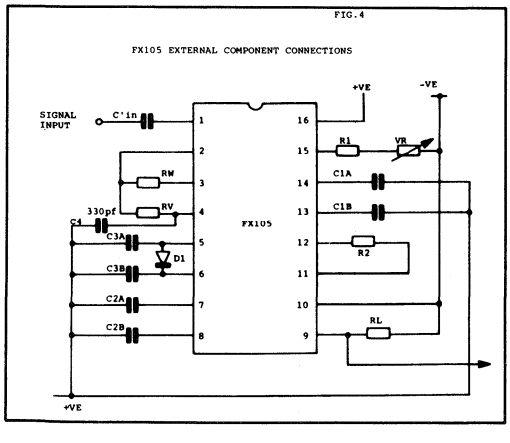
These capacitor potentials are differentially amplified and applied to a D.C. comparator, which switches at a predetermined threshold voltage. The comparator output is a logic signal used to control a counter which switches the FX-105 output ON when the comparator output is maintained in the 'Word Present' state for a minimum number of consecutive signal samples. The output switch reduces the comparator threshold by 50% when turned on, thereby introducing threshold hysterises which minimises output chatter with marginal input signal amplitudes.



METHOD FOR CALCULATING EXTERNAL COMPONENT VALUES

The external components shown below in Figure 4 are used to adjust the various performance parameters of the FX-105. The signal to noise performance, turn on delay and signal bandwidth are all interrelated factors which should be optimised to meet the requirements of the application.

By selecting component values in accordance with the following graphs nominally optimum circuit performance is obtained for any given application.



The user should first define the following application parameters.

A. The centre frequency to be detected (f'o).

B. The FX-105 Minimum Usable Bandwidth (MUBW). This is obtained by taking into account the worst case tolerances on the input tone frequency and variations in the FX-105 f'o due to supply voltage (0.07%/%) and ambient temperature (0.02%/°C) changes.

C. The maximum permissible FX-105 response time.

D. The minimum input signal amplitude.

Using this information the appropriate component values can be calculated, and the signal to noise performance obtained may then be read from a chart.

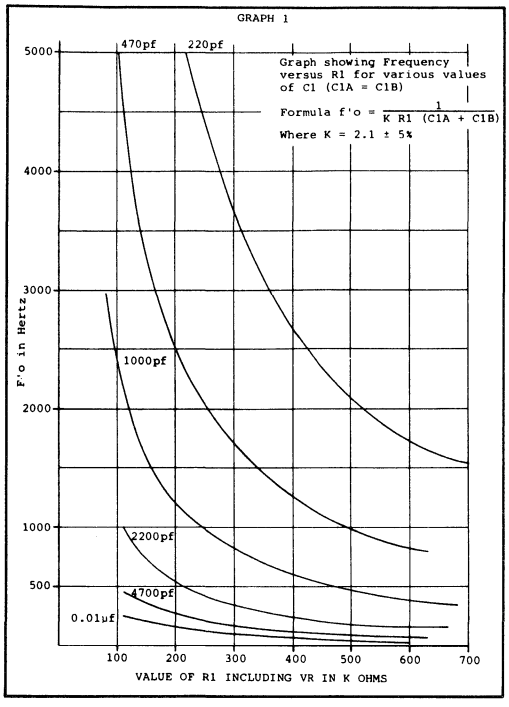
Using the graphs overleaf the following worked example may be used to calculate component values for any given application.

A. FX-105 centre band frequency (f'o) = 2800Hz.

B. FX-105 bandwidth = 6%.

C. FX-105 maximum response time = 50ms.

D. Minimum input signal amplitude = 200mVolts R.M.S.



R1 C1A C1B

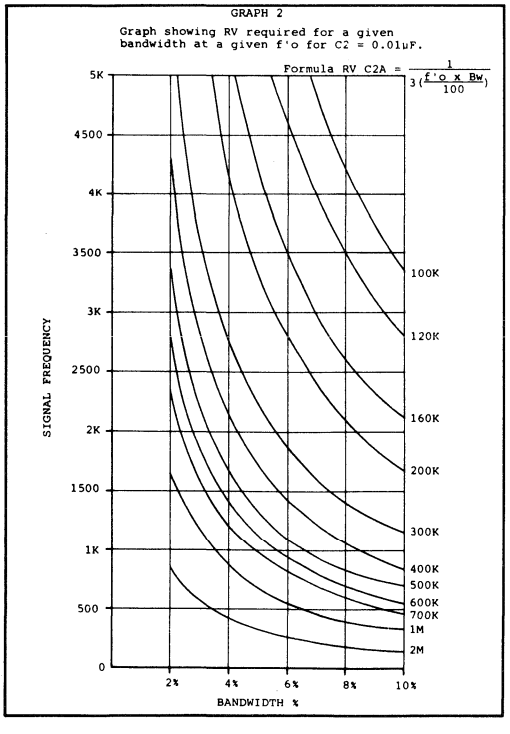
These components set the free running frequency of the V.C.O. and thereby the centre band frequency of the FX-105.

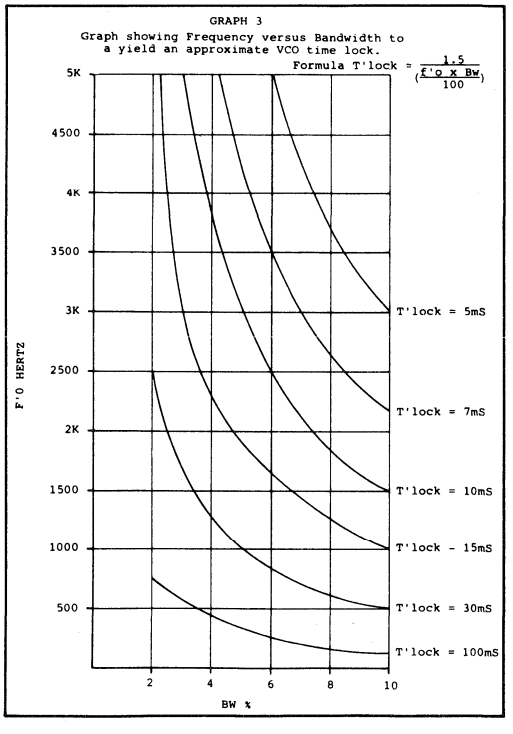
By using graph number 1 the frequency 2800Hz can be seen to correspond to a value of capacitor of 220 picofarads and a resistor value of 385k ohms, this resistance can be achieved with a 300k ohm fixed resistor for R1 and a 100k ohm potentiometer.

Graph number 2 shows that for a frequency of 2800Hz and a bandwidth of 6% a resistor RV of 200k ohms and a capacitance for C2A and C2B of 0.01 microfarads will be required.

The response time of the FX-105 is the sum of the V.C.O. 'Lock' time (T'lock) and the 'Word' integration time (T'word).

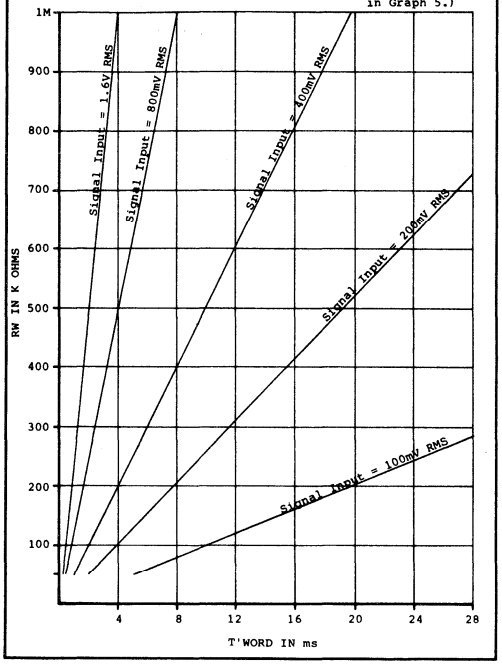
Graph number 3 shows that for a frequency of 2800Hz and a bandwidth of 6% the approximate 'Lock' time will be 9 milliseconds, as we have a maximum response time of 50 milliseconds, this allows for a 'Word' time of 41 milliseconds.





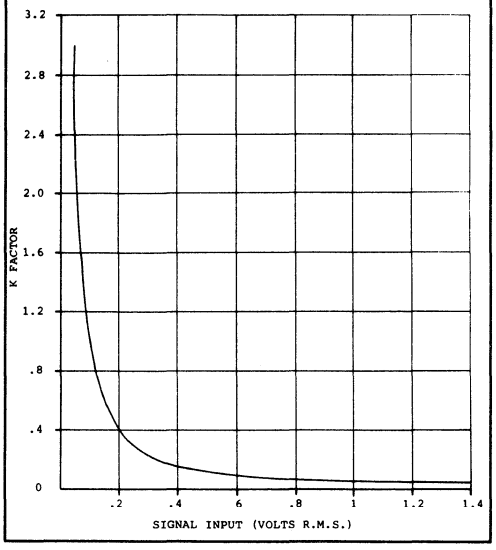
GRAPH 4

Graph showing RW required for T'word for a given signal input assuming C3A = C3B = 0.1μF. Formulae T'word = RwC3A x K(given in Graph 5.)



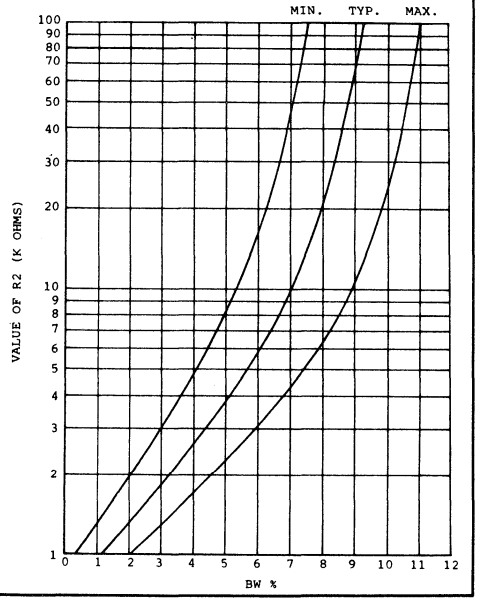
GRAPH 5

GRAPH SHOWING K FACTOR VS SIGNAL INPUT AMPLITUDE.



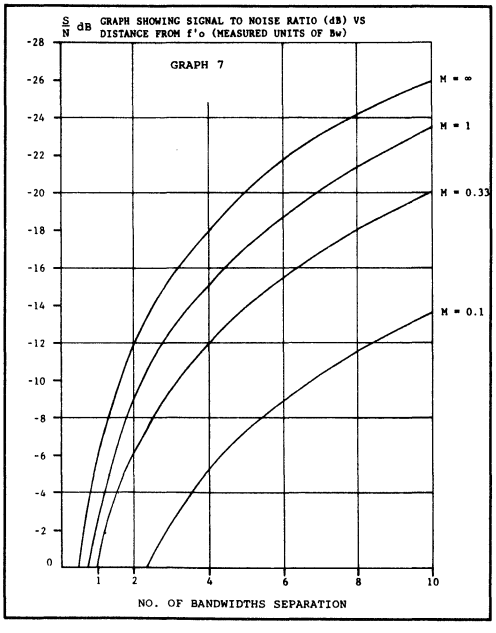
GRAPH 6

GRAPH SHOWING VALUE OF R2(KΩ) TO YIELD SELECTED BANDWIDTH(%)



GRAPH 7

GRAPH SHOWING SIGNAL TO NOISE RATIO (dB) VS DISTANCE FROM f'o (MEASURED UNITS OF Bw)



Graph number 4 shows that for a signal amplitude of 200mVolts, a resistor value RW of 510k ohms with a 0.1 microfarad capacitor for C3A and B will yield a 'Word' time of 20ms. This will yield a response time of 9ms + 20ms = 29ms.

Graph 6 shows the range of values for R2 to yield a given bandwidth. The exact bandwidth given by any value of R2 will vary with differing production batches, therefore in applications where an exact bandwidth is required R2 should be a variable resistor which is adjusted on test.

To calculate the worst case signal to noise ratio the FX-105 will work with the above component values. The formula is as follows:

$$M = \frac{f'o \times Bw}{100} \times (Rw\ C3A)$$

$$\therefore M = \frac{2800 \times 6}{100} \times (0.51M\Omega \times 0.1\mu F)$$

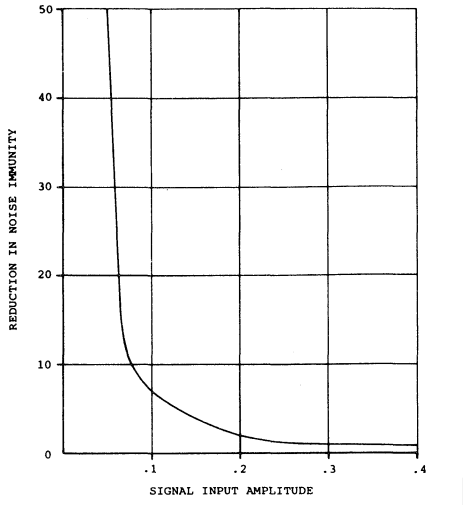
$$\therefore M = 168 \times 0.051$$

$$\therefore M \simeq 8.57$$

By substituting the value for M of 8.57 in graph number 7 the signal to noise ratio of an adjacent tone can be found, this then has to be decreased depending upon the tone amplitude. The figure to decrease SNR by is given in graph 8.

Graphs 9 and 10 show the approximate time the FX-105 will take to turn off after an inband signal has been removed. The turn off time is calculated with a diode (1N914 or similar) between pins 5 and 6 as shown in Figure 4. The effect of this diode is to greatly reduce the turn off time with signal input amplitudes greater than 300mV R.M.S.

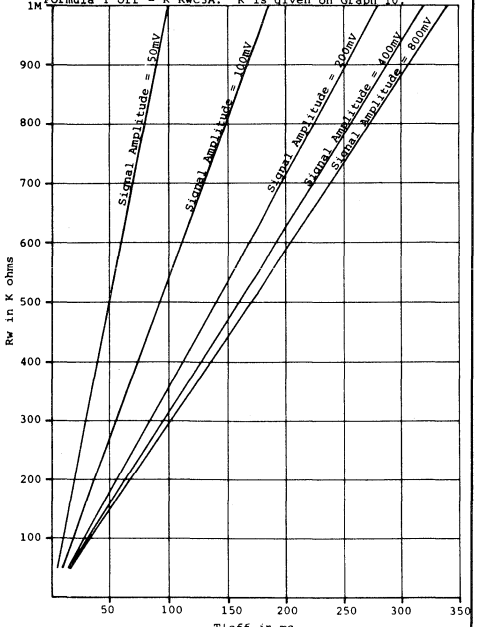
GRAPH 8



GRAPH 9

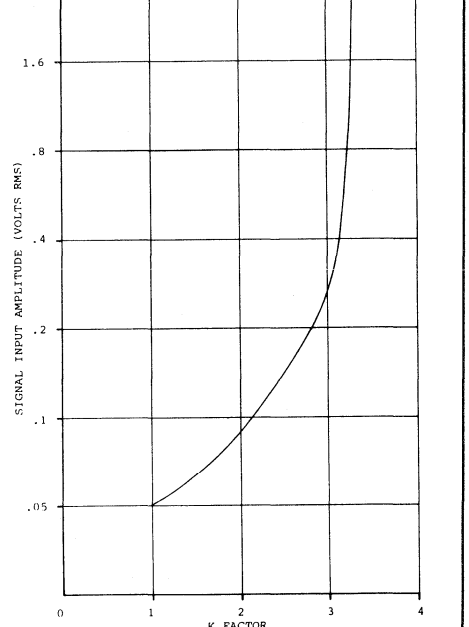
Graph showing T'off time for a given Signal Amplitude C3 = 0.1μF and Diode D1 between C3A & C3B.

Formula T'off = K RwC3A. K is given on Graph 10.



GRAPH 10

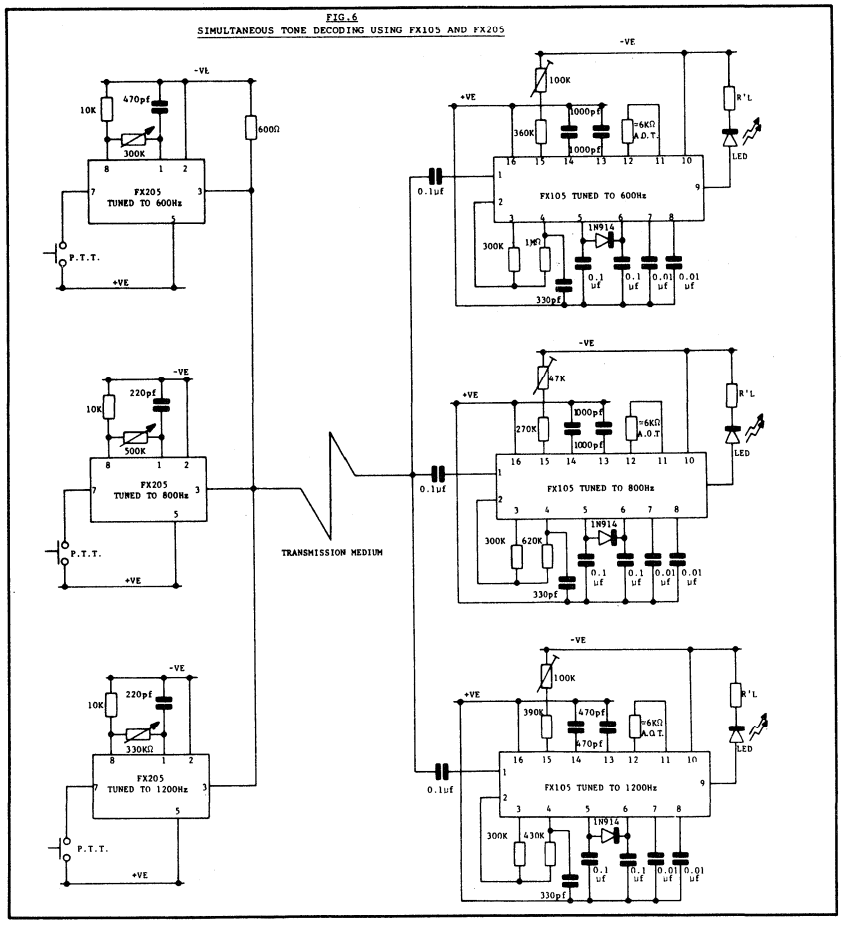
Graph showing 'K' factor for T'off vs Signal Input Amplitude (volts RMS).



FX105P Pin Functions

1	Signal Input	**9**	Switch Output
2	Buffer Output	**10**	V_{DD}
3	RW	**11**	HI
4	RV	**12**	LO
5	C3A	**13**	C1B
6	C3B	**14**	C1A
7	C2A	**15**	RI
8	C2B	**16**	V_{SS}

Due to the FX105's ability to decode tones in the presence of adjacent channel tones or noise, the device is ideally suited to applications where a number of tones are sequentially or simultaneously transmitted over a common link.
In the example shown below, a number of single-tone transmitters are transmitting over a common link (such as cable, radio or optical) to a number of FX105P receivers. The transmitters may transmit either individually or simultaneously without the FX105P receivers missing or receiving a false call.



Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Input voltage between any pin and +ve supply	-20V and +0.3V
Total device dissipation @ T_{AMB} 20°C	400mW Max.
Operating temperature range: **FX105P**	-30°C to +85°C
Storage temperature range: **FX105P**	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 12.0V, T_{AMB} = 20°C. Due to ac signal coupling either supply may be 'ground'.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		10.0	12.0	15.0	V
Supply Current	1	-	5.0	-	mA
Input Impedance		-	200	-	kΩ
Signal Input	2, 3	0.055	-	5.0	V rms
Channel Frequency		0.04	-	5.0	kHz
Bandwidth		2.0	-	10.0	%
Output Switch Load Current		-	-	10.0	mA
Frequency Stabilty (with temperature)		-	0.02	-	$\%/^{\circ}C$
Frequency Stabilty (with supply voltage)		-	0.07	-	$\%/V$

Notes

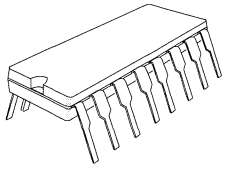
1. Supply current excluding load. Note maximum switch load current.
2. Signal-plus-noise range.
3. For signal input voltages greater than V_{DD} x 0.143, pins 1 and 2 should be open circuit and the signal applied via C_{IN} to the junction of RV and RW.

Package Outlines

The FX105P is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX105P 16-pin plastic DIL (P3)

NOT TO SCALE



Max. Body Length 19.24mm
Max. Body Width 6.41mm

Handling Precautions

The FX105P is a PMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

Ordering Information

FX105P 16-pin plastic DIL (P3)

CML Semiconductor Products

PRODUCT INFORMATION

FX326 Audio Bandpass Filter

Publication D/326/4 July 1994

Features/Applications

- 300Hz – 3000/3400Hz Audio Bandpass Filter
- Low Group Delay Distortion
- On-Chip Uncommitted Amplifier
- Range of Usable Xtal/Clock Frequencies
- Switched Capacitor Filters
- Chip Enable Powersave Feature
- Plastic DIL and SMD Packages
- General Purpose Audio Filtering
- Mobile and Portable Radio
- Data Signalling – Modems
- Portable Audio Equipment
- Delta and PCM Audio Filtering
- Cordless Telephones and Intercoms
- PABX and Trunk Equipment

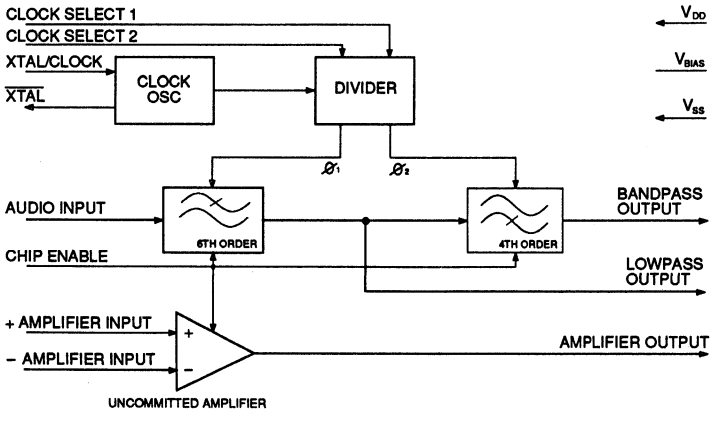


Fig.1 Internal Block Diagram

Brief Description

The FX326 is a general purpose low-power CMOS switched capacitor audio bandpass filter.
The filter frequency response is clock related and with the pin programmable divider allows for standard (300Hz - 3000/3400Hz) or non-standard frequency responses.

The device in detail consists of:

(1) A 6th order low group delay distortion lowpass filter.
(2) A 4th order highpass filter.
(3) An uncommitted amplifier.
(4) On-chip clock circuitry.

The two filters are connected in series, thus providing an audio bandpass filter output, the lowpass filter output may be used independently.

An on-chip oscillator requiring a Xtal, resonator or external clock pulse input provides all reference clocks for the switched capacitor filters. The two clock select lines (S1, S2) enable the device to be used with various clock frequencies without significantly altering the filter response. Additionally the clock select inputs provide the facility to shift the filter cut-off frequencies, allowing non-standard bandpasses and lowpasses to be produced. The chip enable input, when a logic '0,' will disable the filter and amplifier sections, thus reducing current consumption. The uncommitted amplifier may be used for any specific application such as pre-emphasis, de-emphasis, buffering, gain, etc. The FX326 Audio Bandpass Filter is available in 14-pin Plastic DIL and 24-pin SMD packages.

Pin Number		Function
Quad FX326LG	DIL FX326P	
1	1	V_{DD} : Positive supply rail. A single +5 volt power supply is required.
2	2	**Select 2** (S2) : Control inputs to the clock programmable divider. The configuration of these inputs selects a division ratio (n), which with the input clock frequency (f_C) is used to select either the *upper* (f_H) or *lower* (f_L) filter cut-off frequency. The division ratio (n) is achieved
3	3	**Select 1** (S1) : using S1 and S2 as shown in the following table :

S1	S2	n
0	0	10
0	1	6
1	0	20
1	1	12

The lower (-3dB) cut-off frequency (f_L) and the upper (-3dB) cut-off frequency (f_H) are calculated using the formulas described below.

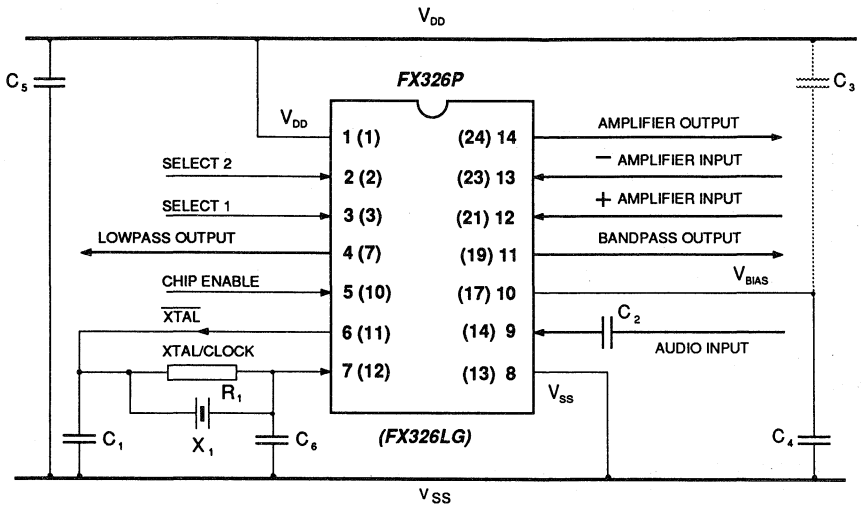
$$f_L = \frac{2.5 \times f_C}{n} \qquad f_H = \frac{34 \times f_C}{n}$$

where : f_L and f_H are calculated in Hz.
f_C is the Clock Frequency in kHz.
n is the Division Ratio set by inputs S1 and S2.

Inputs S1 and S2 each have internal 1MΩ pulldown resistors (n = 10).

7	4	**Lowpass Output :** The audio output of the lowpass filter section whose upper cut-off frequency (-3dB) is determined by the input clock frequency (f_C) and the selection control inputs, S1 and S2, see Figure 5. This output is internally biased to V_{BIAS}.
10	5	**Chip Enable :** Internally pulled to V_{DD} (logic'1') - enabling this device. A logic '0' applied to this pin will disable all filters and the uncommitted amplifier, putting the device into powersave to reduce current consumption.
11	6	$\overline{\text{Xtal}}$: Output of the clock oscillator inverter. The clock oscillator remains powered in powersave. See Figure 2 (circuitry).
12	7	**Xtal/Clock :** The input to the clock oscillator inverter. A Xtal, resonator or externally derived clock pulse (f_C) is applied to this input. The clock frequency (f_C), with selection control inputs S1 and S2 will determine the upper and lower (-3dB) filter cut-off frequencies. See Figures 2, 3, 4 and 5.
13	8	V_{SS} : Negative supply rail (GND).
14	9	**Audio Input :** The input to the Lowpass/Bandpass filters. This input should be a.c. coupled using capacitor C_2, see Figure 2.
17	10	V_{BIAS} : The output of the on-chip analogue bias circuitry, held at $V_{DD}/2$. Remains at V_{BIAS} during powersave. This pin requires to be decoupled to V_{SS} by capacitor C_4, see Figure 2.
19	11	**Bandpass Output :** The audio bandpass output, whose upper and lower cut-off frequencies (-3dB) are determined by the input clock frequency (f_C) and the selection control inputs, S1 and S2.
21	12	**Amplifier Input (+ve) :** The uncommitted amplifier non-inverting input.
23	13	**Amplifier Input (-ve) :** The uncommitted amplifier inverting input.
24	14	**Amplifier Output :** The output of the uncommitted amplifier.
4,5,6, 8,9,15,16, 18,20,22.		No internal connection, do not use.

Application Information



Component	Value	Note	Component	Value	Note
R_1	1MΩ	1	C_4	0.1μF	2
C_1	33pF	1	C_5	0.1μF	
C_2	0.1μF		C_6	33pF	1
C_3	0.1μF	2	X_1	Xtal/Resonator	3

Tolerances : R = 10%. C = 20%.

Notes

1. Xtal/Clock components shown are in accordance with CML application note D/XT/1 April 1986. This input can be either a Xtal/Resonator circuit as shown, or a clock 'pulse' input.
2. V_{BIAS} may be decoupled to V_{SS} and V_{DD}. For input signals referenced to V_{SS}, decouple V_{BIAS} to V_{SS} using C_4 only.
3. Xtal/clock frequencies are dependant upon required filter responses – Table 1, Figures 4 and 5.

Fig.2 Recommended External Component Connections

Table 1 shows the upper or lower cut-off frequencies that can be achieved with differing combinations of Clock Rate (f_C) and Division Ratio (n) using the formulas described on Page 2 (pins 2 and 3). Typical bandpass characteristics using a 1.0MHz clock are displayed in Figure 3.

Clock f_C *(kHz)*	Division Ratio n	Lower Cut-Off *(-3dB)* f_L *(Hz)*		Upper Cut-Off *(-3dB)* f_H *(Hz)*	Bandwidth *(Hz)*
560	6	233	–	3173	2940
	10	140	–	1904	1764
	12	116	–	1586	1470
	20	70	–	952	882
1000	6	416	–	5666	5250
	10	250	–	3400	3150
	12	208	–	2833	2625
	20	125	–	1700	1575
1500	6	625	–	8500	7875
	10	375	–	5100	4725
	12	312	–	4250	3938
	20	187	–	2550	2363
2000	6	833	–	11333	10500
	10	500	–	6800	6300
	12	416	–	5666	5250
	20	250	–	3400	3150
2500	6	1041	–	14166	13125
	10	625	–	8500	7875
	12	520	–	7083	6563
	20	312	–	4250	3983

Table 1 Examples of Upper and Lower Cut-Off Frequencies

Application Information

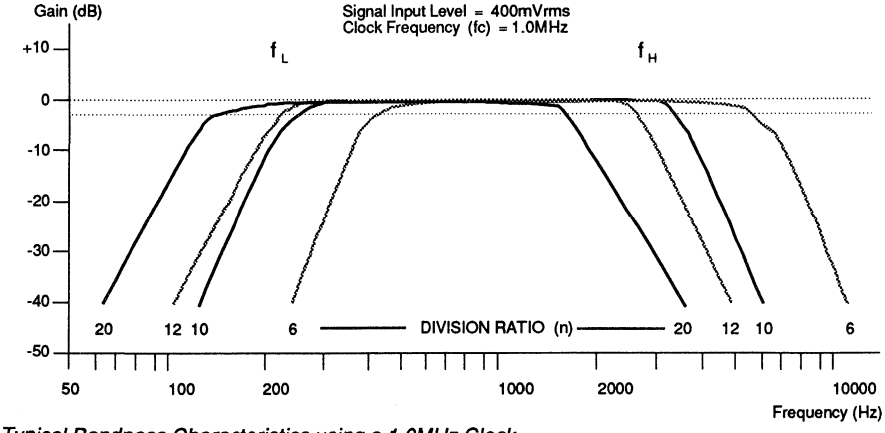


Fig. 3 Typical Bandpass Characteristics using a 1.0MHz Clock

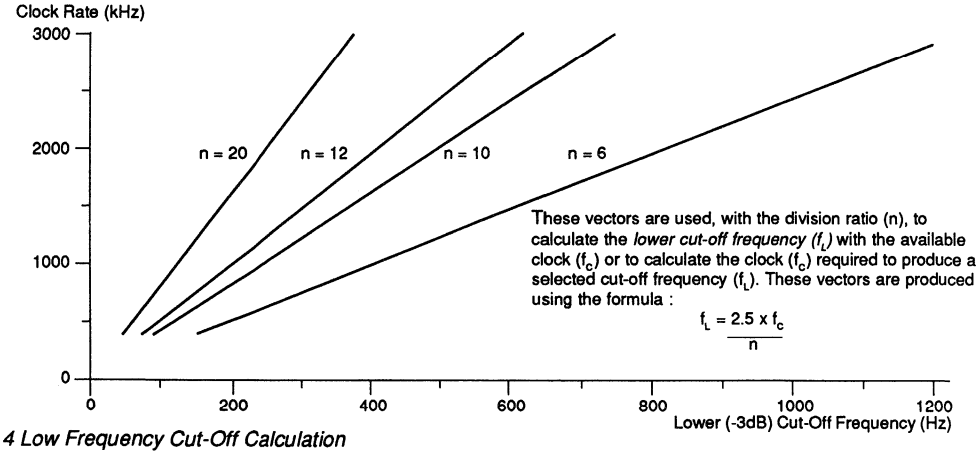


Fig. 4 Low Frequency Cut-Off Calculation

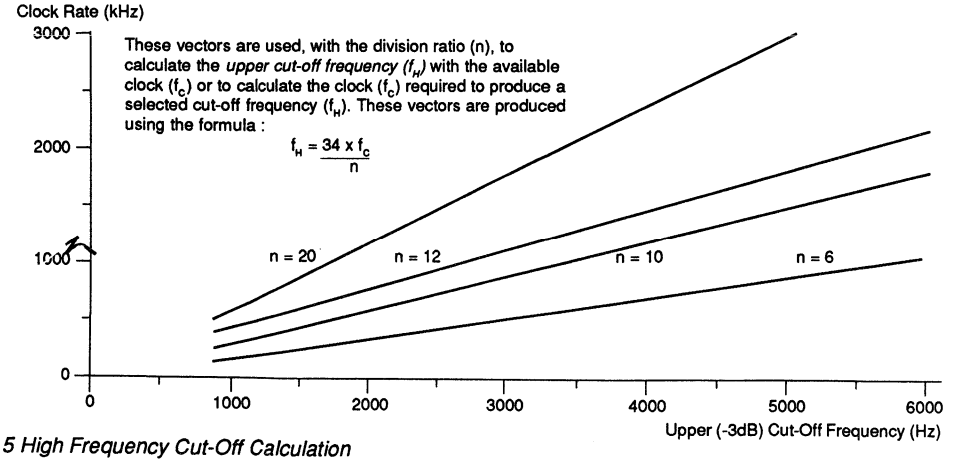


Fig. 5 High Frequency Cut-Off Calculation

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating temperature range: **FX326LG/P**	-30°C to +70°C
Storage temperature range: **FX326LG/P**	-40°C to +85°C

Operating Limits

All device characteristics are measured using the following parameters unless otherwise specified :

V_{DD} = 5.0V, T_{AMB} = 25°C. Xtal/Clock f_c = 1.0 MHz. n = 10 *(S1 & S2 logic '0').* Audio level 0dB ref: = 400mV rms.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (Enabled)		–	3.5	–	mA
Supply Current (Powersave)		–	1.0	–	mA
Input Logic '1'		3.5	–	–	V
Input Logic '0'		–	–	1.5	V
Input Impedance					
Filters and Amplifier		100	–	–	kΩ
Logic		–	1.0	–	MΩ
Output Impedance					
Filters		–	3.0	–	kΩ
Amplifier – Open Loop		–	800	–	Ω
Amplifier – Closed Loop		–	6.0	–	Ω
Clock Oscillator Inverter					
R_{in}		–	10.0	–	MΩ
R_{out}		–	10.0	–	kΩ
Gain		–	15.0	–	dB
Gain Bandwidth Product		–	5.0	–	MHz
Clock Frequency (f_C) Limits	1	0.5	–	3.0	MHz
Dynamic Values					
Signal Input Range	2	–	0	8.0	dB
Output Noise Level	3	–	-48.0	–	dB
Insertion Loss	4	–	0	–	dB
Group Delay Distortion (300Hz – 3400Hz)	6	–	–	200	µs
Cut-off Frequency -3dB					
Lowpass - (f_H)		–	3400	–	Hz
Highpass - (f_L)		–	250	–	Hz
Stopband Attenuation					
f > 6kHz		–	47.0	–	dB
f < 200Hz		–	27.0	–	dB
Aliasing Frequency		–	f_C/2n	–	Hz
Uncommited Amplifier					
Open Loop Gain	5	–	30.0	–	dB
Gain Bandwidth Product		–	1.0	–	MHz

Notes

1. These frequency limits are those at which the High or Low cut-off frequencies are in accordance with the formulas described in Figures 4 and 5.
2. Upper figure gives 3% distortion in 30dB SINAD. Typical figure gives minimum distortion in maximum SINAD.
3. Measured at the Bandpass Output with the Audio Input a.c. short circuit.
4. Input frequency 1.0kHz.
5. Relative to 1.0kHz at 100mV rms input.
6. Reference frequency 800Hz. See Figure 7.

Application Information...

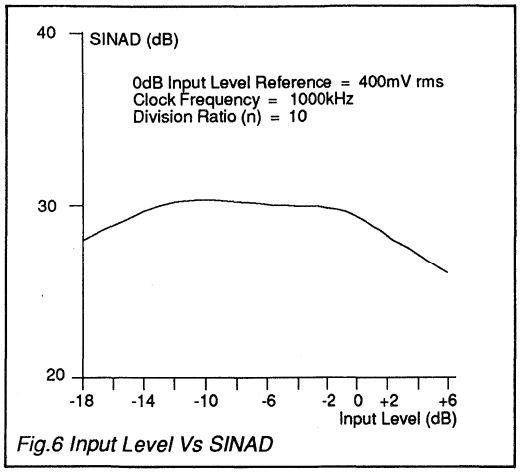


Fig.6 Input Level Vs SINAD

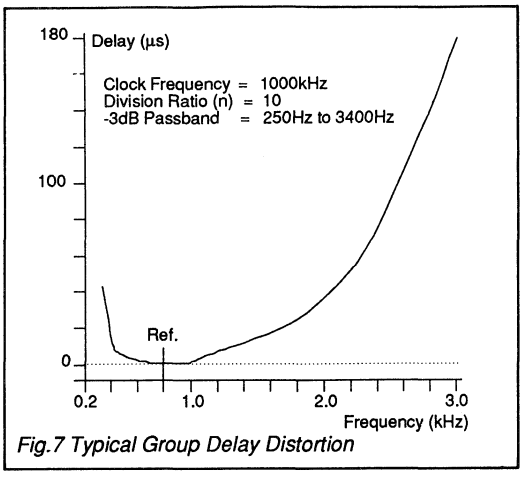


Fig.7 Typical Group Delay Distortion

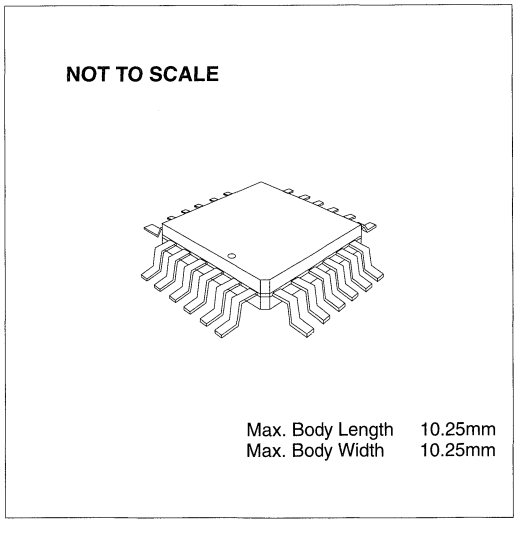
Package Outlines

The FX326 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

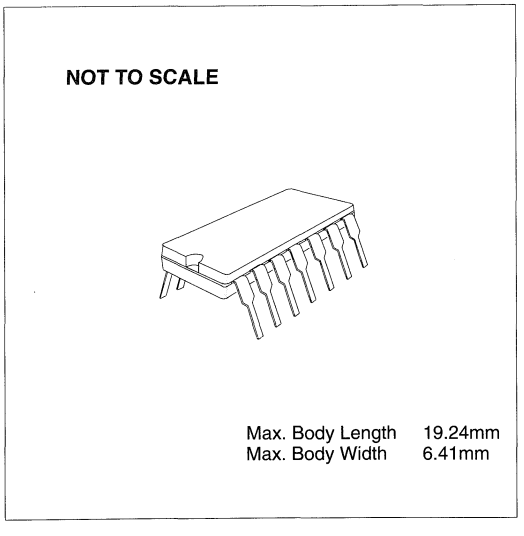
Handling Precautions

The FX326 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX326LG 24-pin plastic encapsulated bent and cropped (L1)



FX326P 14-pin plastic DIL (P2)



Ordering Information

FX326LG 24-pin plastic encapsulated bent and cropped (L1)

FX326P 14-pin plastic DIL (P2)

CML Semiconductor Products

PRODUCT INFORMATION

FX406 Unifil™ Universal Analogue Signal Processor

Publication D/406/7 July 1994

Features/Applications

- 2nd Order Multiple Filter
- PLL Clock Generator
- Programmable Q
- F_c set by RC or External Clock
- Gain Adjustment on Inputs
- Single 5 Volt Supply CMOS
- Programmable Filters
- Voltage Controlled Filters
- Sinewave Oscillator
- Tracking Filters/Oscillators
- FSK and PSK Modems
- Square-Sine, Pulse-Sine Converter

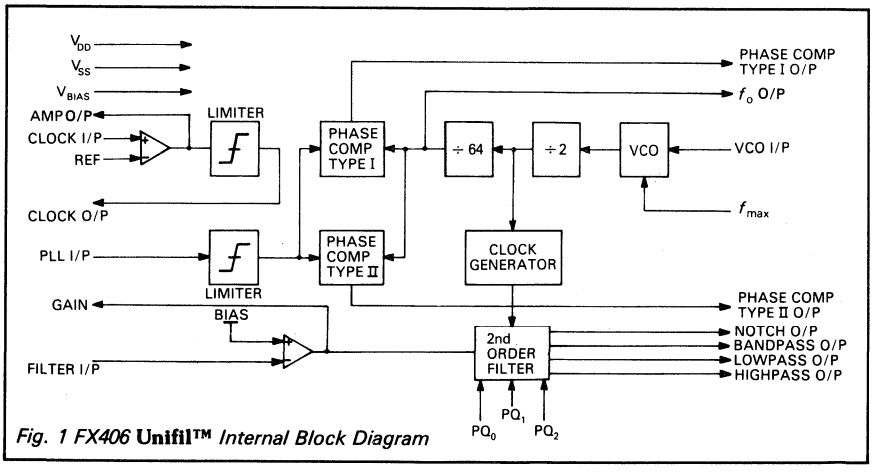


Fig. 1 FX406 **Unifil™** *Internal Block Diagram*

FX406

Brief Description

The FX406 **Unifil™** is a CMOS LSI circuit with a wide variety of signal processing applications. The device consists of a switched capacitor second order active filter with a single input and outputs for bandpass, notch, lowpass and highpass frequency responses, together with a clock generator to provide the switched capacitor sampling clock frequency. The centre frequency of the bandpass and notch filters is the same as the cut-off frequency f_c of the lowpass and highpass filters. The filter sampling clock is derived from a multiplying phase locked loop whose reference or input frequency is the same as the desired cut-off frequency of the filters. The PLL comprises a voltage controlled oscillator, one of two types of phase comparator, a fixed divider and an external RC loop filter. Facilities are provided to programme the cut-off frequency of the filters by injecting an external signal into the PLL, or by using the on-chip clock oscillator circuit. The filters have gain adjustment on the input and the Q is programmable to eight values between 0.54 and 8.0.

Pin Number FX406J	Pin Number FX406LG	Function
1	1	**PCI O/P:** Output of 'EXCLUSIVE-OR' type phase comparator. See Note on PLL operation.
2	2	**PLL I/P:** Input to limiter preceding phase comparators.
3	4	**f_o O/P:** Divided down VCO square wave output.
4	5	**PQ_2 I/P:** These pins set the Q of the filters; they have internal resistors to
5	6	**PQ^0 I/P:** set Q = 0.71 if left open circuit (logic state 1 0 1, = 1MΩ)
6	7	**PQ^1 I/P:** Possible Q values are:

PQ_2	PQ_1	PQ_0	Q	
1	1	1	0.54*	
1	1	0	0.58	(Bessel)
1	0	1	0.71	(Butterworth)
1	0	0	1.00	
0	1	1	1.31	
0	1	0	2.00	
0	0	1	4.00	
0	0	0	8.00	

* (Cascaded with a 1.31 section for a 4th order Butterworth filter).

7	8	**Clock O/P:** Digital output of limiter from uncommitted amplifier.
8	10	**Amp O/P:** Analogue output of uncommitted amplifier.
9	11	**Reference:** Inverting input to uncommitted amplifier.
10	12	**Clock I/P:** Non-inverting input to uncommitted amplifier.
11	13	**V_{SS} :** Negative supply.
12	14	**V_{BIAS} :** $V_{DD}/2$ bias pin, externally decoupled.
13	15	**Filter I/P:** Input to filter input buffer amplifier.
14	16	**Gain:** Output of filter input buffer amplifier.
15	17	**Highpass O/P:** Output of the highpass filter. The cut-off frequency is identical to the input frequency of the PLL when locked.
16	18	**Lowpass O/P:** Output of the lowpass filter. The cut-off frequency is the same as the highpass filter.
17	19	**Bandpass O/P:** Output of the bandpass filter. f_O is identical to the input frequency to the PLL when locked. Gain in passband is dependent on Q.
18	20	**Notch O/P:** Output of the notch filter, f_O, is the same as the bandpass filter.
19	21	**VCO I/P:** Input of the VCO control voltage, usually connected to loop filter output.
20	22	**f_{max} :** This pin is connected to V_{SS} via an external resistor R_{MAX} (R_{MAX}, see Figure7). The value sets the maximum frequency of operation of the VCO, see Figures 9(a) and (b).
21	23	**PCII O/P:** Output of the edge-triggered type of phase comparator. See Note on PLL operation.
22	24	**V_{DD} :** Positive supply.
	3, 9	No Connection: Leave open circuit.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	FX406J	−30°C to + 85°C
	FX406LG	−30°C to + 70°C
Storage temperature range:	FX406J	−55°C to +125°C
	FX406LG	−40°C to + 85°C
Maximum device dissipation:		All versions 100mW

Operating Limits

Typical characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5V, T_{amb} = 25°C, PLL input = 1kHz, filter Q = 0.707.
Limits specified over the full operating temperature and working voltage range.

Characteristics	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply voltage		4.5	5.0	5.5	V
Supply current		—	4.5	8.5	mA
Input impedance (Filter & Clock Osc)		1.0	—	—	MΩ
Output impedance (Filter Outputs)		—	—	1.0	kΩ
Output impedance (Clock Output)		—	—	1.0	kΩ
Input impedance (PQ_0, PQ_1, PQ_2)		250	—	—	kΩ
Output impedance (f_o output)		—	—	5.0	kΩ
Input logic '1'		70% V_{DD}	—	—	V
Input logic '0'		—	—	30% V_{DD}	V
Filter Characteristics					
Maximum cutoff frequency		4.0	5.0	—	kHz
Minimum cutoff frequency		—	50	100	Hz
Gain at f_c (f_o) (HP BP LP)		—	20 log Q	—	dB
Notch filter depth	1	—	−30	—	dB
Notch accuracy	1	—	±0.5% f_o	—	Hz
Maximum signal handling	2	3.0	—	—	Vp-p
No signal filter noise (BP)		—	6.0	—	mVrms
(LP HP N)		—	3.0	—	mVrms
VCO Characteristics					
VCO maximum frequency	3	4.0	5.0	—	kHz
VCO minimum frequency	3	—	50	100	Hz
VCO input impedance		1.0	—	—	MΩ
Phase Comparator Characteristics					
Input impedance		100	500	—	kΩ
Input sensitivity	4	30	10	—	mVrms
Output impedance PCII	5	—	—	1.5	kΩ
PCI		—	—	1.5	kΩ
Amplifier Characteristics (Clock Oscillator and Filter inputs)					
Open loop gain		40	—	—	dB
Input offset voltage		—	—	10	mV
Maximum signal handling	2	3.0	—	—	Vp-p

Notes: *1. Q = 8.*
2. For SINAD = 30dB at output.
3. VCO frequency divided down at f_o output.
4. At PLL input pin, ac coupled.
5. Output impedance when conducting, output is high impedance three-state when PLL is in lock.

Typical Filter Frequency Responses

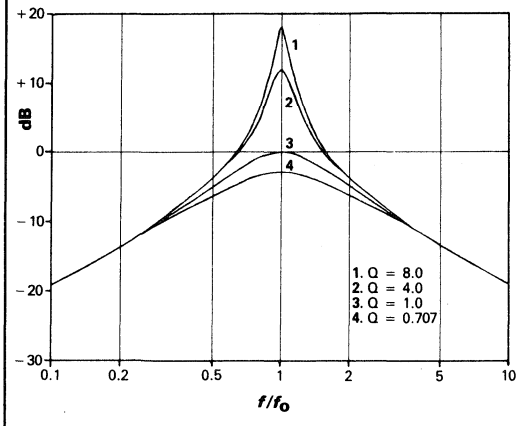


Fig. 2 Bandpass Frequency Response for different Q Values

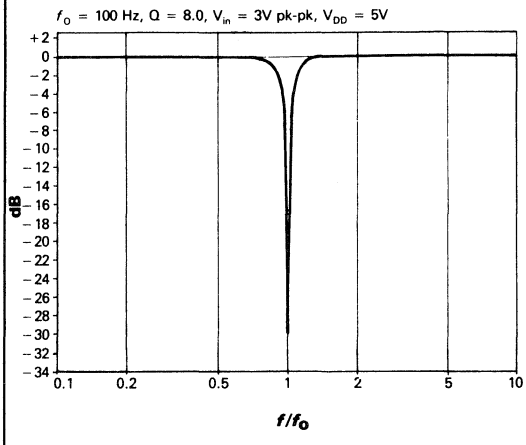


Fig. 3 Notch Frequency Response

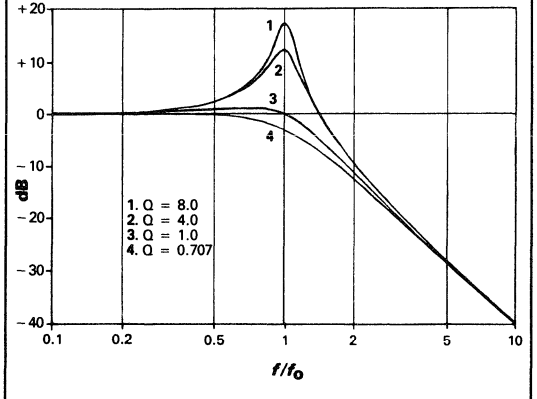


Fig. 4 Lowpass Frequency Response for different Q Values

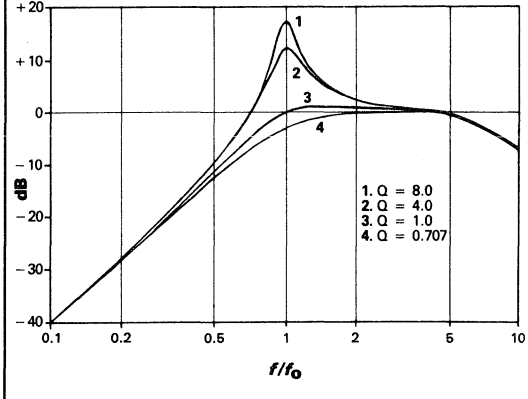


Fig. 5 Highpass Frequency Response for different Q Values

PC4060 PCB For Design Evaluation

To assist in customer's design evaluation of the FX406, a PCB is available to enable external components to be connected for easy evaluation of application circuits.

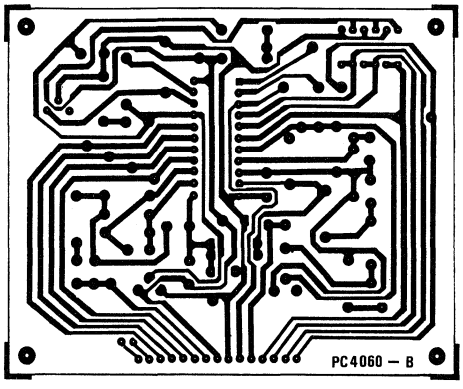


Fig. 6 (a) Track Side

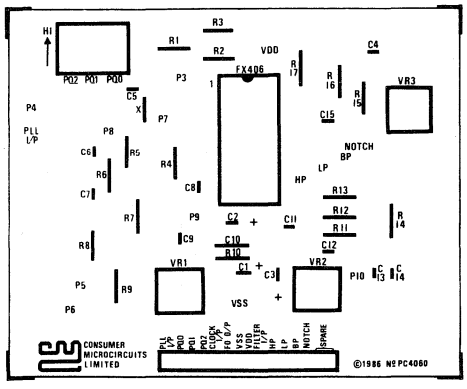


Fig. 6 (b) Component Side

Fig. 6 PC4060 Printed Circuit Board

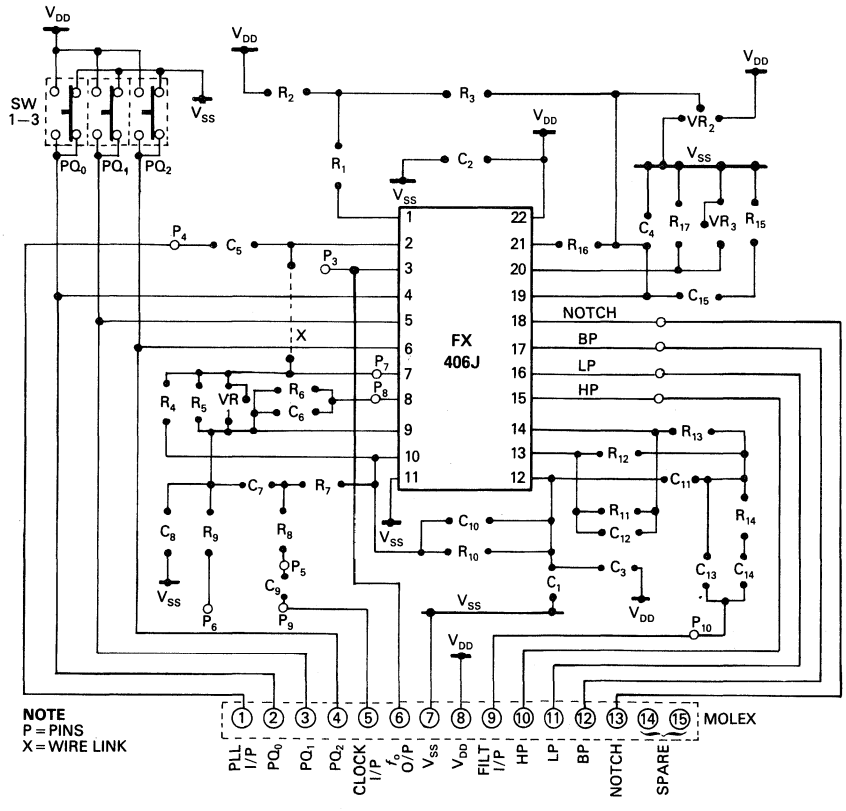


Fig. 6 (c) PC4060 Printed Circuit Board Schematic Diagram

External Component Connections

The following examples of external component connections illustrate the basic modes of operation of the FX406. Where component references are used, these are the same as the circuit references on the PC4060 Evaluation PCB.

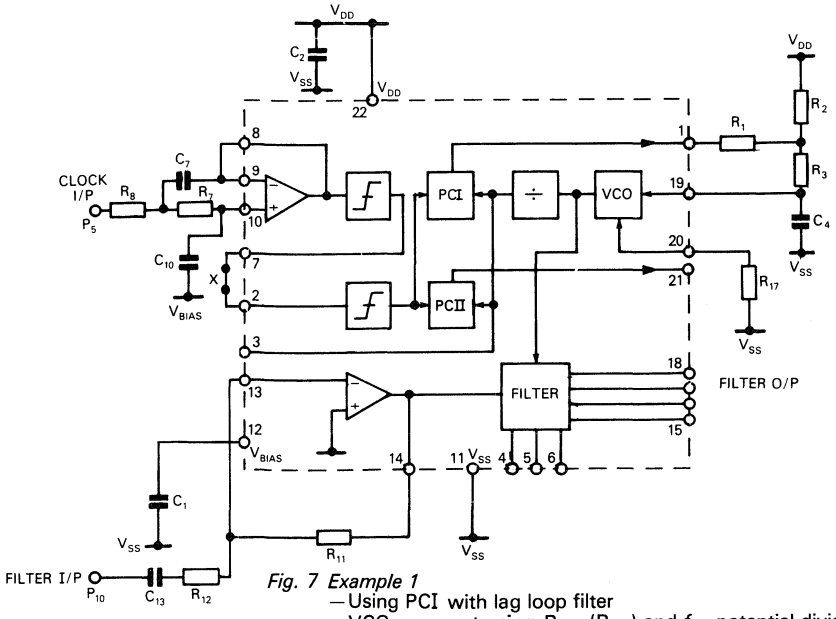


Fig. 7 Example 1

—Using PCI with lag loop filter
—VCO range set using R_{max} (R_{17}) and f_{min} potential divider (R_1, R_2)
—Filter input with simple gain adjustment
—Clock input pre-filtered with 2nd order LPF.

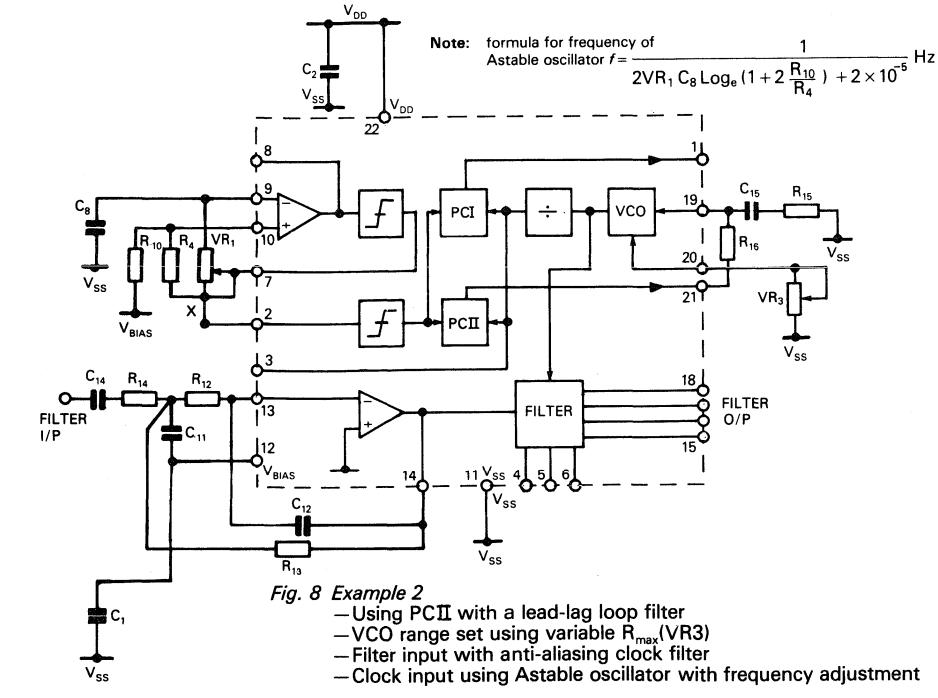


Fig. 8 Example 2

—Using PCII with a lead-lag loop filter
—VCO range set using variable R_{max}(VR3)
—Filter input with anti-aliasing clock filter
—Clock input using Astable oscillator with frequency adjustment

Application Notes

Note 1 — Setting VCO Frequency Range.

Set f_{max}* of VCO by selecting R_{max} using graph in Fig. 9(a) & 9(b). If Phase comparator I is being used, it is also possible to set f_{min} of the VCO by using the network shown in Fig. 9(c). R_{min} may be determined using the graph in Fig. 9(c).

*Frequencies shown in graphs are actually $f_{VCO}/128$.

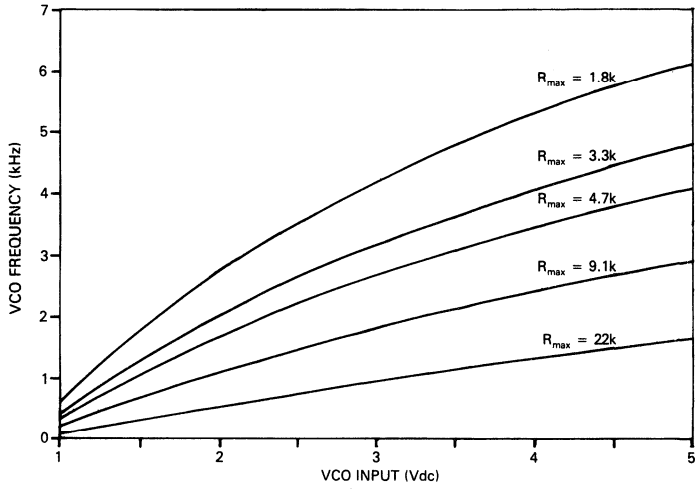


Fig. 9(a) VCO Conversion Gain Curves For Different Values of R_{max} (R_{17})

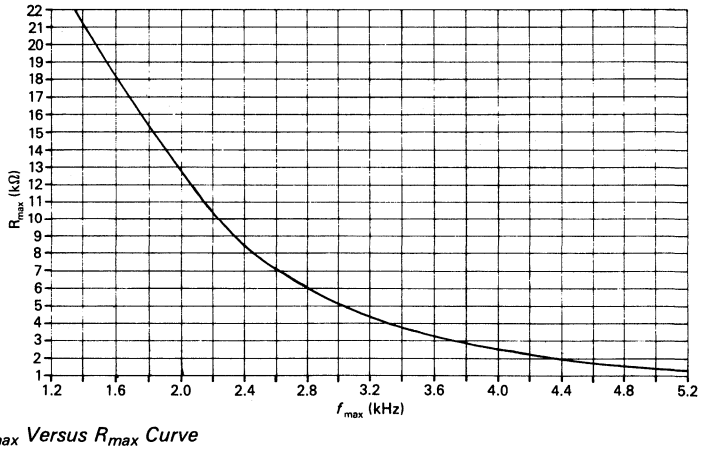


Fig. 9(b) VCO f_{max} Versus R_{max} Curve

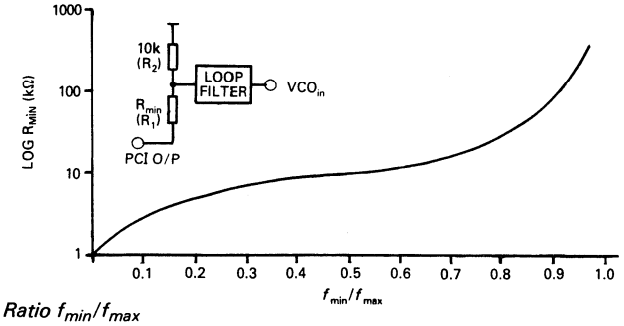


Fig. 9(c) R_{min} Versus Ratio f_{min}/f_{max}

Note 2 — Loop Filter Design

In order to maintain a fixed phase relationship between the VCO and reference input (or clock) signals, a 'second order loop' must be established. This is achieved by placing a lowpass filter between the phase comparator output and the VCO control input
This filter may be a 'lag' filter, (Fig.10a)or for improved stability a 'lead-lag' filter, (Fig10b).

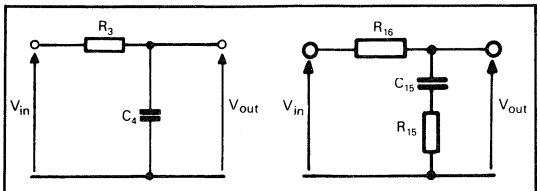


Fig. 10(a) 'Lag' Filter *Fig. 10(b) 'Lead-Lag' Filter*

The overall loop gain is given by $K_p . K_F \frac{K_{vco} . K_{div}}{j\omega}$

Where: K_p = phase comparator gain in volts/radian.
K_F = filter gain in volts/volt.
K_{vco} = VCO conversion gain in radians/sec-volt.
K_{div} = divider gain in radians/radian (1/128).

Selection of the frequency at which the loop gain is unity (0dB) depends on the application, the unity gain frequency should be high enough to allow the loop to track expected variations of the reference frequency but low enough to provide a 'flywheel' action to average noise and unwanted input transients.

Some typical loop filter component values for the FX406 using phase comparator II are tabled below.

f_{ug} Unity gain frequency (Hz)	R_{17} = 1.8kΩ		C_{15} (F)
	R_{16} (Ω)	R_{15} (Ω)	
50	92k	13k	1μ
100	39k	6k2	1μ
250	200k	62k	0.1μ
500	16k	24k	0.1μ

When using phase comparator I, the locp filter frequency response may be used to limit the capture range of the loop, that is the range of input frequencies that the loop will lock onto. This property may be used to provide a degree of selectivity if required. The following table shows filter component values for various capture ranges. It should be noted that the loop filter used here is the simple 'lag' filter (i.e. R_2 = 0), this is to minimise ripple at 2 x f_{in} on the loop filter output which would cause frequency modulation of the switched capacitor filter response.

Capture Range $2f_c$ (Hz)	R_3 (Ω)	C_4 (F)
100	470k	340n
200	100k	390n
500	100k	68n
1000	100k	15n
2000	100k	3.9n

Note 3 — Phase Comparators

The following table shows the principal characteristics of second order loops using phase comparator I ('EX-OR') with a 'lag' filter and phase comparator II (edge-triggered) using a 'lead-lag' filter.

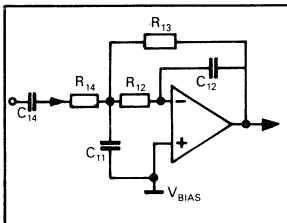
	PC I	PC II
Input duty cycle	50% optimum	don't care
Locks on harmonics of wanted signal	Yes	No
Noise rejection	Good	Poor
Ripple at 2 x f_{in} on loop filter output	Yes	Low
Lock range, $2f_l$	$f_{max} - f_{min}$	$f_{max} - f_{ug}$
Capture range, $2f_c$	$\frac{1}{\pi}\sqrt{\frac{K_p K_{vco} K_{div}\,\pi}{2\tau_1}}$	$f_{max} - f_{ug}$
Frequency of VCO for no signal input	$\frac{f_{max} - f_{min}}{2}$	f_{min}
Phase angle between f_{ref} and $f_{vco}/128$ in lock.	0° at f_{min} 180° at f_{max} 90° at mid-point	0°

Note 4 — Anti-aliasing

The relationship between f_o and the switched capacitor sampling clock in the FX406 is $f_{clk} = 64f_o$. This type of sampled filter produces alias or image responses centred on half the sampling rate, i.e., $32f_o$,

Filters with passbands extending beyond $32f_o$ will have spurious responses reflected into the passband at a corresponding distance below $32f_o$.

If the input frequency spectrum to the filter is likely to contain components at these alias frequencies then an additional RC filter is required to attenuate these inputs. This is easily accomplished by using the filter input amplifier, Fig. 11 shows a 2nd order 5kHz lowpass filter with passband gain suitable for values of f_o above 250Hz.



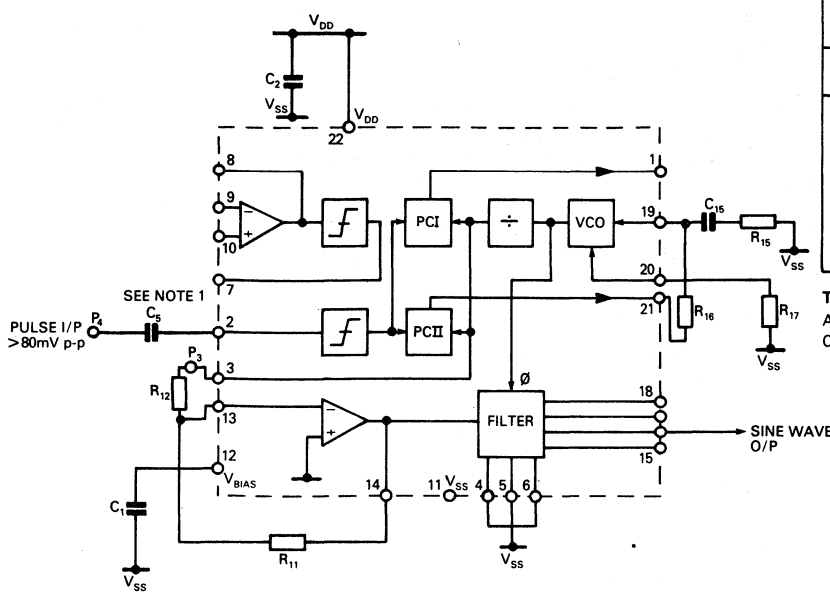
R_{12}	47kΩ
R_{13}	100kΩ
R_{14}	100kΩ
C_{11}	560pF
C_{12}	150pF
C_{14}	0.1μF

Fig. 11 Anti-Aliasing Filter

Special Note

Care must be taken when using the FX406 with f_o below 200Hz as the aliasing frequencies lie within the specified minimum passband of the filter.

On the highpass filter only, an additional lowpass response exists with its — 3dB point at $7f_c$ and a roll-off of 20dB/decade.



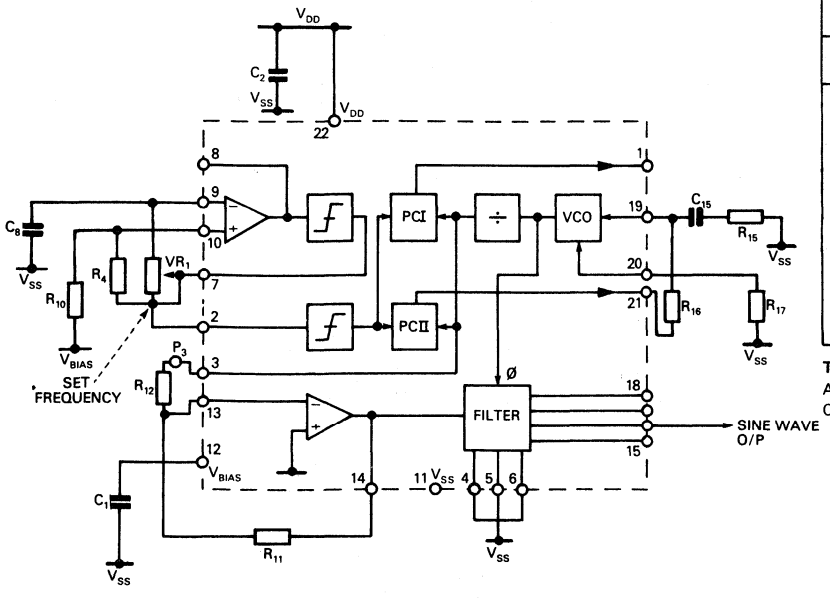
Component References

Component	Unit Value
R_{11}	24k
R_{12}	330k
R_{16}	39k
R_{15}	6.2k
R_{17}	1.8k
C_1, C_2	1.0μ
C_5	0.1μ
C_{15}	1.0μ

Tolerance
All resistors ±5%
Capacitors ±20%

NOTE 1
C_5 can be omitted for TTL or CMOS logic level input signals.

Fig. 12 Pulse to Sine Converter

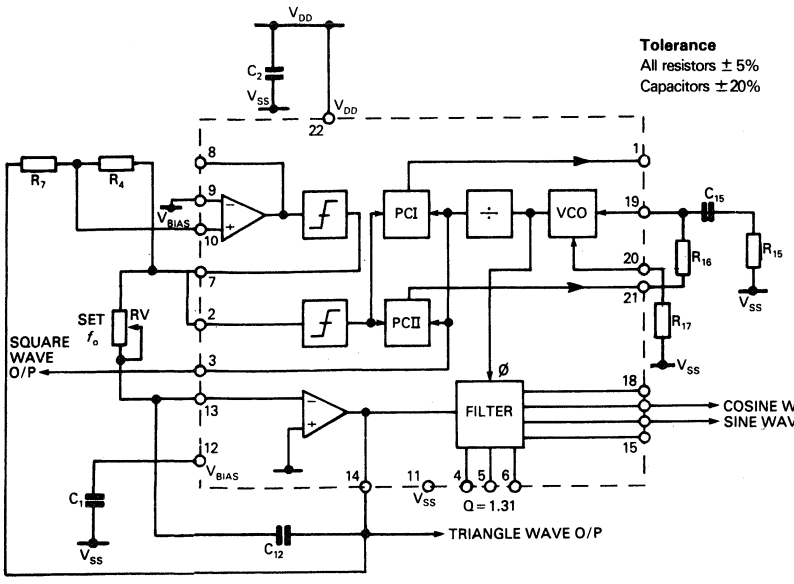


Component References

Component	Unit Value
R_4	200k
R_{10}	100k
R_{11}	24k
R_{12}	330k
R_{14}	220k
R_{15}	13k
R_{16}	91k
R_{17}	1.8k
C_1, C_2	1.0μ
C_8	4.7n
C_{15}	1.0μ
VR_1	1MΩ

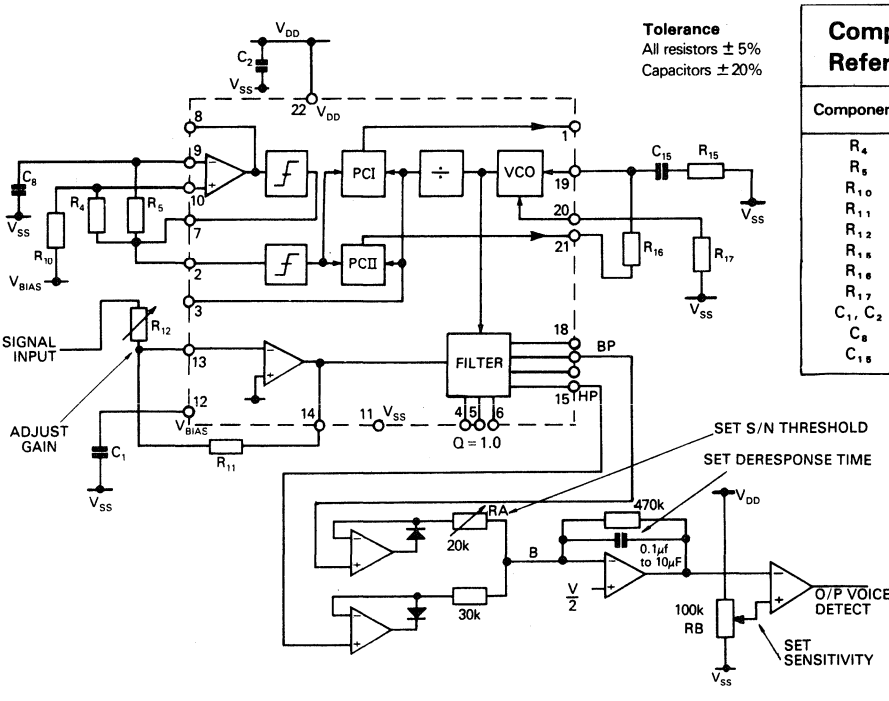
Tolerance
All resistors ±5%
Capacitors ±20%

Fig. 13 1kHz Sine Wave Oscillator



Component References	
Component	Unit Value
R_4	180k
R_7	100k
R_{15}	13k
R_{16}	91k
R_{17}	1.8k
RV	1M
C_1, C_2	1.0μ
C_{12}	4.7n
C_{15}	1.0μ

Fig. 14 Function Generator



Component References	
Component	Unit Value
R_4	100k
R_5	56k
R_{10}	100k
R_{11}	24k
R_{12}	30k
R_{15}	62k
R_{16}	200k
R_{17}	1.8k
C_1, C_2	1.0μ
C_8	10n
C_{15}	0.1μ

NOTES:
1. *Adjust gain R_{12} for largest filter output without clipping.*
2. *Vary R_A to give $V_{\frac{1}{2}}$ at point B.*
3. *Set R_B for threshold.*
4. *Set C_A for de-response time.*

Fig. 15 Voice Operated Switch

Component References	
Component	**Unit Value**
R_4	100k
R_{10}	100k
R_{11}	24k
R_{12}	330k
R_{15}	24k
R_{16}	16k
R_{17}	1.8k
VR_1	100k
C_1, C_2	1.0μ
C_8	4.7n
C_{15}	0.1μ

Tolerance
All resistors ± 5%
Capacitors ± 20%

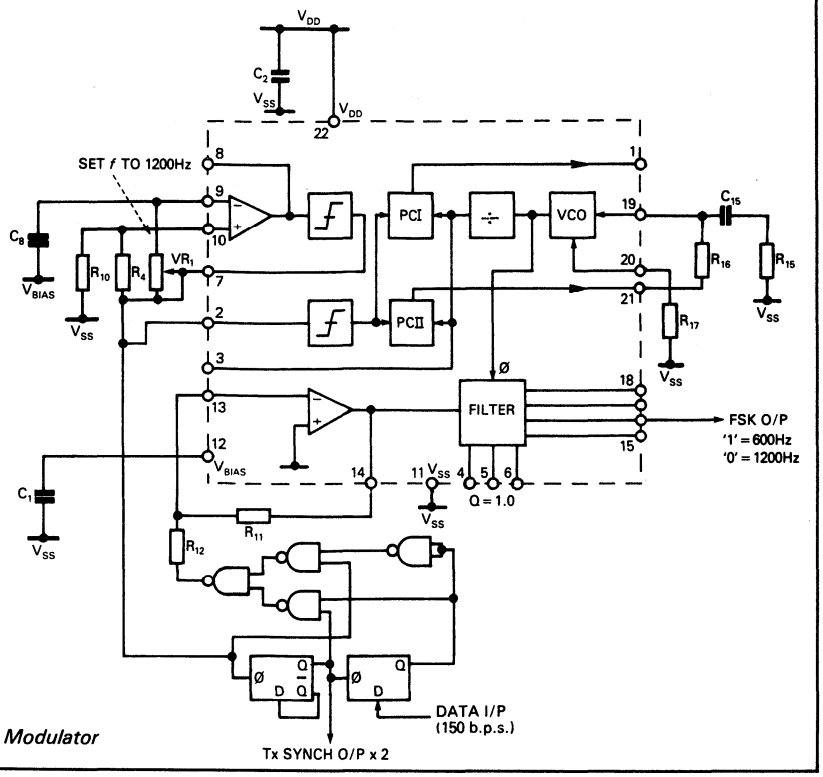


Fig. 16 150 Baud FSK Modulator

Component References	
Component	**Unit Value**
R_4	200k
R_{10}	130k
R_{11}	270k
R_{12}	24k
R_{17}	1.8k
VR_2	50k
C_1, C_2	1.0μ
C_{13}	0.1μ

Tolerance
All resistors ±5%
Capacitors ±20%

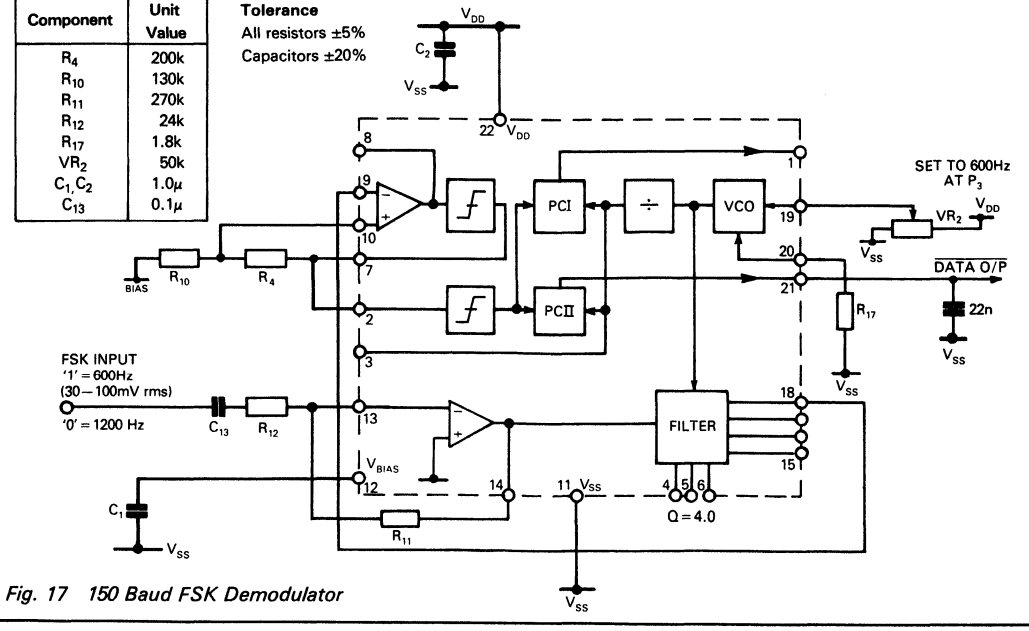


Fig. 17 150 Baud FSK Demodulator

Package Outlines

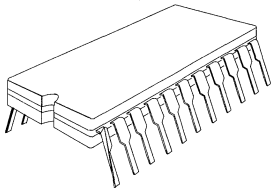
The FX406 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX406 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX406J 22-pin cerdip DIL (J3)

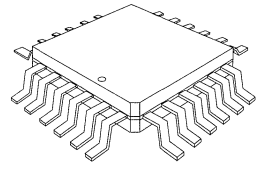
NOT TO SCALE



Max. Body Length 27.38mm
Max. Body Width 9.75mm

FX406LG 24-pin quad plastic encapsulated bent and cropped (L1)

NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

Ordering Information

FX406J 22-pin cerdip DIL (J3)

FX406LG 24-pin plastic encapsulated bent and cropped (L1)

Integrated Circuits Data Book

Section 8

Modems for Radio and Data Comms

CML Semiconductor Products

PRODUCT INFORMATION

FX429 Band III FFSK Modem for Trunked Radio Systems

Publication D/429/6 July 1994

Features/Applications

- Band III and General Purpose Trunked Radio Applications
- Full-Duplex 1200 Baud Operation
- High Intelligence
- Error Checking in Receive
- Error Check Word Generation
- Frame SYNC and SYNT Detection
- Preamble Generation
- µProcessor Compatible Interface
- Carrier Detection On-Chip
- Low Power Consumption
- General Purpose Timer

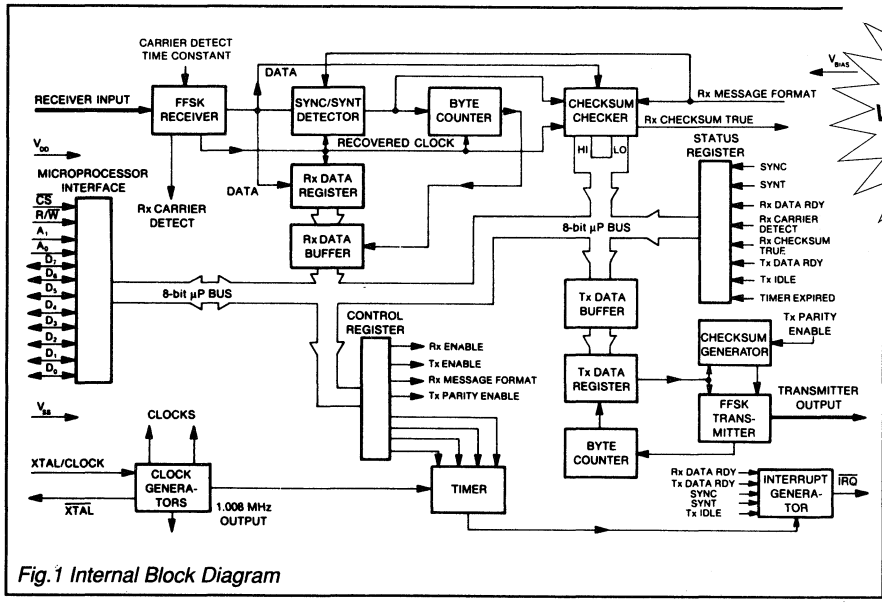


Fig.1 Internal Block Diagram

NEW
1200/2400Baud Version Available
FX429A

FX429

Brief Description

The FX429 is a single-chip CMOS 1200 baud FFSK Modem, designed primarily for use in trunked radio systems but may also be employed in other general purpose radio or line data communication applications.

The device has been designed to conform to the UK Band III trunked radio protocols MPT 1317/1327.

The FX429 is full duplex at 1200 baud and includes an 8-bit parallel microprocessor interface and a programmable timer which may be set for interrupt periods of 8 to 120 bits.

Preamble and an error-check word are automatically generated in the transmit mode.

Error checking is performed and the 16-bit SYNC or SYNT words are detected in the receive mode.

An on-chip Xtal/clock generator requiring an external 4.032MHz Xtal or clock input provides all microcircuit filter sampling clocks and modem timings whilst also supplying a "Clock ÷ 4" output (1.008MHz).

The FX429, which has a powersaving facility, requires a single 5-volt power supply and is available in both cerdip DIL and plastic SMD packages.

Pin Number DIL FX429J	Pin Number Quad FX429LG/LS	Function
1	1	**V_{BIAS} :** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS} by capacitor C_4, see Figure 3. **Warning Note** – In order to reduce current consumption, the potential at this pin is lowered to V_{SS} when both Tx and Rx are disabled.
2	2	**Transmit Output :** The 1200 baud, 1200Hz/1800Hz FFSK Tx output. When not enabled by the Control Register (D_0) its output impedance is set high.
3	4	**Receiver Input :** The 1200 baud received FFSK signal input. The 1200Hz/1800Hz audio to this pin must be a.c. coupled via capacitor C_3, see Figure 3.
5	5	**V_{DD} :** Positive Supply. A single +5V regulated supply is required. It is recommended that this power rail be decoupled to V_{SS} by capacitor C_6, see Figure 3.
6	6	**Carrier Detect Time Constant :** The on-chip Carrier Detect integration function requires two external components on this pin. A capacitor, C_5, to V_{SS}, together with a resistor, R_2, to V_{DD}. See Figure 3.
7	7	**Xtal/Clock :** The input to the clock oscillator inverter. A 4.032 MHz Xtal or externally derived clock pulse input should be connected here. See Figure 3.
8	8	**$\overline{\text{Xtal}}$:** The output of the 4.032 MHz clock oscillator.
9	9	**D_0 :** **Microprocessor Data Interface**
10	10	**D_1 :**
11	11	**D_2 :**
12	12	**D_3 :** These 8 lines are used by the device to communicate with a microprocessor
13	13	**D_4 :** with the A_2, A_0 and A_1 inputs determining register selection.
14	14	**D_5 :**
15	15	**D_6 :**
16	16	**D_7 :**
17	17	**A_0 : Register Selection.** These inputs, with the A_2 input, select the required register to
18	18	**A_1 :** the data bus as shown in Table 1 (below).
19	19	**$\overline{\text{Strobe}}$:** Performs the dual functions of selecting the device for Read or Write and strobing data in or out. It should be generated by gating high-order address bits with a read/write clock. The FX429 is selected when Strobe = logic "0." See Figure 5.
20	20	**A_2 :** Used in conjunction with A_1 and A_0 to determine which internal registers are connected to the data interface pins (D_0 – D_7) during $\overline{\text{Strobe}}$ (see Table 1 and Figure 5).
21	21	**$\overline{\text{IRQ}}$:** Interrupt Request. This line will go to a logic '0' when an interrupt occurs. This output can be "wire OR'd" with other active low components (100kΩ pullup to V_{DD}). The conditions that cause the interrupts are indicated at the Status Register and are as follows: *Timer Expired*, *Rx Data Ready*, *Tx Data Ready*, *Tx Idle*, *Rx SYNC Detect*, *Rx SYNT Detect*
23	22	**V_{SS} :** Negative Supply (GND).
24	23	**Clock ÷ 4 :** A 1.008 MHz ($X_1 \div 4$) clock is available at this output for external circuit use, note the source impedance and source current limits.
4, 22	3, 24	These pins are not connected internally, leave open circuit.

Table 1

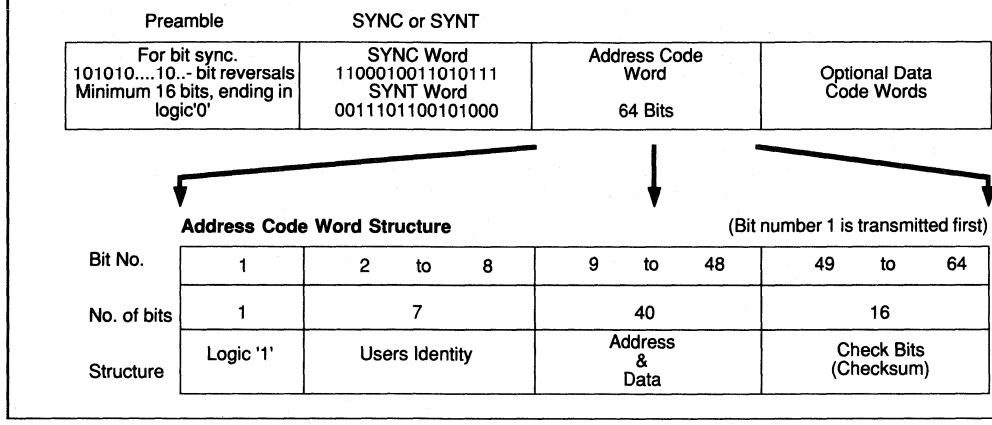
Register	A_2	A_0	A_1
Control	0	1	1
Status	1	1	1
Rx Data	1	0	1
Tx Data	0	0	1
Syndrome Low	1	0	0
Syndrome High	1	1	0

Modems in Mobile Data Signalling ..... An Introduction

Digital Code Format

The recommended Digital Code Format for use over Land Mobile Radio Systems is detailed in the Department of Trade and Industry, Radio Regulatory Division's publications MPT 1317 and MPT 1327, and is as described briefly below.

Fig. 2 The Data stream – Rx and Tx at 1200baud, the minimum, overall transmission length is 96 bits.



Operation

The FX429 can be used for Full-Duplex operation with the host microprocessor only having to operate on the data whilst the modem (FX429) handles all other signalling routines and requirements.

In the **Tx** mode the FX429 will :-

(1) Internally generate and transmit a preamble – bit reversals, for system bit synchronization.
(2) Accept from the host, and transmit, a 16-bit 'SYNC' or 'SYNT' word.
(3) Accept from the host, and transmit, 6 bytes of data (Address Code Word).
(a) Upon a software command, internally calculate and transmit a 2-byte checksum based on the previous 6 data bytes. – or –
(b) Upon a software command, disable internal checksum generation and allow continuous data transmission.
(4) Transmit 1 'hang bit' and go idle when all loaded data traffic has been sent (followed by a "Tx Idle" interrupt).

In the **Rx** mode the FX429 will :-

(1) Detect and achieve bit synchronization within 16 bits.
(2) Search for and detect the 16-bit 'SYNC'/'SYNT' word.
(3) Output all received data after 'SYNC/SYNT,' in byte form.
(4) Upon a software command (Rx Message Format), use the received checksum to calculate the presence (if any) of errors, and advise the host with an interrupt and a 16-bit Syndrome word.

Note – In Rx a software command is used to determine whether a 'SYNC'/'SYNT' word is required after every 8 (6 data + 2 checksum) received bytes, or "data" is received continually.
Normally the 'SYNC' word is used on the Control data channel and the 'SYNT' word is used on the Traffic data channel.

Non MPT Application – Full-Duplex

The functions described in this section, to allow the FX429 modem to operate as a general purpose device, are obtained using the commands and indications detailed in the "Register Instructions" pages.

Tx – When enabled the device transmits a "101010.....10" preamble until data for transmission is loaded by the host microprocessor.
Transmits 6 bytes of the loaded data followed by a 2-byte checksum based on that data. As long as Tx data is loaded the transmitter will transmit, the 2-byte checksum being produced after every 6 bytes (8 byte packages). Automatic checksum generation can be inhibited by a software command to allow transmission of continuous data streams.

Rx – When enabled requires the16-bit SYNC or SYNT word (see notes) before outputting data bytes. The modem receiver will then output continuous bytes of data, after every 6 bytes received a 2-byte checksum word will be output and can be ignored or used for error checking.

Control Register $A_1 = 1$ $A_0 = 1$ $A_2 = 0$ Write Only

The Control Register, when selected, directs the modem's operation as described below.

Bit	Description	Function	Set = logic '1' (High) Clear = logic '0' (Low)
Bit 0 D_0	**Tx Enable ***	**Set** – D_0 enables the transmitter for operation. A '0 – 1' transition causes bit synchronization and the start of 1010.....10 preamble pattern transmission. At least one byte of preamble will be transmitted. If data is loaded into the Tx Data Buffer before one byte has been sent then that data will follow, otherwise whole bytes of preamble will continue until data is loaded. **Clear** – The Transmitter Output pin is set to a high impedance and no transmitter interrupts are produced.	
Bit 1 D_1	**Tx Parity Enable**	**Set** – D_1 indicates to the transmitter that 2–byte checksums are to be generated by the modem. A '0 – 1' transition starts checksum generation on the next six bytes loaded from the Tx Data Buffer into the Tx Data Register. Checksum generation continues for every 6 bytes loaded until this bit is cleared. The transmitter will send the generated checksum (2 bytes) after the last of each 6 bytes have been sent. If an underrun (no more data loaded) condition occurs before 6 bytes have been loaded checksum generation will abort, the transmission will cease after one 'hang' bit has been sent and Bit 4 in the Status Register (Tx Idle) will be set. No checksum will be transmitted. **Clear** – No checksum generation is carried out and the host may supply the checksum bytes. The output is then "as written".	
Bit 2 D_2	**Rx Enable ***	**Set** – D_2 enables the receiver for operation. No data is produced (i.e. No Rx Data Ready interrupts) until a 'SYNC' or 'SYNT' word is found in the received bit stream. **Clear** – The receiver is disabled and all interrupts caused by the receiver are inhibited.	
Bit 3 D_3	**Rx Message Format**	**Set** – D_3 is sampled after a checksum has been received and allows the host to control the way the receiver handles the following data bits. If 'set' the receiver will assume that the next 6 bytes are data and will start error checking accordingly. **Clear** – The receiver will stop data transfer to the host after the 2 checksum bytes until another 'SYNC' or 'SYNT' frame word is received.	
Bit 4 D_4	**Timer LSB**	These four bits control the timer as follows :-	
Bit 5 D_5	**Timer**		
Bit 6 D_6	**Timer**		
Bit 7 D_7	**Timer MSB**		

D_7	D_6	D_5	D_4		
0	0	0	0	Reset counter and disable timer interrupts	
0	0	0	1	Count and interrupt every -	8 bits
0	0	1	0	" " "	16 bits
0	0	1	1	" " "	24 bits
0	1	0	0	" " "	32 bits
0	1	0	1	" " "	40 bits
0	1	1	0	" " "	48 bits
0	1	1	1	" " "	56 bits
1	0	0	0	" " "	64 bits
1	0	0	1	" " "	72 bits
1	0	1	0	" " "	80 bits
1	0	1	1	" " "	88 bits
1	1	0	0	" " "	96 bits
1	1	0	1	" " "	104 bits
1	1	1	0	" " "	112 bits
1	1	1	1	" " "	120 bits

If a new timer value is written to these inputs within 1 byte period of the last timer interrupt then the next timer period will be correct without first having to reset the timer, otherwise the timer must be reset to zero and then set to the new time.

***Note* –**

Enabling Times

The time taken to enable one section (receiver or transmitter) when both sections are initially disabled is 16 bit periods. If one section (receiver or transmitter) is already enabled this time is reduced to "one-half" of a bit period.

Tx Enable

If using the internal Tx Preamble generation facility, e.g. with the internal timer setting the preamble length, the device may occasionally produce a Tx Data Ready interrupt immediately after a Tx Enable command. User software should handle this occurrence by either:

(a) Detecting that the Timer interrupt Status Bit is not set and that it is not appropriate to load Tx data at this time. or,

(b) Not using the Timer. i.e. immediately after Tx enable, reading the Status Register and loading a byte of preamble. This resets any interrupt. The length of preamble transmitted is now controlled by the number of bytes loaded.

Status Register $A_1 = 1$ $A_0 = 1$ $A_2 = 1$ Read Only

When an interrupt is generated the $\overline{IRQ}$ Output goes Low with the Status Register bits indicating the sources of the interrupt.

Bit	Description	Function	Set = logic '1' (High) Clear = logic '0' (Low)
Bit 0 D_0	**Rx Data Ready**	D_0 when set, causes an interrupt indicating that received data is ready to be read from the Rx Data Buffer. This data must be read within 8 bit periods. **Set** – when a byte of data is loaded into the Rx Data Buffer, if a frame (SYNC/SYNT) word has been received. **Bit and Interrupt Cleared** – (i) by a read of the Status Register followed by a read of the Rx Data Buffer or (ii) by Rx Enable going Low.	
Bit 1 D_1	**Rx Checksum True**	D_1 when set, indicates that the error checking on the previous 6 bytes agreed with the received checksum. This function, which is valid when the Rx Data Ready bit (D_0) is set for the second byte of the received checksum, does not cause an interrupt. **Set** – by a correct comparison between the received and generated checksums. **Cleared** – (i) by a read of the Status Register followed by a read of the Rx Data Buffer, or (ii) by Rx Enable going Low.	
Bit 2 D_2	**Rx Carrier Detect**	D_2 is a " Real Time " indication from the modem receiver's carrier detect circuit and does not cause an interrupt. When FFSK tones are present at the receiver input this bit goes High, for no FFSK input this bit goes Low. When the Rx Enable bit (D_2– Control Register) is Low Rx Carrier Detect will go Low.	
Bit 3 D_3	**Tx Data Ready**	D_3 when set, causes an interrupt to indicate that a byte of data should be written to the Tx Data Buffer within 8 bit periods. **Set** – (i) when the contents of the Tx Data Buffer are transferred to the Tx Data Register, or (ii) when the Tx Enable is set – No interrupt is generated in this case. **Bit Cleared** – (i) by a read of the Status Register followed by a write to the Tx Data Buffer, or (ii) by Tx Enable going Low. **Interrupt Cleared** – (i) by a read of the Status Register, or (ii) by Tx Enable going Low.	
Bit 4 D_4	**Tx Idle**	D_4 causes an interrupt when set, to indicate that all loaded data and one 'hang' bit have been transmitted. **Set** – one bit period after the last byte is transmitted. This last byte could be either "checksum" or " loaded data" depending upon the Tx Parity Enable state (Control Register D_1). **Bit Cleared** – (i) by a write to the Tx Data Buffer, or (ii) by Tx Enable going Low. **Interrupt Cleared** – (i) by a read of the Status Register, or (ii) by Tx Enable going Low.	
Bit 5 D_5	**Timer Interrupt**	D_5, when set, causes an interrupt to indicate that the set timer period has expired. (Control Register D_4 — D_7). **Set** – by the timer. **Bit and Interrupt Cleared** – by a read of the Status Register.	
Bit 6 D_6	**Rx SYNC Detect** *	D_6, when set, causes an interrupt to indicate that a 16-bit 'SYNC' word (1100010011010111) has been detected in the received bit stream. **Set** – on receipt of the 16th bit of a 'SYNC' word. **Bit and Interrupt Cleared** – (i) By a read of the Status Register, or (ii) by Rx Enable going Low.	
Bit 7 D_7	**Rx SYNT Detect** *	D_7, when set, causes an interrupt to indicate that a 16-bit 'SYNT' word (0011101100101000) has been detected in the received bit stream. **Set** – on receipt of the 16th bit of a 'SYNT' word. **Bit and Interrupt Cleared** – (i) By a read of the Status Register, or (ii) by Rx Enable going Low.	
***Note** –		*'SYNC' and 'SYNT' Detection is disabled whilst the checksum checker is running.*	

Rx Data Buffer — $A_1 = 1$ — $A_0 = 0$ — $A_2 = 1$ — Read Only

These 8 bits are the last byte of data received with bit 7 being received first. *Note the relative positions of the **MSB** and **LSB** presented in this bit stream, the position may be different to the convention used in other µProcessor peripherals.*

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
LSB	-	-	-	-	-	-	MSB

Tx Data Buffer — $A_1 = 1$ — $A_0 = 0$ — $A_2 = 0$ — Write Only

These 8 bits loaded to the Tx Data Buffer are the next byte of data that will be transmitted, with bit 7 being transmitted first. *Note the relative positions of the **MSB** and **LSB** presented in this bit stream, the position may be different to the convention used in other µProcessor peripherals.* If the the Tx Parity Enable bit (Control Register D_1) is set, a 2–byte checksum will be inserted and transmitted by the modem after every 6 transmitted " message " bytes.

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
LSB	-	-	-	-	-	-	MSB

The Syndrome Word

This 16-bit word (both **Low** and **High** bytes) may be used to correct errors.
Bits S_1 to S_{15} are the 15 bits remaining in the polynomial divider of the checksum checker at the end of 6 bytes of " received message." For a correct message all 15 bits (S_1 to S_{15}) will be zero.
The 2 Syndrome bytes are valid when the Rx Data Ready bit (Status Register D_0) is set for the second byte of the receivedchecksum and should be read, if required, before 8 byte periods.

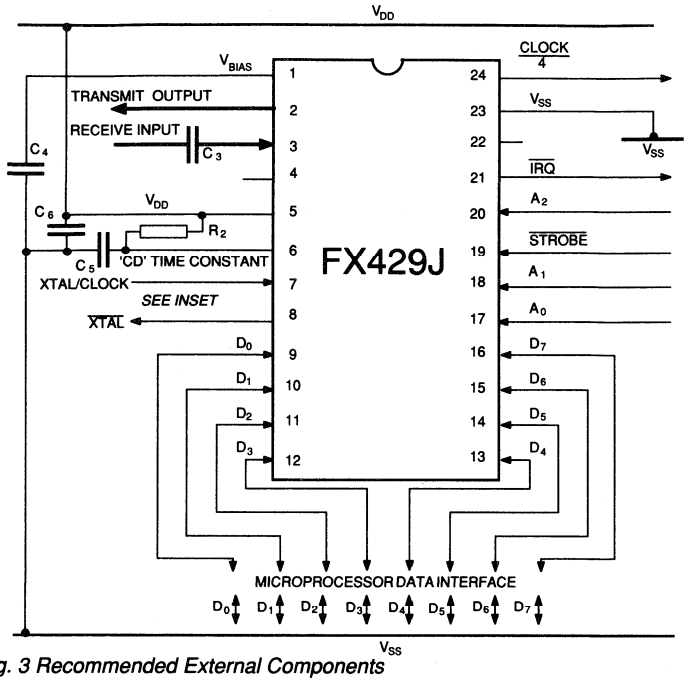
Syndrome Low Byte — $A_1 = 0$ — $A_0 = 0$ — $A_2 = 1$ — Read Only

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
S1	S2	S3	S4	S5	S6	S7	S8

Syndrome High Byte — $A_1 = 0$ — $A_0 = 1$ — $A_2 = 1$ — Read Only

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
S9	S10	S11	S12	S13	S14	S15	PARITY ERROR

D_7 – This is a "Parity Error Bit" – Indicating an error between the received parity bit and the parity bit internally generated from the incoming message. Thus for a correctly received message all 16 bits of the Syndrome Word (S_1 to S_{15} and Parity Error) will be zero.



Component References

Component	Unit Value
R_1	1.0M
R_2	1.0M
C_1	33p
C_2	33p
C_3	0.1µ
C_4	1.0µ
C_5	1.0µ
C_6	1.0µ
X_1	4.032MHz

Tolerances. Resistors ± 10%
Capacitors ± 20%

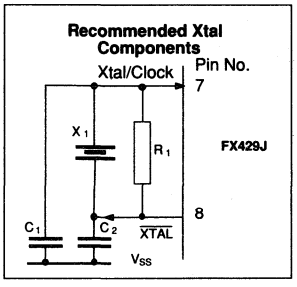


Fig. 3 Recommended External Components

Carrier Detect Time Constant

The value of the Carrier Detect capacitor, C_5, determines the carrier detect time constant. A long time constant (larger value C_5), results in improved noise immunity but increased response time. C_5 may be varied to optimise noise immunity/ reponse time.

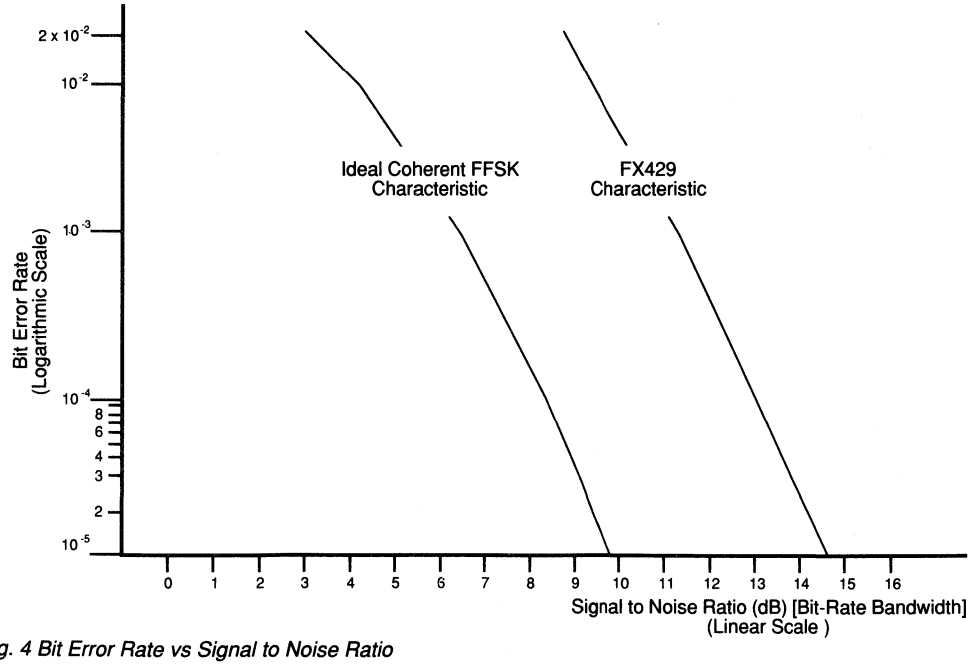
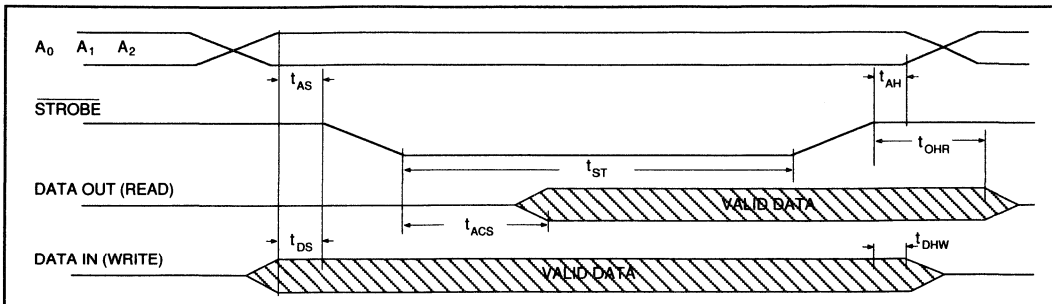


Fig. 4 Bit Error Rate vs Signal to Noise Ratio

Timing Information

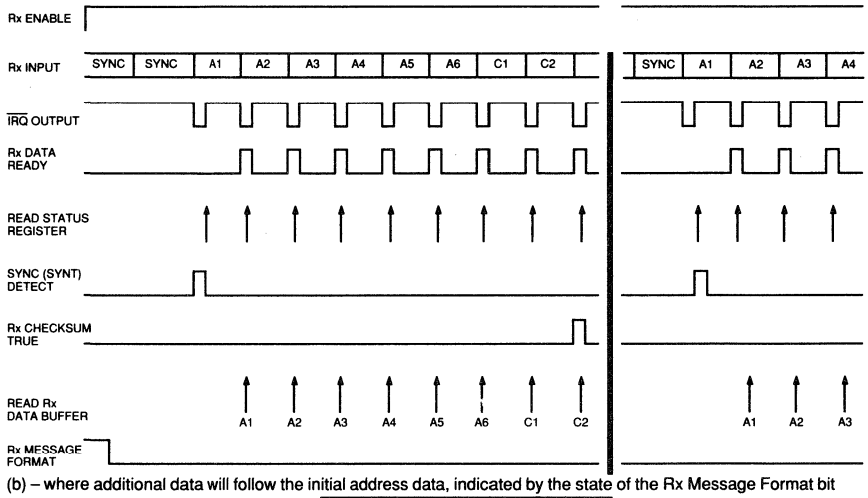


t_{ACS} – Access Time
t_{AS} – Address Setup Time
t_{AH} – Address Hold Time
t_{DS} – Data Setup Time
t_{DHW} – Data Hold Time (Write)
t_{OHR} – Output Hold Time (Read)
t_{ST} – Strobe Time

Fig. 5 Read and Write Timing Diagram

Operation – Rx

(a) Rx – where SYNC/SYNT is required after every message



(b) – where additional data will follow the initial address data, indicated by the state of the Rx Message Format bit

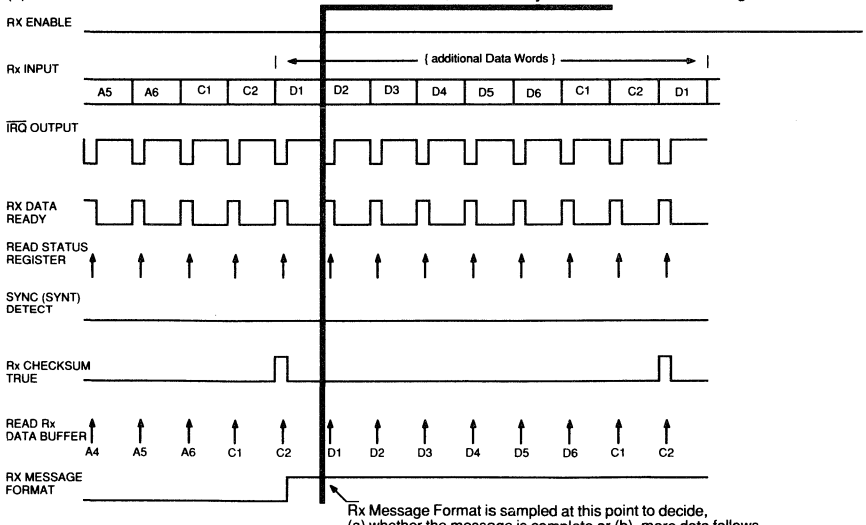


Fig. 6 Simplified Rx Timing

Operation – Tx

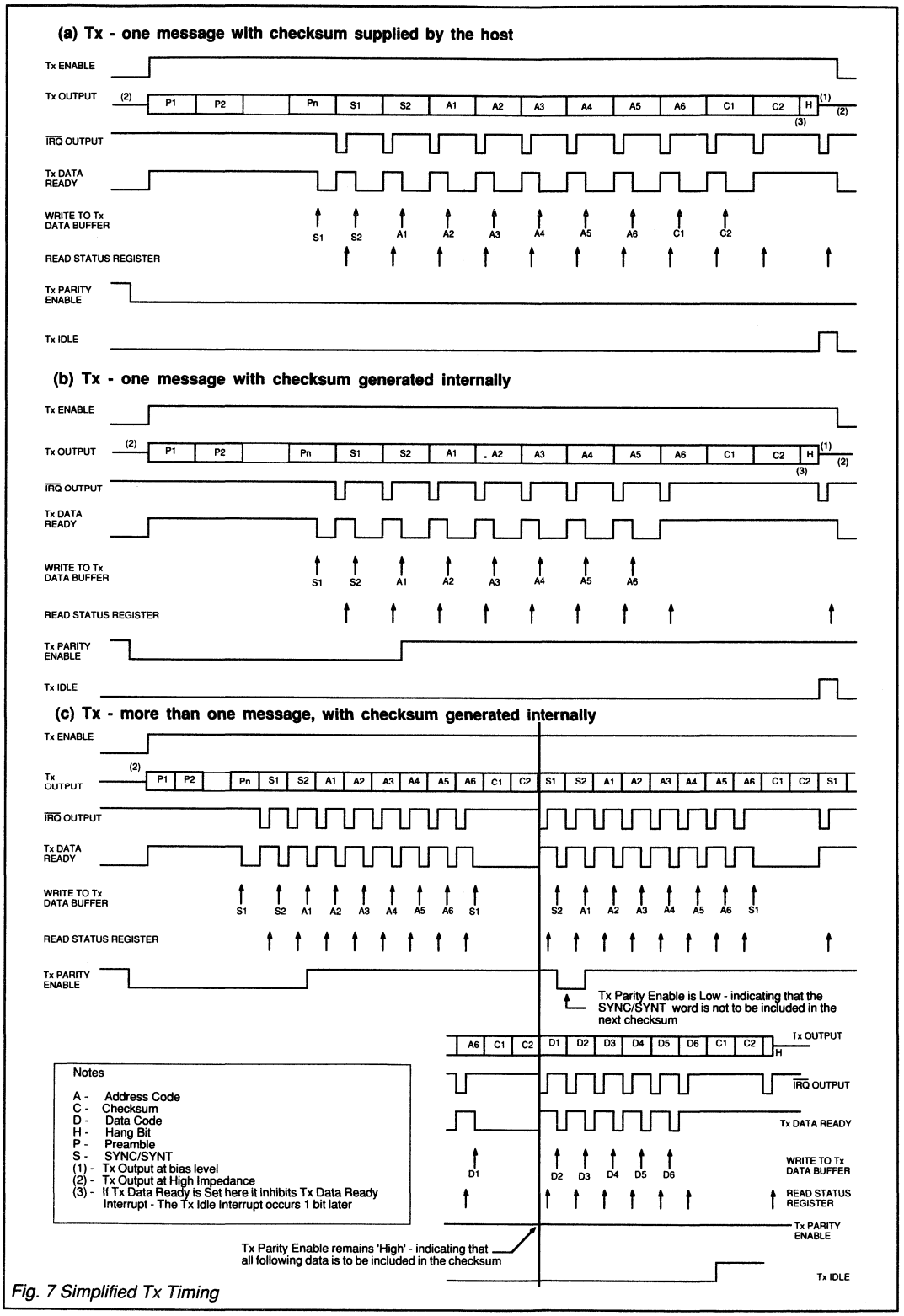


Fig. 7 Simplified Tx Timing

Basic Power-Up Software

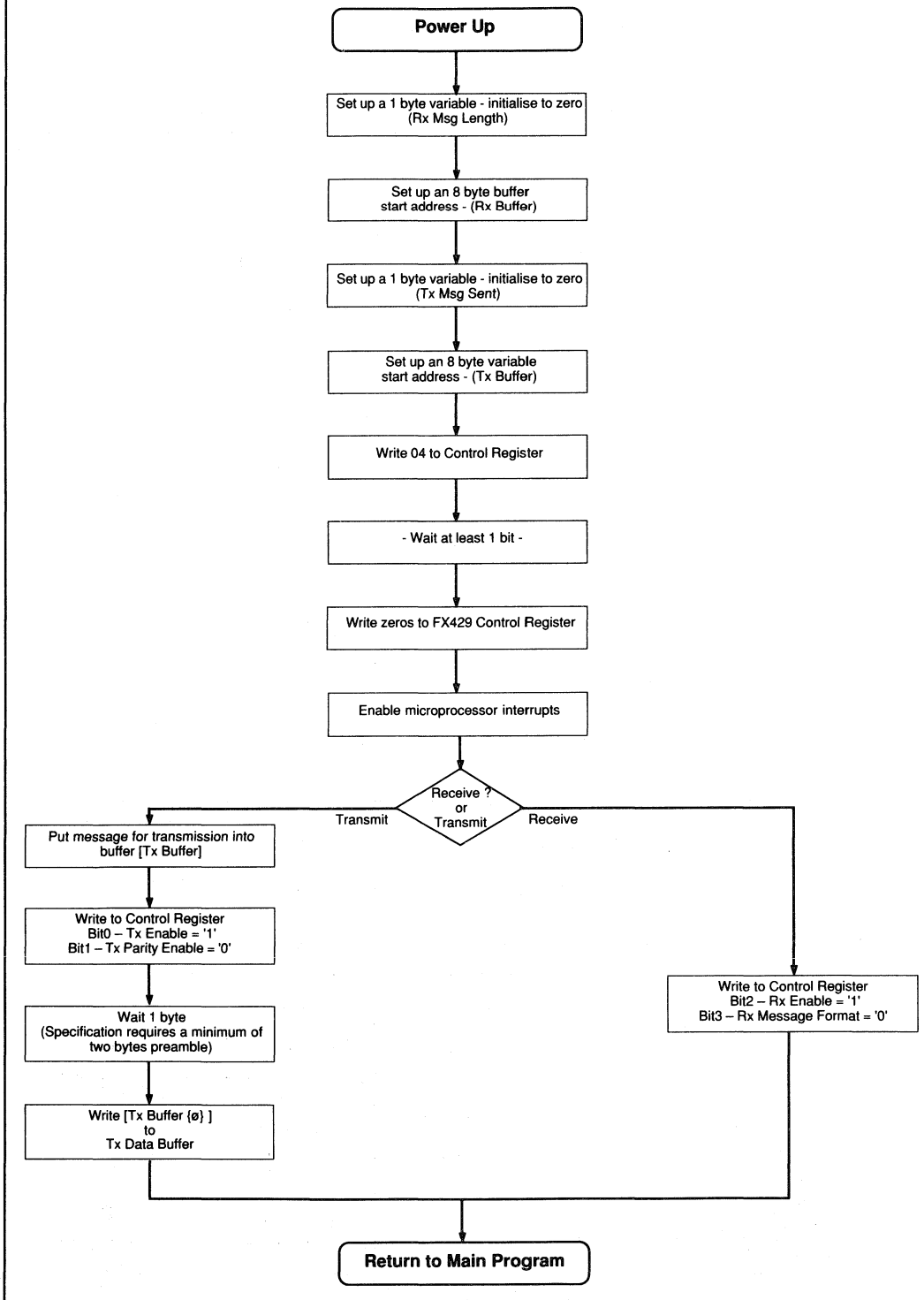


Fig. 8 Power–Up Flow

Basic Software Interrupt Flow

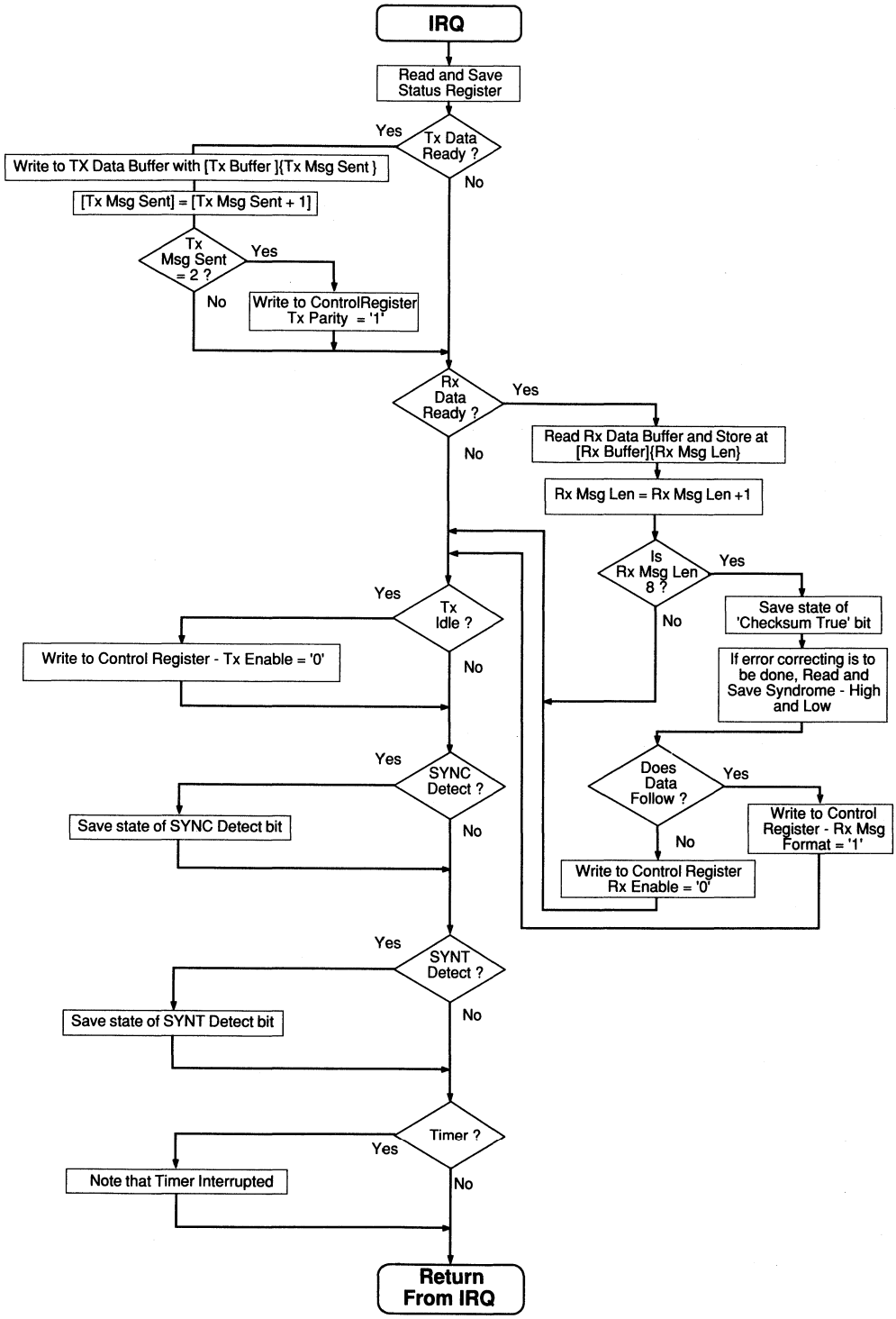


Fig. 9 Interrupt Flow

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX429J**	-30°C to +85°C (ceramic)
	FX429LG/LS	-30°C to +70°C (plastic)
Storage temperature range:	**FX429J**	-55°C to +125°C (ceramic)
	FX429LG/LS	-40°C to +85°C (plastic)

Operating Limits

All characteristics are measured using the following parameters unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C. Xtal/Clock f_0 = 4.032 MHz. Audio level 0dB ref: = 300mV rms.

Bit Rate Bandwidth = 1200Hz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	–	5.5	V
Supply Current Ranges					
Rx and Tx Enabled		–	–	7.0	mA
Rx Enabled, Tx Disabled		–	4.0	6.0	mA
Rx Disabled, Tx Enabled		–	–	7.0	mA
Rx and Tx Disabled	10	–	1.5	2.5	mA
Dynamic Values					
Modem Internal Delay		–	1.5	–	ms
Interface Levels					
Output Logic '1' Source Current	2	–	–	120	µA
Output Logic '0' Sink Current	3	–	–	360	µA
Three State Output Leakage Current		–	–	4.0	µA
D_0 – D_7 Data In/Out	1				
Logic '1' Level		3.5	–	–	V
Logic '0' Level		–	–	1.5	V
A_1, A_0, A_2, $\overline{\text{STROBE}}$, $\overline{\text{IRQ}}$	4				
Logic '1' Level		4.0	–	–	V
Logic '0' Level		–	–	1.0	V
Analogue Impedances					
Rx Input		100	–	–	kΩ
Tx Output (Enabled)		–	10	–	kΩ
Tx Output (Disabled)		–	5	–	MΩ
On-Chip Xtal Oscillator					
R_{IN}		10	–	–	MΩ
R_{OUT}	5	5.0	–	15	kΩ
Oscillator Gain		–	15	–	dB
Xtal frequency		–	4.032	–	MHz
Timing – (Fig. 5)					
Access Time – (t_{ACS})		–	–	135	ns
Address Hold Time – (t_{AH})		0	–	–	ns
Address Set-up Time – (t_{AS})		0	–	–	ns
Data Hold Time (Write) – (t_{DHW})		85	–	–	ns
Data Set-up Time (Write) – (t_{DS})		0	–	–	ns
Output Hold Time (Read) – (t_{OHR})		15	–	105	ns
Strobe Time – (t_{ST})		140	–	–	ns

Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
Dynamic Values.....					
Receiver					
Signal Input Levels	6	–9.0	–2.0	+10.5	dB
Bit Error Rate	7				
@ 12dB Signal/Noise Ratio		–	7.0	–	10^{-4}
@ 20dB Signal/Noise Ratio		–	1.0	–	10^{-6}
Synchronization @ 12dB Signal/Noise Ratio	8				
Probability of Bit16 being correct		–	99.5	–	%
Carrier Detect Response Time	8	–	13.0	–	ms
Transmitter					
Output Level		–	8.25	–	dB
Output Level Variation		-1.0	–	+1.0	dB
Output Distortion		–	3.0	5.0	%
3rd Harmonic Distortion		–	2.0	3.0	%
Logic '1' Frequency	9	–	1200	–	Hz
Logic '0' Frequency	9	–	1800	–	Hz
Isochronous Distortion					
1200Hz – 1800Hz		–	25	40	µs
1800Hz – 1200Hz		–	20	40	µs

Notes

1. With each data line loaded as, C = 50pf and R = 10kΩ.
2. V_{OUT} = 4.6V.
3. V_{OUT} = 0.4V
4. Sink/Source currents ≤ 0.1mA.
5. Both Xtal and Xtal ÷ 4 Outputs.
6. With 50dB Signal/Noise Ratio.
7. See Figure 3, Bit Error Rate.
8. This Response Time is measured using a 10101010101....01 pattern input signal at a level of 230mV rms (-2.3dB) with no noise.
9. Dependent upon Xtal tolerance.
10. Powersave is only active when both Rx and Tx functions are disabled.

Checksum Generation and Checking

Generation – The checksum generator takes the 48 bits from the 6 bytes loaded into the Tx Data Buffer and divides them modulo–2, by the generating polynomial;-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted).
This 16–bit word is used as the "Checksum."

Checking – The checksum checker does two things:
It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo–2, by the generating polynomial;-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

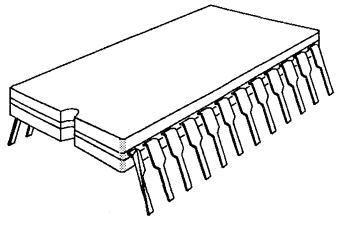
The 15 bits remaining in the polynomial divider are checked for all zero.
Secondly, it generates an EVEN parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64).
If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the Rx Checksum True bit (SR D_1) bit is set.

Package Outlines

The FX429 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX429J 24-pin cerdip DIL (J4)

NOT TO SCALE



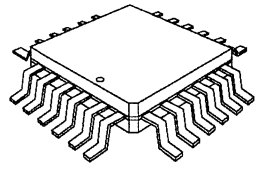
Max. Body Length 32.03mm
Max. Body Width 14.81mm

Handling Precautions

The FX429 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX429LG 24-pin quad plastic encapsulated bent and cropped (L1)

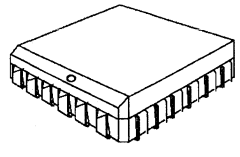
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX429LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX429J 24-pin cerdip DIL (J4)

FX429LG 24-pin quad plastic encapsulated bent and cropped (L1)

FX429LS 24-lead plastic leaded chip carrier (L2)

CML Semiconductor Products

PRODUCT INFORMATION

FX529 FFSK Modem for Trunked Radio Systems

Publication D/529/1 December 1991
Provisional Issue

Features

- PAA 1382 and General Purpose Trunked Radio Applications
- Meets Draft ETSI EBSS 1200 Signalling Specification
- Full-Duplex 1200 Baud Operation
- High Intelligence
- Error Checking in Receive
- Frame SYNC/SYNT Detection
- Preamble Generation
- µProcessor Compatible Interface
- Carrier Detection On-Chip
- General Purpose Timer
- Error Check Word Generation

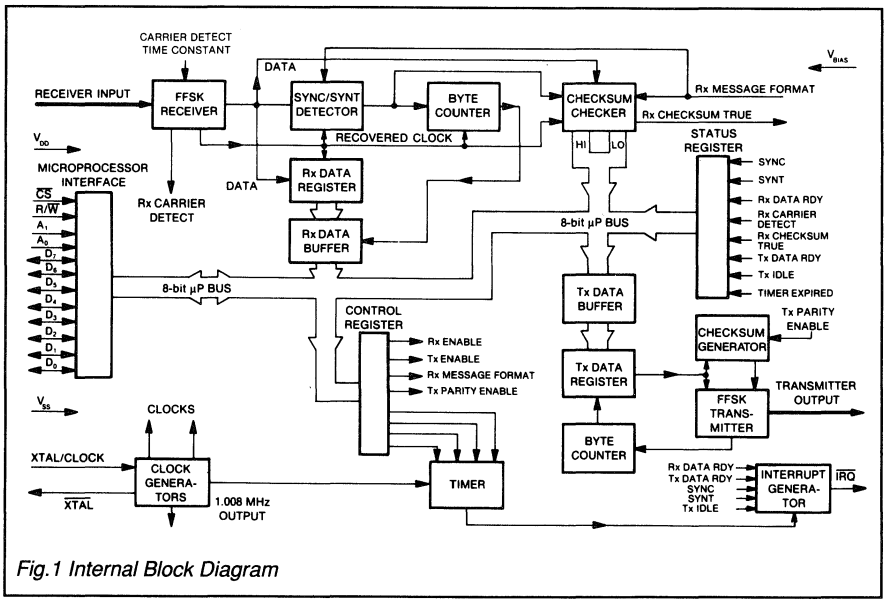


Fig.1 Internal Block Diagram

FX529

Brief Description

The FX529 is a single-chip CMOS 1200 baud FFSK Modem, designed primarily for use in trunked radio systems but may also be employed in other general purpose radio or line data communication applications.

The device has been designed to conform to the French trunked radio protocol PAA 1382

The FX529 is full duplex at 1200 baud and includes an 8-bit parallel microprocessor interface and a programmable timer which may be set for interrupt periods of between 8 and 120 bits.

Preamble data and an error-check word are automatically generated in the transmit mode.

Error checking is performed and the 16-bit SYNC word is detected in the receive mode.

An on-chip Xtal/clock generator requiring an external 4.032MHz Xtal or clock input provides all microcircuit filter sampling clocks and modem timings whilst also supplying a "Clock ÷ 4" output (1.008MHz).

The FX529, which has a powersaving facility, requires a single 5-volt power supply and is available in both cerdip DIL and plastic SMD packages.

CML Semiconductor Products
TECHNICAL INFORMATION
Digital Signalling for Mobiles

Publication D/Signalling/1 May 1988

DIGITAL SIGNALLING FORMAT FOR MOBILES

A step towards standardization of the digital transmission over mobile radio has been made with the UK recommendation of a new format. It specifies a binary format for general purpose use in applications such as selective calling and vehicle identification through to mobile printers and computer terminals. This article, written by P.J. Mabey of Philips Research Laboratories, and published in "Communications International", describes how the format has been tailored to mobile radio requirements, presents the results of performance measurements, and discusses the application of the format which has been submitted to the CCIR for consideration.

Introduction

Data transmission in mobile radio is becoming increasingly important for easing channel congestion and for the new facilities that is enables. Unfortunately it has to operate under extremely unfavourable conditions, suffering from the combined impairments of ignition noise interference from nearby vehicles, signal fading caused by multi-path propagation and shadowing, and co-channel interference which results from sharing the radio channel locally and re-using the channel in another part of

Data Format

In order to ease and encourage the introduction of data transmission in the UK the Electronic Engineering Association (EEA), an association of manufacturers, and the Home Office radio regulatory department, in consultation with mobile radio users, have recommended the binary data format illustrated in Figs.1 and 2 for mobile data communication.

This format provides a high reliability, high falsing immunity and a high throughput. It is designed for variable length messages, being suitable for short message applications such as status reporting and vehicle identification through to text transmission for mobile printers and terminals. Various data formats are already in use for specific applications of data transmission over mobile radio, for example in mobile telephony and radiopaging, but none of these formats were considered suitable as a standard for the wide range of applications expected for mobile data transmission.

Maximum benefit will be obtained by widespread use of the recommended format, and hopefully it will become established outside the UK. The format has been considered by CCIR and has now been included in a CCIR Report.

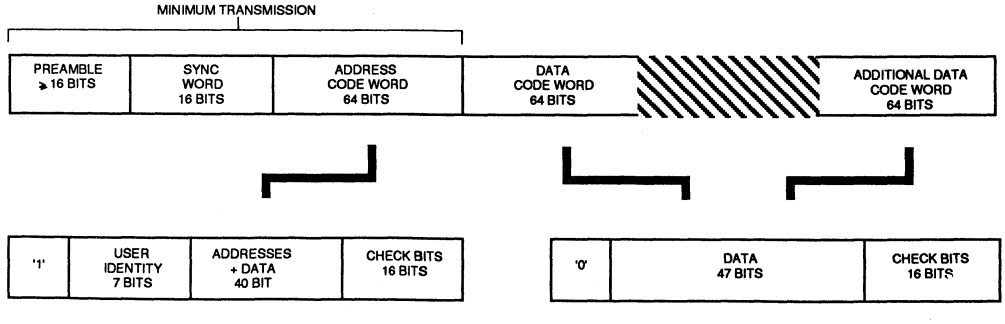


Fig. 1 Binary data format and code word structure as standardised by the EEA, for high reliability, high falsing immunity and high throughput

High Level Data Link Control (HDLC)

When choosing a data format to use on mobile radio an obvious candidate to consider is h.d.l.c. which is an international standard. We will discuss the differences between the EEA and the h.d.l.c. formats and show how the former is better suited to mobile radio. The h.d.l.c. frame is illustrated in Fig. 2. A frame comprises an eight bit start flag, a variable length code word, and an eight bit terminating flag. The terminating flag can also act as the start flag for the next frame. Each code word contains an address and control field. Because the frame length is variable, a bit stuffing scheme is used in which an extra bit is inserted whenever necessary to ensure that the flag sequence is not simulated in the transmitted data.

The error rates encountered on the mobile radio channel are so high that code words should be kept short to ensure an acceptable chance of being received error free. Consequently, many code words may be necessary to accommodate a message. With short words, the address, control and flag bytes for each word would be a severe overhead on throughput, in a medium where a high throughput is important. In contrast the EEA format puts the address and control information into only the first code word of a message, and uses a fixed length code word, which avoids the flag between words. The code words may be decoded independently and a retransmission protocol used to recover corrupted words.

The overhead of a terminating flag byte might be compensated by the reduced quantization waste of variable length code words, but variable length words with delimiting flags and bit stuffing have other disadvantages. Because the h.d.l.c. flag acts as both a frame terminator and an opener for the next frame, corruption of the flag results in the loss of two frames. If error correction is applied, a variable length code word would complicate the decoder. Further, channel errors can cause a decoder to fail to remove stuffing bits, and also mistake data for stuffing bits and wrongly remove them. As a result the decoded code word may be the wrong length, in which case the error correction procedures will be unsuccessful.

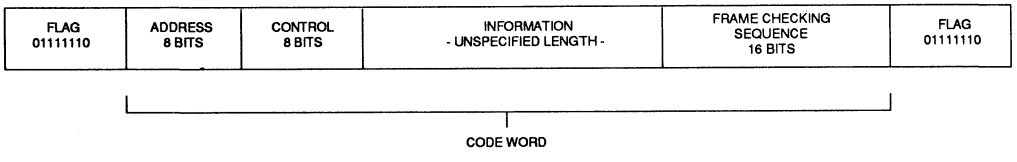


Fig.2 Structure of an h.d.l.c. frame, comprising an 8-bit start flag, a variable length code word and an 8-bit

Flag Sequence

The code used for the h.d.l.c. format ensures that code words all differ in at least four bit positions, so guaranteeing detection of up to three bit errors in a word. The EEA code guarantees detection of up to five errors, which gives it better scope for error correction.

Finally, in mobile radio where a decoder can be exposed to random bits between transmissions, an eight bit flag sequence for word synchronization would be too short for a fixed word length format without terminating flags. A simple decoder can spuriously recognize the synchronization sequence in the bits preceding a message, enter a message decoding algorithm, and so miss the real message. The probability of this is $(s + n)2^{-s} = 0.28$ for an s bit synchronization sequence ($s = 8$) and n bit code word ($n = 64$), which evidently would lead to serious degradation of the message success rate. To summarize, the EEA format is expected to have a significantly higher throughput and success rate than the h.d.l.c. format. This is important for spectrum efficiency. The format specification defines only a basic framework for sending data messages, leaving scope for flexibility in application. Decoding methods are not prescribed. An error detecting decoder can be realized quite simply, for example an encoder, decoder plus a modem have been implemented in one single chip microcomputer, and yet is sufficient for a good performance. The application of error correction will enhance the performance.

The recommended data format is illustrated in Figs. 1 and 2. A full definition is given in the EEA report. Transmissions begin with a preamble of bit reversals 1010.....10 so that the receiver data demodulator can acquire bit synchronization. Every message begins with a 16-bit synchronization word to enable the decoder to establish code word framing. The synchronization word was chosen for a high probability of detection, good correlation properties and infrequent spurious detection.

Error Detecting

Messages are transmitted in 64-bit code words comprising 48 information bits and 16 error check bits. These check bits are determined by a powerful error detecting code. The first code word of a message contains addressing information and some data, and is sufficient for short message applications such as status reporting. The suggested allocation of the 40 bits available for addresses and data, (Fig. 2) is 12 bits for address identity, 12 bits for address or identity, and 16 bits for data. For longer messages with more data such as text, additional data code words are appended as required to accommodate the message.

In order to avoid false calls, it is important not to mistake a data code word for an address code word. Therefore the format distinguishes address and data code words by a one bit flag. Address code words are partly distinguished by being always preceded by the synchronization word. However, without the flag, a data code word may be mistaken for an address code word when the check bits of the preceding code word match the synchronization word. Although only 1 in 10^5 code words are in this category, falsing could become a problem should a system send these code words frequently.

Exclusive Use

Mobile radio users commonly share a radio channel with other organizations because there are insufficient radio channels to permit exclusive use. It is important that different organizations do not accept each others' messages, so the format provides for every message to be labelled with the user's identity in shared channel operation. This identity is normally the organization's or licence holder's identity, not an individual mobile identity. The user identity occupies seven bits, but does not impose a limit of 128 users per channel, or set of channels. Different organizations operating on a common radio channel can have the same user identity if they are spaced geographically far enough apart not to interfere. Therefore, the user identities must be allocated according to a national plan; in the UK, this will be done by the Home Office. It is important to realize that co-channel interference in the form of data messages from different users sharing the same user identity can result in false calls being made.

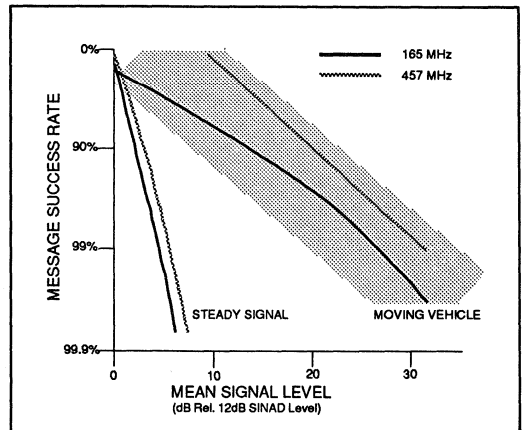


Fig.3 Message Success Rate for Short Transmisions without Data Code Words

Measurements have been made of the chance of receiving a message successfully Fig. 3 shows the message success rate when short messages without data code words were transmitted over conventional f.m. mobile radio equipment with 1200 bit/s fast frequency shift key (f.f.s.k.) data modulation and a simple error detecting decoder. The steady signal level curves were measured in the laboratory and apply to a stationary vehicle. The moving vehicle curves were measured during field tests under typical fading conditions. The EIA land mobile signalling standard RS374A specifies that a message success rate of 80% should require a steady signal level of ≤3dB, relative to the 12dB SINAD level, and that the degradation with a fading signal should be less than 20dB. The EEA format is well within these targets requiring 1dB with a steady signal and a mean level of 9dB at v.h.f (14dB at u.h.f.) with fading.

The difference in performance between moving and stationary vehicles is not as dramatic as it may seem initially. Because there is a chance that a vehicle may park where the signal is faded, a mean level of 8dB (rel. 12dB SINAD) is required to ensure that stationary vehicles have an average success rate of 80%. Further, moving vehicles benefit significantly from retransmissions, and can readily have a superior success rate to stationary vehicles.

Falsing Immunity

The falsing immunity required will depend on the particular application, and the false rates experienced will depend on the decoding method. Whatever decoding method is used there are several falsing mechanisms which must be evaluated:

False address word. Errors can corrupt an address code word into another address word, resulting in a false call.

False data word. Errors can corrupt a data code word into another data word, resulting in a false message.

Spurious calls. A call can be spuriously decoded from noise, speech or interference, when no calls is, in fact, in the process of being transmitted.

Misframed calls. Errors may corrupt the synchronization word which is then simulated in the received data, and an address code word is formed misframed, resulting in a false call.

Bit slip. A burst of noise or interference may cause bit slip in the data demodulator and data code words are decoded misframed, resulting in a false message.

Interference. Another transmission can overlap in time and substitute part of a message, so that the decoded call is a composite of wanted and interfering data words, resulting in a false message.

False Probability

The format design ensures that a simple error detecting decoder can achieve a very low false probability. For example, Fig. 3 shows the probability that a synchronization word and address code word will be decoded as a synchronization word and a different address code word. As the signal level is reduced the false rate peaks and then becomes very small at low signal levels because failure to synchronize prevents decoding. The peak false is 10^{-6} per transmitted call.

Such low false rates are impractical to measure, and so these curves are predictions from calculations and the analysis of bit error patterns recorded during mobile data transmission experiments.

The RS374A standard suggests that the level of falsing immunity is specified in one of four categories: low, medium, high and secure. The EEA format is adequate for the most stringent category, where 'secure' is defined as a false rate less than 10^{-5}.

Optimization

Addressing and handshake protocols will further reduce falsing, whereas the application of error correction will tend to increase falsing. Clearly there is much scope for optimizing decoders for specific applications and it is up to designers to demonstrate that their implementation has adequate falsing capabilities. Analysis has shown that the geographical range of mobile data systems which use the EEA format will be at least as good as the range for speech communication. A good combined high reliability and high throughputs obtained by the use of an efficient code in the format, with only 25% error check bits, and a retransmission protocol which repeats messages, but only when necessary as most vehicles will receive the initial transmission of a message.

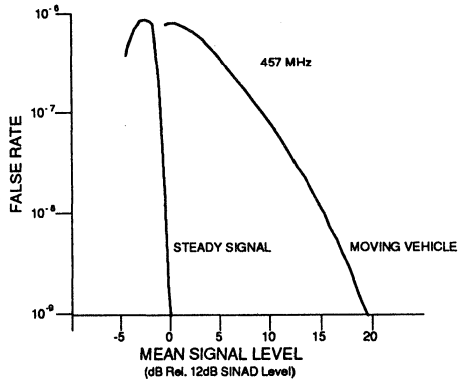


Fig.4 False Rate for Moving and Fixed Signals

Selective retransmission of only the corrupted code words is particularly efficient.

Both moving and stationary vehicles were considered in the analysis. Moving vehicles were found to have a lower throughput (e.g. 0.46 for a short text of 67 characters) than stationary vehicles (correspondingly 0.6) because they require more retransmissions. These throughputs include all the overheads of transmitter turn-on time, synchronizing and obtaining an acknowledgement. Careful application of error correction to the format will reduce the amount of retransmission and will, consequently, increase the throughput for moving vehicles.

Conclusions

The recommended binary format is the result of a desire by mobile radio manufacturers and users for digital signalling standards. For manufacturers, standardization minimizes the variety of signalling schemes to be supported, while customers can have confidence in a system which is approved and supported by several manufacturers. The format has been designed specifically to suit the characteristics of mobile radio and is flexible for a wide range of mobile applications. It is efficient, offering a good throughout. It has good falsing immunity. A simple decoder is sufficient, yet there is scope to optimize the decoder for specific applications. Reliable data communications will be possible throughout existing mobile radio service areas which were designed originally for speech communication.

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CML Semiconductor Products

PRODUCT INFORMATION

FX469 1200/2400/4800 Baud FFSK Modem

Publication D/469/3 July 1994
Provisional Issue

Features

- **Selectable Data Rates**
  1200, 2400 and 4800 Baud
- **Full-Duplex FFSK**
- **Rx and Tx Bandpass Filters**
- **Clock Recovery and Carrier Detect Facilities**
- **Rx and Tx Enable Functions**
- **Pin Selected Xtal/Clock Inputs**
  1.008MHz or 4.032MHz
- **Radio and General Applications**
  - **Data-Over-Radio**
  - **PMR and Cellular Signalling**
  - **Portable Data Terminals**
  - **Personal/Cordless Telephone**

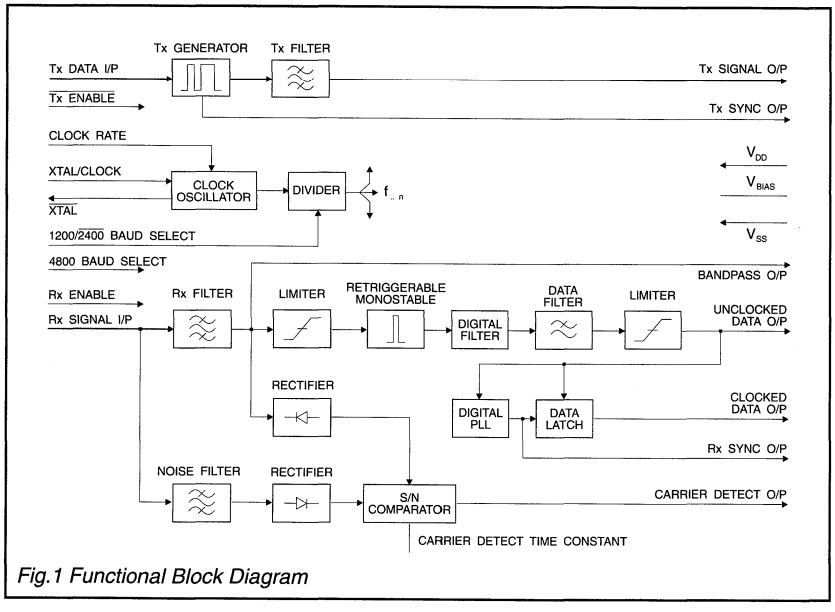


Fig.1 Functional Block Diagram

FX469

Brief Description

The FX469 is a single-chip CMOS LSI circuit which operates as a full-duplex pin-selectable 1200, 2400 or 4800 baud FFSK Modem. The mark and space frequencies are 1200/1800, 1200/2400 and 2400/4800 Hz respectively. Tone frequencies are phase continuous; transitions occur at the zero crossing point.

Employing a common Xtal oscillator with a choice of two clock frequencies (1.008MHz or 4.032MHz) to provide baud-rate, transmit frequencies, and Rx and Tx synchronization, the transmitter and receiver operate entirely independently including individual section powersave functions.

The FX469 includes on chip circuitry for Carrier Detect and Rx Clock recovery, both of which are made available as output pins.

Rx, Tx and Carrier Detect paths each contain a bandpass filter to ensure the provision of optimum signal conditions both in the modem and for the Tx modulation circuitry.

The FX469 demonstrates a high sensitivity and good bit-error-rate under adverse signal conditions; the carrier detect time constant is set by an external capacitor, whose value should be arranged as required to further enhance this product's performance in high noise environments.

This low-power device requires few external components and is available in small outline plastic (S.O.I.C) and cerdip DIL packages.

Pin Number Function

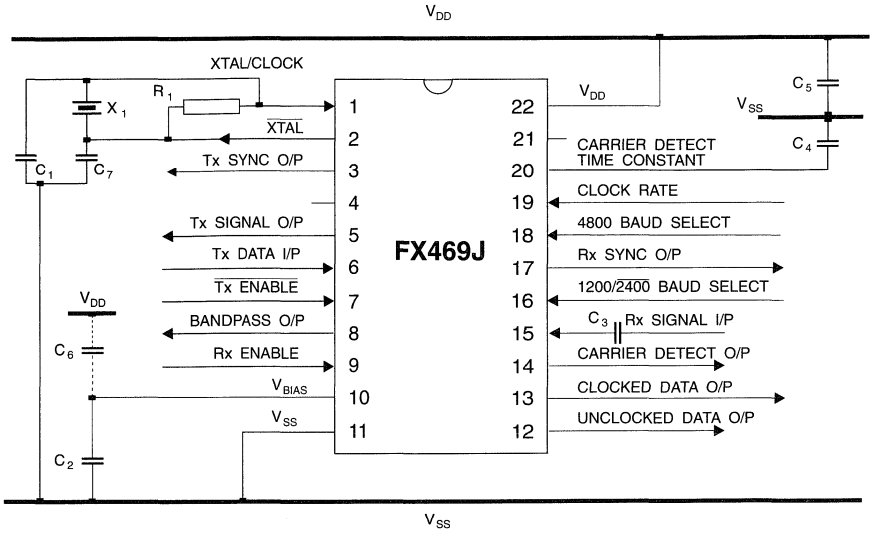
FX469 DW	FX469 J	
1	1	**Xtal/Clock :** The input to the on-chip inverter, for use with either a 1.008MHz or a 4.032MHz Xtal or external clock. Clock frequency selection is by the "Clock Rate" input pin. The selection of this frequency will affect the operational Data Rate of this device. Refer to Baud Selection information on the next page. Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/ drive failure. it is recommended that the power rail (V_{DD}) is fitted with a current limiting device (resistor or fast-reaction fuse).
2	2	**Xtal :** Output of the on-chip inverter.
3	3	**Tx Sync O/P :** A squarewave, produced on-chip, to synchronize the input of logic data and transmission of the FFSK signal (See Figure 4).
4	5	**Tx Signal O/P :** When the transmitter is enabled, this pin outputs the (140-step pseudo sinewave) FFSK signal (See Figure 4). With the transmitter disabled, this output is set to a high-impedance state.
5	6	**Tx Data I/P :** Serial logic data to be transmitted is input to this pin.
6	7	**Tx Enable :** A logic '0' will enable the transmitter (See Figure 4). A logic '1' at this input will put the transmitter into powersave whilst forcing "Tx Sync Out" to a logic '1' and "Tx Signal Out" to a high-impedance state. This pin is internally pulled to V_{DD}.
7	8	**Bandpass O/P :** The output of the Rx Bandpass Filter. This output impedance is typically 10kW and may require buffering prior to use.
8	9	**Rx Enable :** The control of the Rx function. The control of other outputs is given below.
9	10	**V_{BIAS}:** The output of the on-chip analogue bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} by a capacitor (C_2). (See Figure 2. This bias voltage is maintained under all powersave conditions.
	11	**V_{SS}:** Negative supply rail (GND).

Rx Enable	=	Rx Function	Clock Data O/P	Carrier Detect	Rx Sync Out
"1"	=	Enabled	Enabled	Enabled	Enabled
"0"	=	Powersave	"0"	"0"	1" or "0"

Pin Number FX469 DW	Pin Number FX469 J	Function
11	12	**Unclocked Data O/P:** The recovered asynchronous serial data output from the receiver.
12	13	**Clocked Data O/P:** The recovered synchronous serial data output from the receiver. Data is latched out by the recovered clock, available at the "Rx Sync O/P," (See Figure 5).
13	14	**Carrier Detect O/P:** When an FFSK signal is being received this output is a logic '1.'
14	15	**Rx Signal I/P:** The FFSK signal input for the receiver. This input should be coupled via a capacitor, C_3.
15	17	**Rx Sync O/P:** A flywheel squarewave output. This clock will synchronize to incoming Rx FFSK data (See Figure 5).
16	16	**1200/2400 Baud Select:** A logic '1' on this pin selects the 1200 baud option. Tone frequencies are: one cycle of 1200Hz represents a logic '1,' one-and-a-half cycles of 1800Hz represents a logic '0.' A logic '0' on this pin selects the 2400 baud option. Tone frequencies are: one-half cycle of 1200Hz represents a logic '1,' one cycle of 2400Hz represents a logic '0.' This function is also used, in part, to select the 4800 baud option. This pin has an internal 1MΩ pullup resistor. **Operational Data Rate Configurations** are illustrated in the table below.
17	18	**4800 Baud Select:** A logic '1' on this pin combined with a logic '0' on the 1200/2400 Baud Select pin will select the 4800 option (1MΩ pulldown resistor). Tone frequencies are: one-half cycle of 2400Hz represents a logic '1,' one cycle of 4800Hz represents a logic '0.' This state can only be achieved using a 4.032MHz Xtal input.
18	19	**Clock Rate:** A logic input to select and allow the use of either a 1.008MHz or 4.032MHz Xtal/clock. Logic '1' = 4.032MHz, logic '0' = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).
19	20	**Carrier Detect Time Constant :** Part of the carrier detect integration function. The value of C_4 connected to this pin will affect the carrier detect response time and hence noise performance (See Figure 2, Note 3).
20	22	V_{DD}: Positive supply rail. A single 5-volt supply is required.
	4, 21	No internal connection, do not use.

Xtal/Clock Frequency	1.008MHz		4.032MHz		
Clock Rate pin	0	0	1	1	1
1200/2400 Select pin	1	0	1	0	0
4800 Select pin	0	0	0	0	1
Baud Rate	**1200**	**2400**	**1200**	**2400**	**4800**

Application Information



Component	Value	Tolerance
R_1	1.0MW	±10%
C_1	33.0pF	
C_2	1.0µF	±20%
C_3	0.1µF	
C_4	0.1µF	±10%
C_5	1.0µF	±20%
C_6	1.0µF	
C_7	33.0pF	
X_1	1.008MHz or 4.032MHz	See 'Clock-Rate' Pin

Notes

1. V_{BIAS} may be decoupled to V_{SS} and V_{DD} using C_2 and C_6 when input signals are referenced to the V_{BIAS} pin. For input signals referenced to V_{SS}, decouple V_{BIAS} to V_{SS} using C_2 only.
2. Use C_5 when input signals are referenced to V_{SS}, to decouple V_{DD}.
3. The value of C_4 determines the Carrier Detect time constant. A long time constant results in improved noise immunity but increased response time. C_4 may be varied to trade-off response time for noise immunity.
4. C_7 reduces Xtal voltage overshoot. Refer to CML Xtal Application Note D/XT/1 April 1986.

Fig.2 External Components

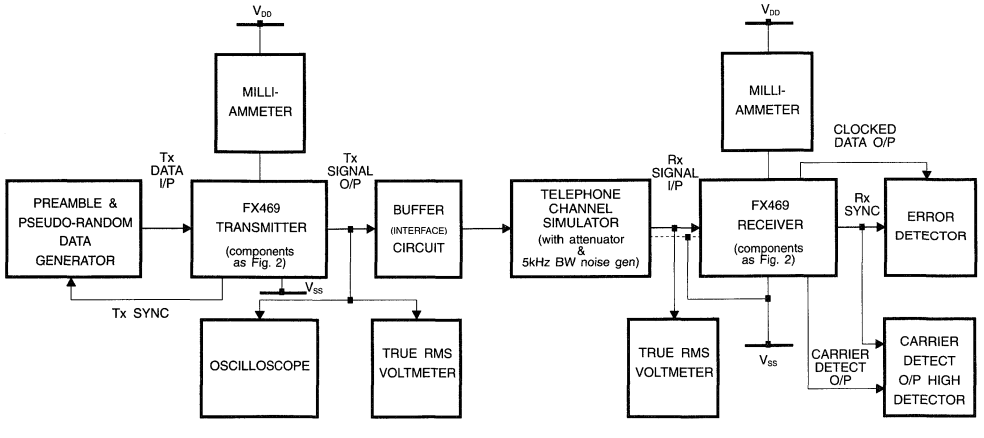


Fig.3 Suggested FX469 Test Set-Up

Application Information .....

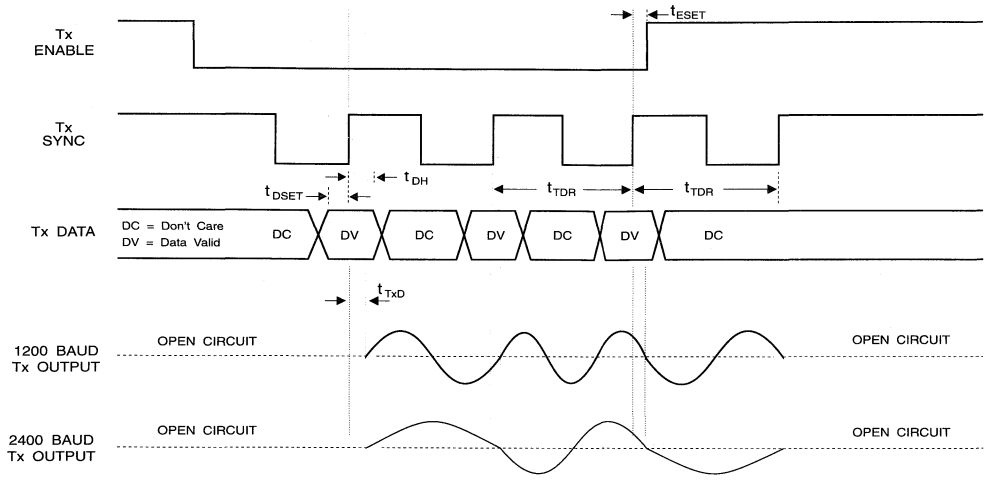


Fig.4 Transmitter Timing

Characteristics		Note	Min.	Typ.	Max.	Unit
Tx Delay, Signal to Disable Time	t_{ESET}	3	2.0	-	800	µs
Data Set-Up Time	t_{DSET}	1	2.0	-	-	µs
Data Hold Time	t_{DH}		2.0	-	-	µs
Tx Delay to O/P Time	t_{TxD}		-	1.2	-	µs
Tx Data Rate Period	t_{TDR}	3	-	833	-	µs
Rx Data Rate Period	t_{RDR}	3	800	-	865	µs
Undetermined State			-	-	2.0	µs
Internal Rx Delay	t_{ID}		-	1.5	-	ms

1. Consider the Xtal/Clock tolerance.
2. All Tx timings are related to the Tx Sync Output.
3. 1200 baud example.

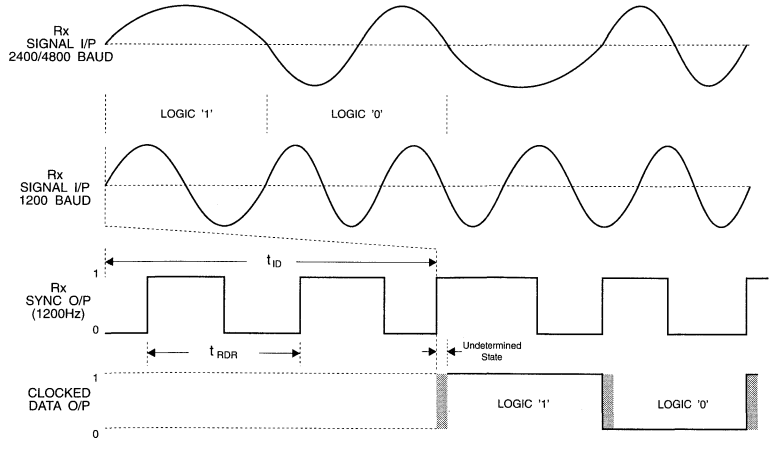


Fig.5 Rx Timing Diagram

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX469DW**	-30°C to +70°C (plastic)
	FX469J	-30°C to +85°C (cerdip)
Storage temperature range:	**FX469DW**	-40°C to +85°C (plastic)
	FX469J	-55°C to +125°C (cerdip)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:
V_{DD} = 5.0V, T_{AMB} = 25°C. Audio Level 0dB ref: = 300mVrms. Xtal/Clock = 4.032MHz.
Signal-to-Noise Ratio measured in the Bit-Rate Bandwidth Baud Rate = 1200 baud.

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage			4.5	5.0	5.5	V
Supply Current	Rx Enabled Tx Disabled		-	3.6	-	mA
	Rx and Tx Enabled		-	4.5	-	mA
	Rx and Tx Disabled		-	650	-	µA
Logic '1' Level		1	4.0	-	-	V
Logic '0' Level		1	-	-	1.0	V
Digital Output Impedance			-	4.0	-	kΩ
Analogue and Digital Input Impedance			100	-	-	kΩ
Tx Output Impedance			-	0.6	1.0	kΩ
On-Chip Xtal Oscillator						
	R_{IN}		10.0	-	-	MΩ
	R_{OUT}		5.0	-	15.0	kΩ
Inverter d.c. Voltage Gain			10.0	-	20.0	V/V
Gain Bandwidth Product			4.1	-	-	MHz
Xtal Frequency		2	-	1.008	-	MHz
Xtal Frequency		2	-	4.032	-	MHz
Dynamic Values						
Receiver						
Signal Input Dynamic Range	SNR = 50dB	3, 4	100	230	1000	mVrms
Bit Error Rate	SNR = 12dB	4				
	1200 Baud		-	2.5	-	10^{-4}
	2400 Baud		-	1.5	-	10^{-3}
	4800 Baud		-	1.5	-	10^{-3}
	SNR = 20dB	4				
	1200/2400/4800 Baud		-	<1.0	-	10^{-8}
Receiver Synchronization	**SNR =12dB**	7				
Probability of Bit 16 Being Correct			-	0.995	-	
Carrier Detect		5, 10				
Sensitivity		7, 8	-	-	150	mVrms
Probabilty of C.D. Being High						
After Bit 16	SNR = 12dB	5, 9		0.995		
0dB Noise	No Signal	9		0.01		

Specification .....

Characteristics		See Note	Min.	Typ.	Max.	Unit
Transmitter Output						
Tx Output Level			-	775	-	mVrms
Output Level Variation						
1200/1800Hz or 1200/2400Hz or 2400/4800Hz			0	-	±1.0	dB
Output Distortion			-	3.0	5.0	%
3rd Harmonic Distortion			-	2.0	3.0	%
Logic '1' Carrier Frequency	1200 Baud	6	-	1200	-	Hz
	2400 Baud	6	-	1200	-	Hz
	4800 Baud	6	-	2400	-	Hz
Logic '0' Carrier Frequency	1200 Baud	6	-	1800	-	Hz
	2400 Baud	6	-	2400	-	Hz
	4800 Baud	6	-	4800	-	Hz
Isochronous Distortion						
1200Hz - 1800Hz/1800Hz - 1200Hz			-	25.0	40.0	µs
1200Hz - 2400Hz/2400Hz - 1200Hz			-	20.0	30.0	µs
2400Hz - 4800Hz/4800Hz - 2400Hz				-	10.0	20 µs

Notes

1. With reference to V_{DD} = 5.0 volts.
2. Xtal frequency, type and tolerance depends upon system requirements.
3. See Figure 5 (variation of BER with Input Signal Level).
4. SNR = Signal-to-Noise Ratio in the Bit-Rate Bandwidth.
5. See Figure 2.
6. Dependent upon Xtal tolerance.
7. 10101010101 ...01 pattern.
8. Measured with a 150mVrms input signal (no noise); 1200/2400 baud operation.
9. Reference (0dB) level for C.D. probability measurements is 230mVrms.
10. For 1200 and 2400 baud operation only; when operating at 4800 baud the Carrier Detect output should be ingnored.

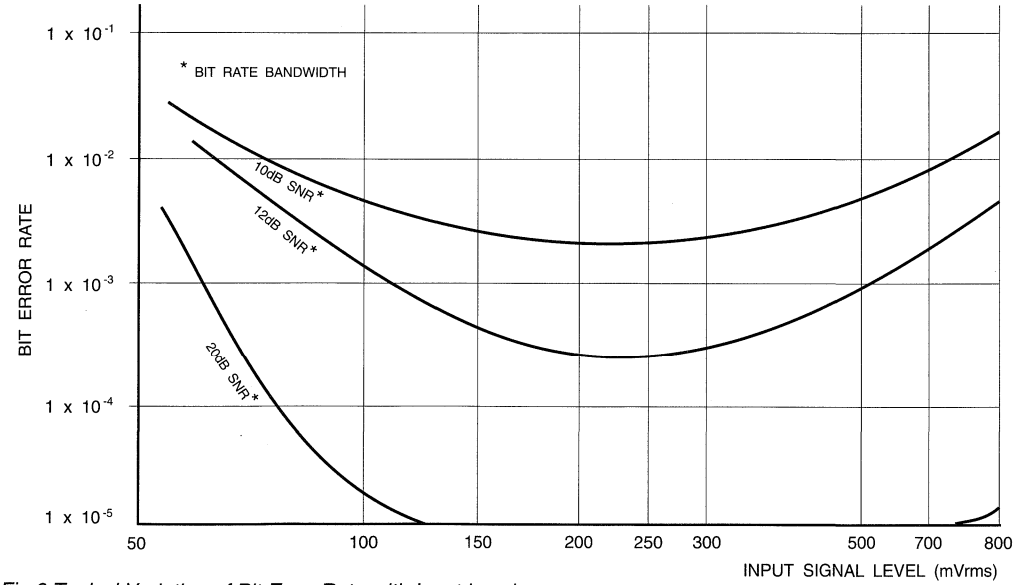


Fig.6 Typical Variation of Bit Error Rate with Input Level

Application Information

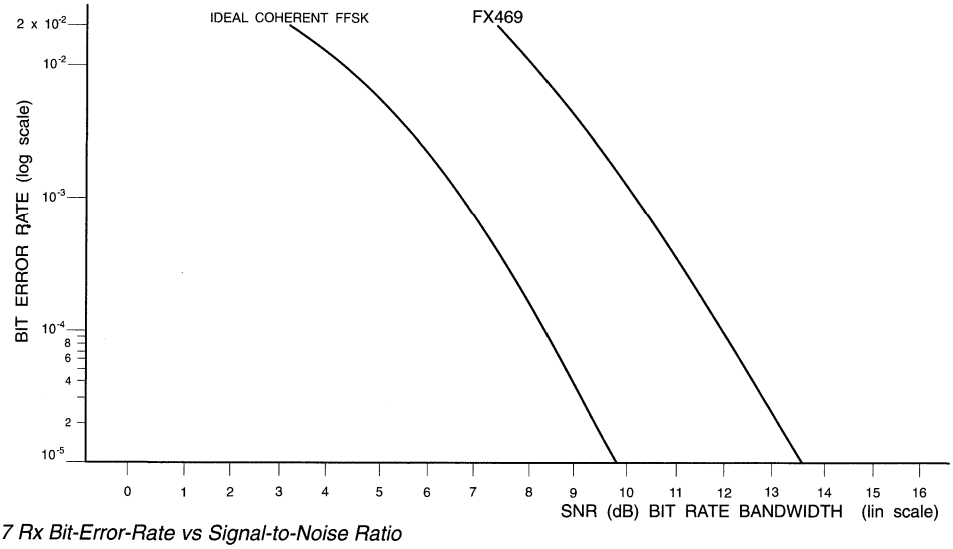


Fig.7 Rx Bit-Error-Rate vs Signal-to-Noise Ratio

Package Outlines

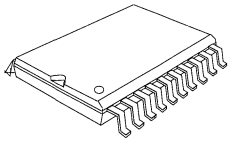
The FX469 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX469 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX469DW 20-pin plastic S.O.I.C. (D3)

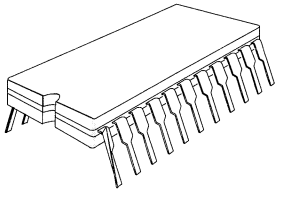
NOT TO SCALE



Max. Body Length 12.85mm
Max. Body Width 7.59mm

FX469J 22-pin cerdip DIL (J3)

NOT TO SCALE



Max. Body Length 27.38mm
Max. Body Width 9.75mm

Ordering Information

FX469DW 20-pin surface mount S.O.I.C.
FX469J 22-pin cerdip DIL

CML Semiconductor Products

PRODUCT INFORMATION

FX589 Low-Voltage/High-Speed GMSK Modem

Publication D/589/3 July 1994
Provisional Issue

Features

- **Full-Duplex Gaussian Minimum Shift Keying (GMSK)**
  Operating from 3 Volts to 5.5 Volts
- **Data Rates 4kb/s to 40kb/s**
- **Selectable BT (0.3 or 0.5)**
- **Low-Current Analogue/Digital Non-DSP Solution**
- **Meets RCR STD-18**

Applications

- **Wireless LAN/Modems**
- **Handy Data Terminals**
- **Low-Power Wireless Data Link for PCs, Laptops and Printers**
- **Point-Of-Sale Terminals**
- **Wireless Bar-Code Readers and Stock Controllers**

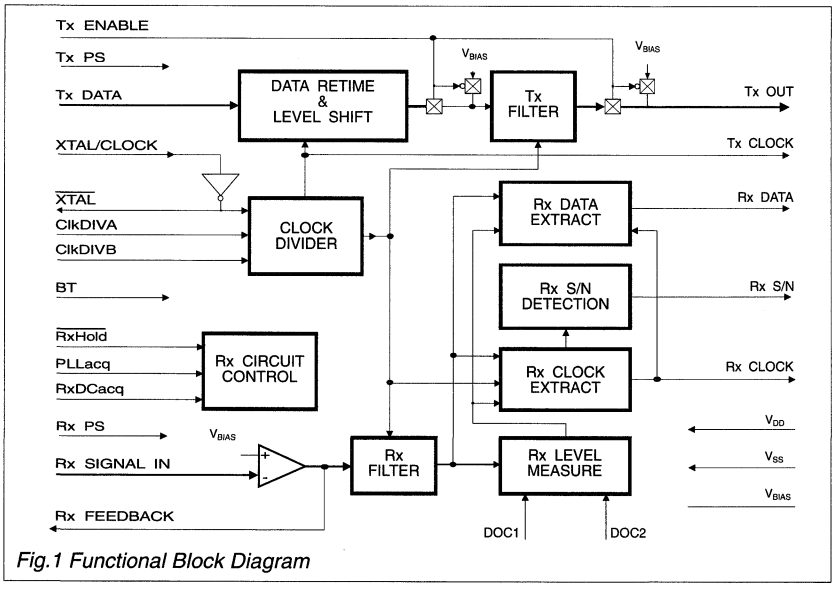


Fig.1 Functional Block Diagram

FX589

Brief Description

The FX589 is a single-chip modem employing Gaussian Minimum Shift Keying (GMSK) modulation.

Data rates of 4kb/s to 40kb/s and the choice of BT to 0.3 or 0.5 are pin-programmable functions to suit radio data channel bandwidth requirements.

The Rx and Tx digital data interfaces are bit-serial and synchronised to Rx and Tx data clocks generated by the modem. Separate Rx and Tx Powersave/ Enable inputs allow for full- or half-duplex operation.

Rx input levels can be set by a suitable ac and dc level adjusting circuit built, with external components, around an on-chip Rx input amplifier.

Acquisition, lock and hold of Rx data signals is made easier and faster by the use of Rx Control Inputs to clamp, detect and/or hold input data levels and can be set by the system µProcessor as required.

Indication is available, from the Rx S/N output, as to the quality of the received signal.

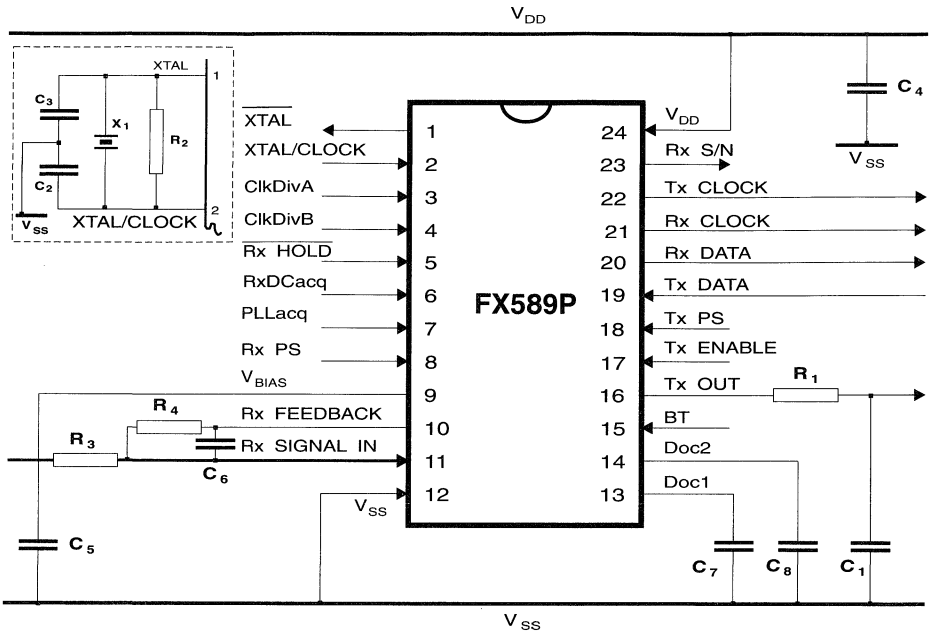
The FX589 design features a low-current analogue/ digital ASIC process offering significantly lower current consumption than DSP technology. For data rates up to 20kb/s the FX589 draws typically 1.5mA at 3.0 volts V_{DD} and for data rates up to 40kb/s at 5.0 volts, typically 4.0mA.

This low-power CMOS microcircuit is available in both 24-pin plastic DIL and Small Outline (S.O.I.C.) packages.

Pin Number FX589DW FX589P	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	**Xtal/Clock:** The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock (f_{XTAL}) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the $\overline{\text{Xtal}}$ pin left unconnected. Note that operation of the FX589 without a suitable Xtal or clock input may cause device damage.
3	**ClkDivA:** Two logic level inputs that control the internal clock divider and hence the transmit and receive data rate. See Table 1.
4	**ClkDivB:**
5	**$\overline{\text{Rx Hold}}$:** A logic "0" applied to this input will 'freeze' the Clock Extraction and Level Measurement circuits unless they are in 'acquire' mode.
6	**RXDCacq:** A logic "1" applied to this input will set the Rx Level Measurement circuitry to the 'acquire' mode.
7	**PLLacq:** A logic "1" applied to this input will set the Rx Clock Extraction circuitry to 'acquire' mode (see Table 2).
8	**Rx PS:** A logic "1" applied to this input will powersave all receive circuits except for "Rx Clock" output (which will continue at the set bit-rate) and cause the "Rx Data" and "Rx S/N" outputs to go to a logic "0".
9	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to V_{SS} by a capacitor mounted close to the pin.
10	**Rx Feedback:** The output of the Rx Input Amplifier/the input to the Rx Filter.
11	**Rx Signal In:** The input to Rx Input Amplifier.
12	**V_{SS}:** Negative supply rail. Signal ground.

Pin Number FX589DW FX589P	Function
13	**Doc1:** Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from each pin to V_{SS}. See Figure 2.
14	**Doc2:**
15	**BT:** A logic level to select the modem 'BT' (the ratio of the Tx Filter's -3dB frequency to the Bit-Rate). A logic "1" sets the modem to a BT of 0.5, a logic "0" to a BT of 0.3.
16	**Tx Out:** The Tx signal output from the FX589 GMSK Modem.
17	**Tx Enable:** A logic "1" applied to this input enables the transmit data path through the Tx Filter to the "Tx Out" pin. A logic "0" will put the "Tx Out" pin to V_{BIAS} via a high impedance.
18	**Tx PS:** A logic "1" applied to this input will powersave all transmit circuits except for the "Tx Clock".
19	**Tx Data:** The logic level input for the data to be transmitted. This data should be synchronous with the "Tx Clock".
20	**Rx Data:** A logic level output carrying the received data, synchronous with the "Rx Clock".
21	**Rx Clock:** A logic level clock output at the received data bit-rate.
22	**Tx Clock:** A logic level clock output at the transmit-data rate.
23	**Rx S/N:** A logic level output which may be used as an indication of the quality of the received signal.
24	**V_{DD}:** Positive supply rail. A single, stable power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin.

Application Information



External Components

Component	Value	Tolerance	Component	Value	Tolerance
R_1	Note 1	±5%	C_3	Note 5	
R_2	1.0MΩ	±10%	C_4	100nF	±20%
R_3	Note 2	±10%	C_5	1.0µF	±20%
R_4	100kΩ	±10%	C_6	22.0pF	±20%
C_1	Note 1	±10%	C_7	Note 4	
C_2	Note 5		C_8	Note 4	
			X_1	Note 3	

Fig.2 Recommended External Components

Notes

1. The RC network formed by R_1 and C_1 is required between the Tx Out pin and the input to the modulator. This network, which can form part of any dc level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering.
   The ground connection to the capacitor C_1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.
   The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:
   BT of 0.3 = 0.34/bit rate (bits/second)
   BT of 0.5 = 0.22/bit rate (bits/second)
   - with suitable values for common bit rates being:

		R_1	C_1
8,000 bits/sec	BT = 0.3	91.0kΩ	470pF
4,800 bits/sec	BT = 0.5	100kΩ	470pF
9,600 bits/sec	BT = 0.5	47.0kΩ	470pF
32,000 bits/sec	BT = 0.3	47.0kΩ	220pF
32,000 bits/sec	BT = 0.5	47.0kΩ	150pF
38,400 bits/sec	BT = 0.3	47.0kΩ	180pF
38,400 bits/sec	BT = 0.5	47.0kΩ	120pF

   Note that in all cases, the value of R_1 should be not less than 47.0kΩ and that the calculated value of C_1 includes calculated parasitic (circuit) capacitances.
2. R_3, R_4 and C_6 form the gain components for the Rx Input signal. R_3 should be chosen as required by the signal input level.
3. The FX589 can operate correctly with Xtal/Clock frequencies between 1.0MHz and 6.5MHz; see Table 1 for examples. Operation of this device without a Xtal or Clock input may cause device damage.
4. C_7 and C_8 should both be 15.0nF for a data rate of 8kb/s, and inversely proportional to the data rate for other data rates, e.g. 30.0nF at 4kb/s, 3.0nF at 40kb/s.
5. The value chosen for C_2 and C_3 (including stray capacitances) should be suitable for the applied V_{DD} and the frequency of X_1.
   As a guide: At 5 volts, $C_2 = C_3 = 33.0$pF at 1.0MHz falling to 18pF at 6.5MHz.
   At 3 volts, $C_2 = C_3 = 33.0$pF falling to 18pF at 5.0MHz. The equivalent series resistance of X_1 should be less than 2.0kΩ falling to 150Ω at the maximum frequency. Stray capacitance on the Xtal/clock circuit pins must be minimised.

Application Information .....

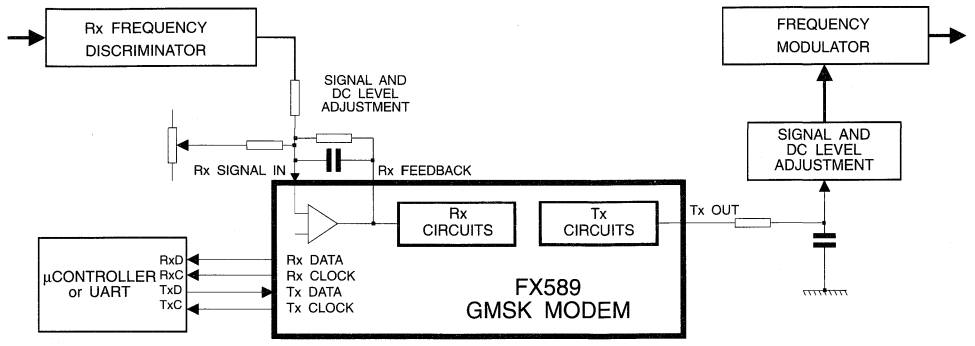


Fig.3 External Signal Paths

Clock Oscillator and Dividers

The Tx and (nominal) Rx data rates are determined by division of the frequency present at the Xtal pin, which may be generated by the on-chip Xtal oscillator or be derived from an external source. Any Xtal/clock frequency in the range 1.0MHz to 5.0MHz (V_{DD} = 3.0V) or 1.0MHz to 6.5MHz (V_{DD} = 5.0V) may be employed, depending upon the desired data rate.

A division ratio to facilitate data-rate setting is controlled by the logic level inputs on the ClkDivA/B pins, and is shown in Table 1 (below) - together with examples of how various 'standard' data-rates may be derived from common µP or Xtal frequencies.

$$\text{Data Rate} = \frac{\text{Xtal/Clock Frequency}}{\text{Division Ratio (ClkDivA/B)}}$$

***Note** that device operation is not guaranteed or specified above 40,000 bits/s or below 4,000 bits/s at the relevant supply voltage*			**Xtal/Clock Frequency (MHz)**			
			4.096 [12.288/3]	4.9152	2.048 [6.144/3]	2.4576 [12.288/5]
Inputs **ClkDiv A**	**ClkDiv B**	**Division Ratio: Xtal Freq / Data Rate**	**Data Rate (b/s)**			
0	0	128	32000	38400	16000	19200
0	1	256	16000	19200	8000	9600
1	0	512	8000	9600	4000	4800
1	1	1024	4000	4800		

Table 1 Clock/Data Rates

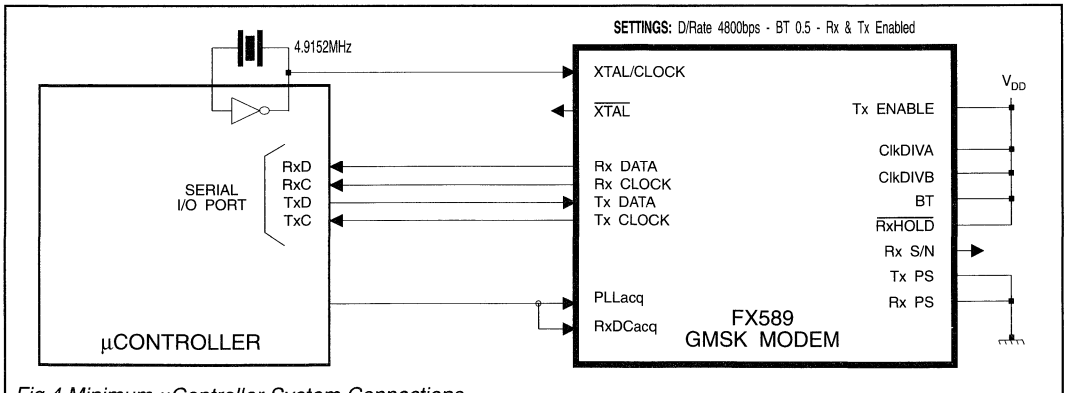


Fig.4 Minimum µController System Connections

Application Information .....

Rx Signal Path Description

The function of the Rx circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide dc level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide Rx data in a binary form.
6. Assess signal quality and provide Signal-to-Noise information.

The output of the radio receiver's Frequency Discriminator should be fed to the FX589's Rx Filter via a suitable gain and dc level adjusting circuit. This gain circuit can be built, with external components, around the on-chip Rx Input Amplifier, with the gain set so that the signal level at the Rx Feedback pin is nominally 1-volt peak-to-peak (for V_{DD} = 5.0 V) centred around V_{BIAS} when receiving a continuous "1111000011110... " data pattern.

Positive going signal excursions at Rx Feedback pin will produce a logic "0" at the Rx Data Output. Negative going excursions will produce a logic "1."

The received signal is fed through the lowpass Rx Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors. One of which measures the amplitude of the 'positive' parts of the received signal; the other measures the amplitude of the 'negative' portions. External capacitors are used by these detectors, via the Doc 1/2 pins, to form voltage- 'hold' or 'integrator' circuits. Results of the two measurements are then processed to establish the optimum dc level decision-thresholds for the Clock and Data extraction, depending upon the Rx signal amplitude, BT and any dc offset present.

Rx Circuit Control Modes

The operating characteristics of the Rx Level Measurement and Clock Extraction circuits are controlled, as shown in Table 2, by logic level inputs applied to the 'PLLacq,' '$\overline{\text{Rx Hold}}$' and 'RxDCacq' pins to suit a particular application, or to cope with changing reception conditions.

With reference to Figure 5, the Rx Mode Control diagram: In general, a data transmission will begin with a preamble of, for example, "1100110011001100," to allow the receive modem to establish timing -and level-lock- as quickly as possible. After the Rx carrier has been detected, and during the time that the preamble is expected, the 'RxDCacq' and 'PLLacq' inputs should be switched from a logic "0 to 1" so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The '$\overline{\text{Rx Hold}}$' input should normally be held at a logic "1" while data is being received, but may be driven to a logic "0" to freeze the Level Measuring and Clock Extraction circuits during a fade. If the fade lasts for less than 200 bit periods, normal operation can be resumed by returning the '$\overline{\text{Rx Hold}}$' input to a logic "1" at the end of the fade. For longer fades, it may be better to reset the Level Measuring circuits by placing the 'RxDCacq' to a logic "1" for 10 to 20 bit periods.

'$\overline{\text{Rx Hold}}$' has no effect on the Level Measuring circuits while 'RxDCacq' is at a logic "1", and has no effect on the PLL while 'PLLacq' is at a logic "1".

A logic "0" on '$\overline{\text{Rx Hold}}$' does not disable the 'Rx Clock' output, and the Rx Data Extraction and S/N Detector circuits will continue to operate.

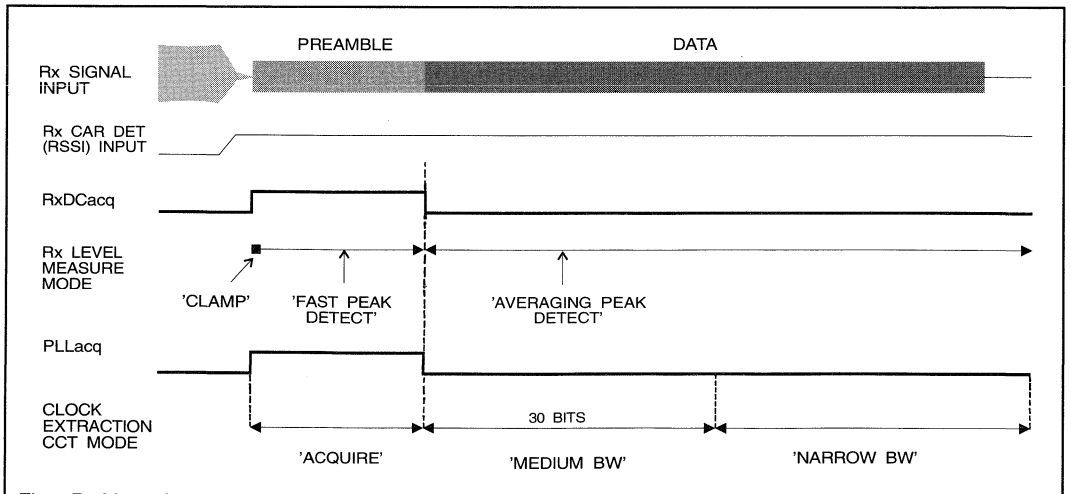


Fig.5 Rx Mode Control Diagram

Application Information .....

PLLacq	$\overline{\text{Rx Hold}}$	PLL Action
"1"	X	**Acquire:** Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. This mode will operate as long as PLLacq is a logic "1".
"1" to "0"	"1"	**Medium Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±1/16th bit-period for every two received zero-crossings. The PLL operates in this mode for a period of about 30 bits immediately following a "1" to "0" transition of the PLLacq input, provided that the $\overline{\text{Rx Hold}}$ input is a logic "1".
"0"	"1"	**Narrow Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±1/64th bit-period for every two received zero-crossings. The PLL operates in this mode whenever the $\overline{\text{Rx Hold}}$ Input is a logic "1" and PLLacq has been a logic "0" for at least 30 bit periods (after Medium Bandwidth operation for instance).
"0"	"0"	**Hold:** The PLL feedback loop is broken, allowing the Rx Clock to freewheel during signal fade periods.
RxDCacq	**$\overline{\text{Rx Hold}}$**	**Rx Level Measure Action**
"0" to "1"	X	**Clamp:** Operates for one bit-time after a "0" to "1" transition of the RxDCacq input. The external capacitors are rapidly charged towards a voltage mid-way between the received signal input level and V_{BIAS}, with the charge time-constant being of the order of 0.5bit-time.
"1"	X	**Fast Peak Detect:** The voltage detectors act as peak-detectors, one capacitor is used to capture the 'positive'-going signal peaks of the Rx Filter output signal and the other capturing the 'negative'-going peaks. The detectors operate in this mode whenever the RxDCacq input is at a logic "1," except for the initial 1-bit Clamp-mode time.
"0"	"1"	**Averaging Peak Detect:** Provides a slower but more accurate measurement of the signal peak amplitudes.
"0"	"0"	**Hold:** The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000bits] towards V_{BIAS}).

Table 2 PLL and Rx Level Measurement Operational Modes *X = don't care*

Rx Clock Extraction

Synchronized by a phased locked loop (PLL) circuit to zero-crossings of the incoming data, the 'Rx Clock Extraction' circuitry controls the 'Rx Clock' output. The Rx Clock is also used internally by the Data Extraction circuitry. The PLL parameters can be varied by the 'Rx Circuit Control' inputs PLLacq and Rx Hold to operate in one of four PLL modes as described in Table 2.

Rx Data Extraction

The 'Rx Data Extraction' circuit decides whether each received bit is a "1" or "0" by sampling the output of the Rx Filter in the middle of each bit-period, and comparing the sampled voltage against a threshold derived from the 'Level Measuring' circuit. This threshold is varied on a bit-by-bit basis to compensate for intersymbol interference depending on the chosen BT. The extracted data is output from the 'Rx Data' pin, and should be sampled externally on the rising edge of the 'Rx Clock.'

Rx S/N Detection

The 'Rx S/N Detector' system classifies the incoming zero-crossings as GOOD or BAD depending upon the time when each crossing actually occurs with respect to its expected time as determined by the Clock Extraction PLL. This information is then processed to provide a logic level output at the 'Rx S/N' pin; a 'high' level indicates a series of GOOD crossings, a 'low' level indicates a BAD crossing.

By averaging this output it is possible to derive a measure of the Signal-to-Noise-Ratio and hence the Bit-Error-Rate of the received signal.

Application Information .....

Bit Error Rate Performance

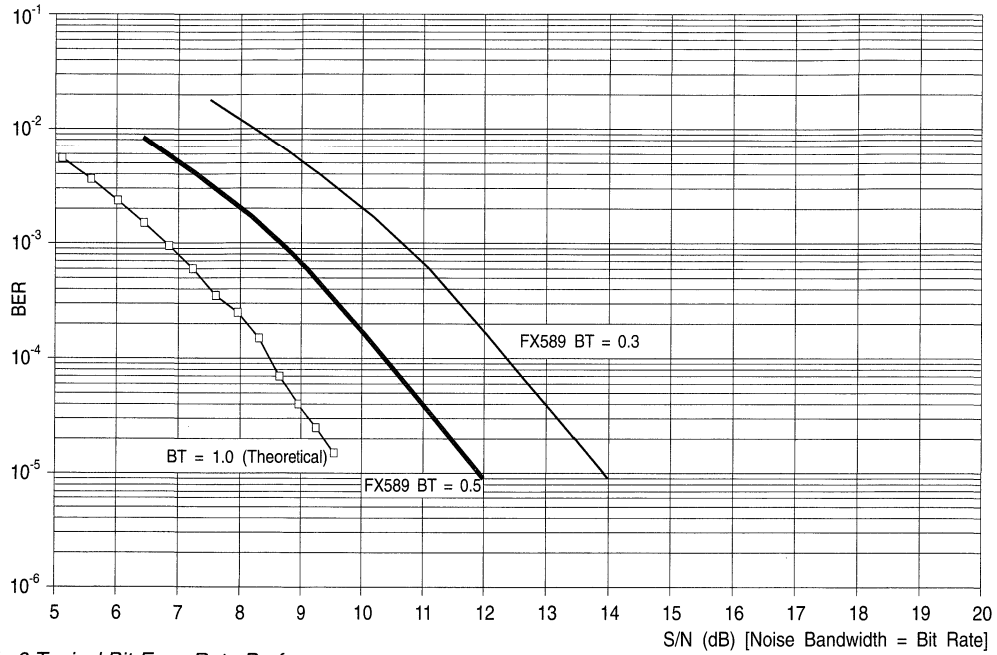


Fig.6 Typical Bit-Error-Rate Performance

Rx Signal Quality

Figure 7 shows, diagrammatically, the effect of input Rx signal quality on the "Rx S/N" output.

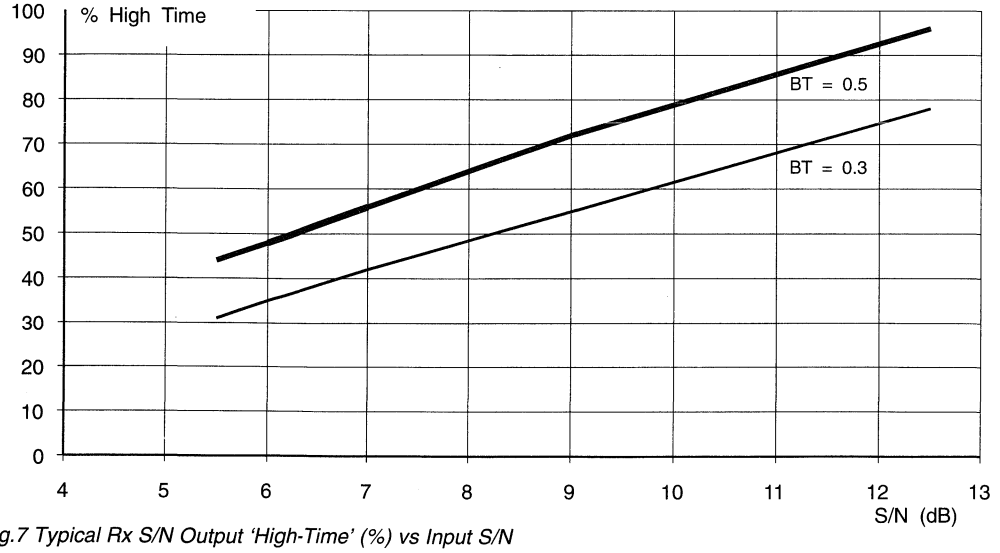


Fig.7 Typical Rx S/N Output 'High-Time' (%) vs Input S/N

Application Information .....

Tx Signal Path Description

The binary data applied to the 'Tx Data' input is re-timed within the chip on each rising edge of the 'Tx Clock' and then converted to a 1-volt peak-to-peak binary signal centred about V_{BIAS} (for V_{DD} = 5.0 V).

If the 'Tx Enable' input is 'high,' then this internal binary signal will be connected to the input of the lowpass Tx Filter, and the output of the filter connected to the 'Tx Out' pin.

Tx Enable	Tx Filter Input	Tx Out Pin
"1" (high)	$^{VDD}/_{5}$volt p-p Data In	Filtered Data
"0" (low)	V_{BIAS}	V_{BIAS} via 500kΩ

A 'low' input to the 'Tx Enable' will connect the input of the Tx Filter to V_{BIAS}, and disconnect the 'Tx Out' pin from the filter, connecting it instead to V_{BIAS} through a high resistance (nominally 500kΩ).

The Tx Filter has a lowpass frequency response, which is approximately gaussian in shape as shown in Figure 9, to minimise amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels. The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation-vs-frequency response of the transmit filtering provided by the FX589 have been designed to meet the specifications for most GMSK modem systems, having a -3dB bandwidth switchable between 0.3 and 0.5 times the data bit-rate (BT).

Note that an external RC network is required between the 'Tx Out' pin and the input to the Frequency Modulator (see Figures 2 and 3). This network, which can form part of any dc level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering, and the ground connection to the capacitor C_1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:

BT of 0.3 = 0.34/bit rate (bits/second)

BT of 0.5 = 0.22/bit rate (bits/second)

with suitable values for common bit rates being:

Data Rate	BT	R_1	C_1
8,000 bits/sec	BT = 0.3	91.0kΩ	470pF
4,800 bits/sec	BT = 0.5	100kΩ	470pF
9,600 bits/sec	BT = 0.5	47.0kΩ	470pF
32,000 bits/sec	BT = 0.3	47.0kΩ	220pF
32,000 bits/sec	BT = 0.5	47.0kΩ	150pF
38,400 bits/sec	BT = 0.3	47.0kΩ	180pF
38,400 bits/sec	BT = 0.5	47.0kΩ	120pF

The signal at 'Tx Out' is centred around V_{BIAS}, going positive for logic "1" (high) level inputs to the 'Tx Data' input and negative for logic "0" (low) inputs.

When the transmit circuits are put into a 'powersave' mode (by a logic "1" to the 'Tx PS' pin) the output voltage of the Tx Filter will go to V_{SS}. When power is subsequently restored to the Tx Filter, its output will take several bit-times to settle. The 'Tx Enable' input can be used to prevent these abnormal voltages from appearing at the 'Tx Out' pin.

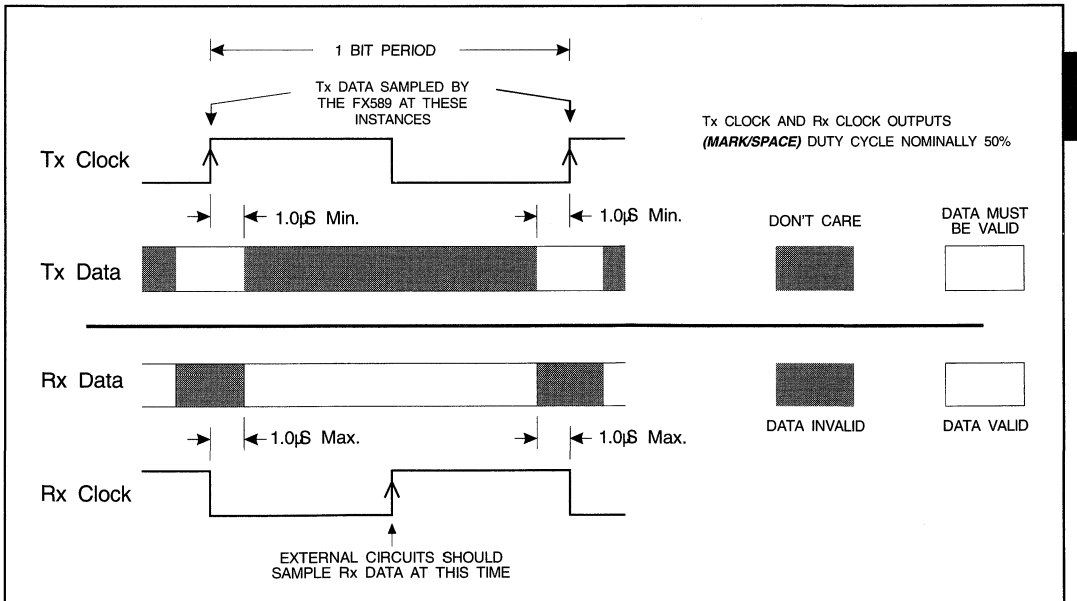


Fig.8 Rx and Tx Clock Data Timings

Application Information .....

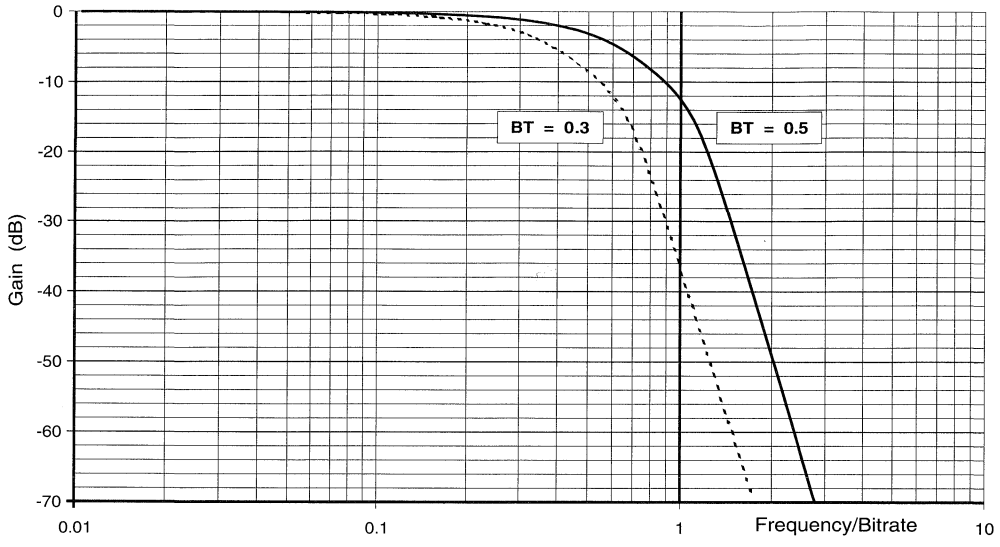


Fig.9 Tx Filter Response

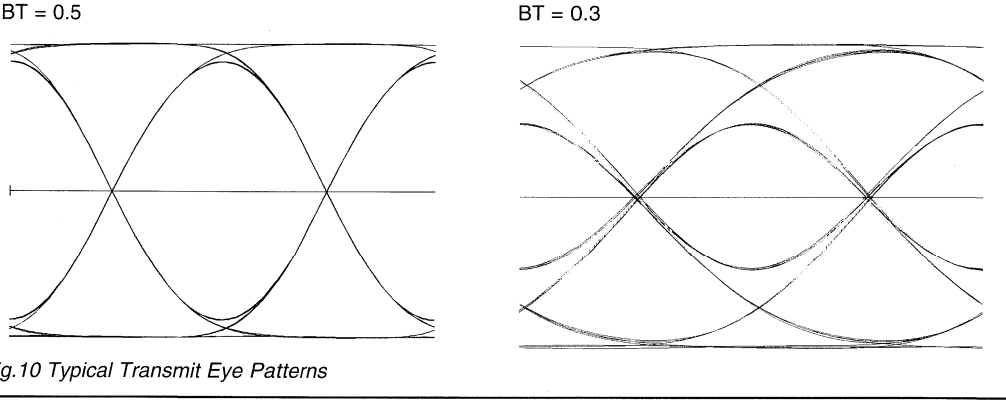


Fig.10 Typical Transmit Eye Patterns

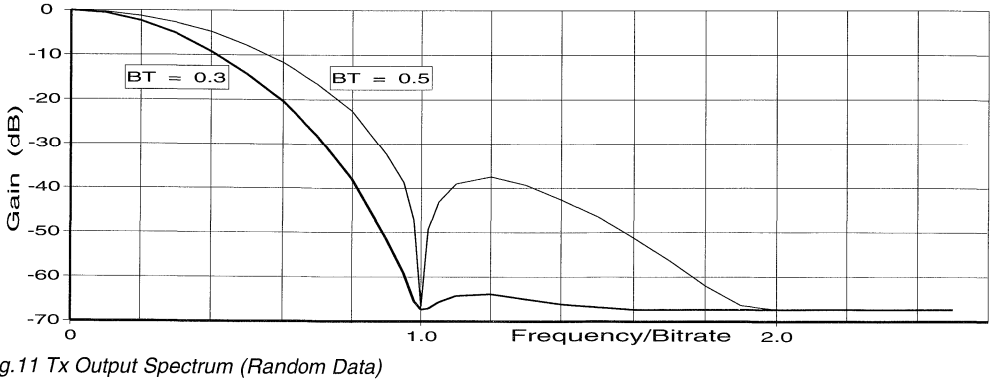


Fig.11 Tx Output Spectrum (Random Data)

Application Information .....

Radio Channel Requirements

To achieve legal adjacent channel performance at high bit-rates, a radio with an accurate carrier frequency and an accurate modulation index will be required.

To achieve optimum channel utilization, (eg. low BER and high data-rates) attention must be paid to the phase and frequency response of both the IF and baseband circuitry.

Bitrate, BT and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on:

- Channel spacing
- Allowable adjacent channel interference
- Tx filter bandwidth (BT)
- Peak carrier deviation (Modulation Index)
- Tx and Rx carrier frequency accuracies
- Modulator and Demodulator linearity
- Rx IF filter frequency and phase characteristics
- Use of error correction techniques
- Acceptable error-rate

As a guide, a raw data-rate of 8,000b/s at 12.5kHz channel spacing may be achievable -depending on local regulatory requirements- using a BT of 0.3 +/- 2kHz maximum deviation and no more than 1.5kHz discrepancy between Tx and Rx carrier frequencies. Forward Error Correction (FEC) could then be used with interleaving to reduce the effect of burst errors.

Reducing the data-rate to 4,800b/s would allow the BT to be increased to 0.5, improving the error-rate performance.

FM Modulator, Demodulator and IF

For optimum performance, the 'eye' pattern of the received signal (when receiving random data) applied to the FX589 should be as close as possible to the Transmit 'eye' pattern examples shown in Figure 10.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening.

To achieve this, attention must be paid to -

- Linearity and frequency/phase response of the Tx frequency modulator. Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few Hertz, two-point modulation being necessary for synthesised radios.
- Bandwidth and phase response of the Rx IF filters.
- Accuracy of the Tx and Rx carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the Rx demodulator should be dc coupled to the FX589 'Rx Signal In' pin (with a dc bias added to centre the signal at the Rx Feedback pin around $V_{DD}/2$ [V_{BIAS}]), however ac coupling can be used provided that:

- The 3dB cut-off frequency is 20Hz or below (i.e. a 0.1uF capacitor in series with 100kΩ).
- The data does not contain long sequences of consecutive ones or zeroes.
- Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of an RF carrier) for the voltage into the FX589 to settle before the 'RxDCacq' line is strobed.

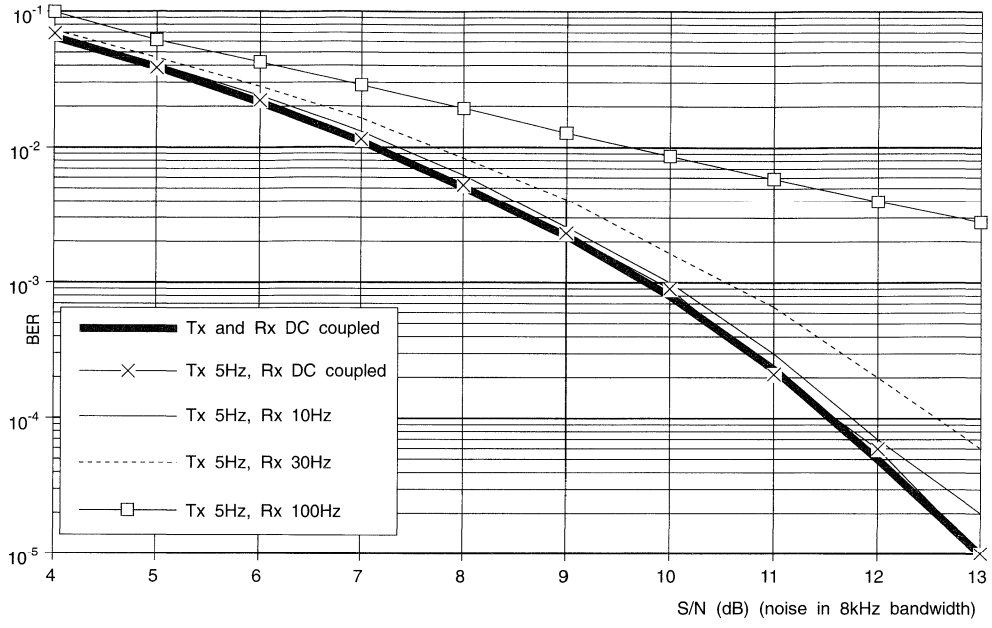


Fig.12 Effect of AC Coupling on Typical Bit-Error Rate

AC Coupling of Rx and Tx Signals

In practical applications, it will usually be possible to arrange for any ac coupling between the FX589 Tx Output and the frequency modulator to cut-off at a very low frequency such as 5.0Hz, but ac coupling between the receive discriminator and the input of the FX589 may need to have a shorter time-constant to avoid problems from voltage steps at the output of the discriminator when changing channels or when the distant transmitter turns on.
For these reasons, as well as to maintain reasonable BER, the optimum -3dB cut-off frequencies are around 5.0Hz in the Tx path and 20.0Hz in the Rx path.

The chart in Figure 12 (above) shows the typical static Bit-Error-Rate performance of the FX589 operating under nominal conditions for various degrees of ac coupling at the Rx Input and the Tx Output:

Data Rate	=	8kb/s
V_{DD}	=	5.0V
Tamb	=	25°C
Tx BT	=	0.3

Two Point Modulation

In a radio employing a frequency synthesiser, to prevent the radio's PLL circuitry counteracting the modulation process, and to provide a clean flat modulation response down to dc, it is recommended that a two-point modulation technique is employed when using the FX589.

Figure 13 shows a suggested basic configuration to provide a two-point modulation drive from the FX589 Tx Output using the FX019 (a CML product) Digitally Controlled 'Quad' Amplifier Array.
The FX019 elements will provide individual setting-up, calibration and dynamic control of modulation levels. Level setting control of the amplifiers/attenuators of the FX019 is via an 8-bit data word.

With reference to Figure 13:

The buffer amplifier is required to prevent loading of the FX589 external RC circuit.

Stage B, with R_1/R_2, provides suitable signal and dc levels for the VCO varactor; C_1 is RF decoupling. The drive level should be adjusted (digitally) to provide the desired deviation.

Stage C, with R_3/R_4, provides the Reference Oscillator drive (application dependant). This parameter is set by adjusting for minimum ac signal on the PLL control voltage with a low-frequency modulating signal (inside the PLL bandwidth) applied.

Stage D, with its attendant components, could be employed if a negative reference drive is required.

Stage A provides buffering and overall level control.

Application Information .....

Two Point Modulation .....

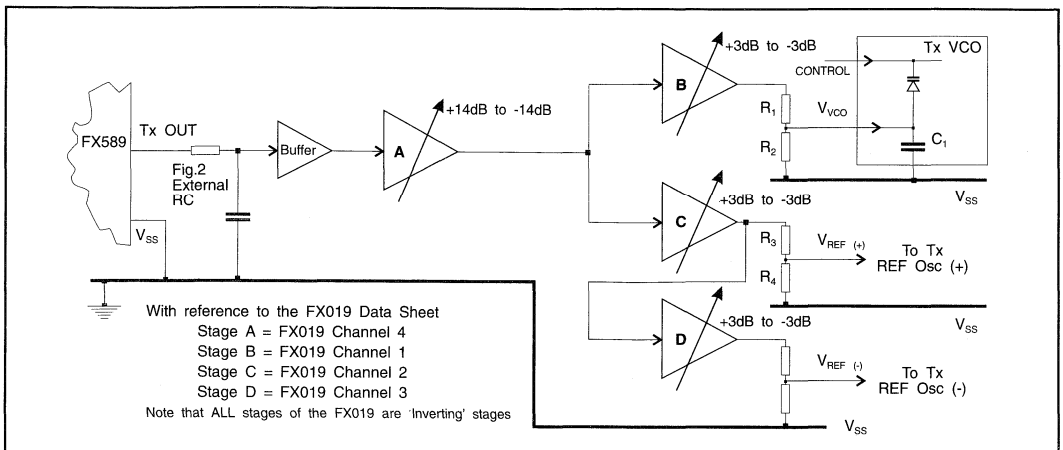


Fig.13 An Example of Two-Point Modulation Drive with Individual Adjustment Using the FX019

Data Formats

The receive section of the FX589 works best with data which has a reasonably 'random' structure --the data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences of consecutive 'ones' or 'zeroes'. Also, long sequences (>100 bits) of '10101010 ...' patterns should be avoided.

For this reason, it is recommended that data is scrambled in some manner before transmission, for example by 'exclusive-ORing' it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble should be at least 16 bits long, and should preferably consist of alternating pairs of '1's and '0's i.e. '110011001100 .....'; the pattern '10101010 ....' should not be used.

'Acquisition' and 'Hold' Modes

The 'RxDCacq' and 'PLLacq' inputs must be pulsed 'High' for about 16 bits at the start of reception to ensure that the dc measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, then the above inputs should be taken 'Low' again.

In most applications, there will be a dc step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on.

The FX589 can tolerate dc offsets in the received signal of at least +/- 0.5V with respect to V_{BIAS}, (measured at the Rx Feedback pin) however to ensure that the dc offset compensation circuit operates correctly and with minimum delay, the 'Low' to 'High' transition of the 'RxDCacq' and 'PLLacq' inputs should occur after the mean input voltage to the FX589 has settled to within about 0.1V of its final value. (Note that this can place restrictions on the value of any series signal coupling capacitor.)

As well as using the 'Rx Hold' input to freeze the Level Measuring and Clock Extraction circuits during a signal 'fade', it may also be used in systems which employ a continuously transmitting control channel to freeze the receive circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronisation.
To achieve this, the FX589 'Xtal' clock needs to be accurate enough that the derived 'RxClock' output does not drift by more that about 0.1 bit time from the actual received data-rate during the time that the 'RxHold' input is 'Low'.

The 'RxDCacq' input, however, may need to be pulsed 'High' to re-establish the level measurements if the 'RxHold' input is 'Low' for more that a few hundred bit-times.

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude.
Note however, that these pins are driven from very high-impedance circuits, so that the dc load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX589DW/P**	-40°C to +85°C
Storage temperature range:	**FX589DW/P**	-40°C to +85°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Remarks	Min.	Max.	Unit
Supply Voltage (V_{DD})		3.0	5.5	V
Operating Temperature		-40.0	+85.0	°C
Rx and Tx Data Rate	(V_{DD} ⊕ 3.0V)	4,000	20,000	bits/sec
	(V_{DD} ⊕ 4.5V)	4,000	40,000	bits/sec
Xtal/Clock Frequency	(V_{DD} ⊕ 3.0V)	1.0	5.0	MHz
	(V_{DD} ⊕ 4.5V)	1.0	6.5	MHz
"High" Pulse Width	Note 10	60.0		ns
"Low" Pulse Width	Note 10	60.0		ns

Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C. Xtal/Clock Frequency = 4.096MHz. Data Rate = 8,000 bits/sec.
Noise Bandwidth = Bit Rate.

Characteristics	Tx PS	Rx PS	See Note	Min.	Typ.	Max.	Unit
Static Values							
Supply Current ((I_{DD}) V_{DD} = 3.0V)	**Tx PS**	**Rx PS**	1				
	1	1		-	0.5	-	mA
	0	1		-	1.0	-	mA
	1	0		-	1.0	-	mA
	0	0		-	1.5	-	mA
((I_{DD}) V_{DD} = 5.0V)	1	1		-	1.0	-	mA
	0	1		-	2.0	-	mA
	1	0		-	3.0	-	mA
	0	0		-	4.0	-	mA
Input Logic Levels							
Logic "1"				3.5	-	-	V
Logic "0"				-	-	1.5	V
Logic Input Current			2	-5.0	-	5.0	µA
Logic "1" Output Level at IOH = -120µA				4.6	-	-	V
Logic "0" Output Level at IOL = 120µA				-	-	0.4	V
Transmit Parameters							
Tx OUT, Output Impedance			3	-	1.0	-	kΩ
Tx OUT, Level			4, 11	0.8	1.0	1.2	V p-p
Tx Data Delay (BT = 0.3)			5	-	2.0	2.5	bit-periods
(BT = 0.5)			5	-	1.5	2.0	bit-periods
Tx PS to Output-Stable Time			6	-	4.0	-	bit-periods

Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
Receive Parameters					
Rx Amplifier -					
Input Impedance		1.0	-	-	MΩ
Output Impedance	7	-	10.0	-	kΩ
Voltage Gain		-	50.0	-	dB
Rx Filter Signal Input Level	8, 11	0.7	1.0	1.3	V p-p
Rx Time Delay	9	-	-	3.0	bit-periods
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}	12	-	50.0	-	kΩ
Voltage Gain	12	-	25.0	-	dB

Notes

1. Not including current drawn from the FX589 pins by external circuitry. See Absolute Maximum Ratings.
2. For V_{IN} in the range V_{SS} to V_{DD}.
3. For a load of 10kΩ or greater. Tx PS input at logic "0"; Tx Enable = "1".
4. Data pattern of "1111000011110000 .."
5. Measured between the rising edge of 'Tx Clock' and the centre of the corresponding bit at 'Tx Out.'
6. Time between the falling edge of 'Tx PS' and the 'Tx Out' voltage stabilising to normal output levels.
7. For a load of 10kΩ or greater. Rx PS input at logic "0".
8. For optimum performance, measured at the 'Rx Feedback' pin for a "1111000011110000 ..." pattern.
9. Measured between the centre of bit at 'Rx Signal In' and corresponding rising edge of the 'Rx Clock'.
10. Timing for an external clock input to the Xtal/Clock pin.
11. 'Typical' level shown is at V_{DD} = 5.0V; actual levels are proportional to applied V_{DD}.
12. Small signal measurement at 1.0kHz with no load on $\overline{Xtal}$ output.

Package Outlines

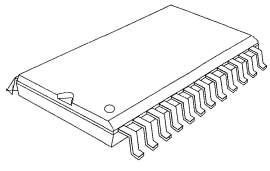
The FX589 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX589 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX589DW 24-pin plastic S.O.I.C. (D2)

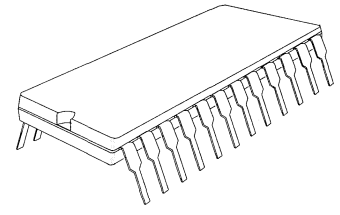
NOT TO SCALE



Max. Body Length 15.70mm
Max. Body Width 7.65mm

FX589P 24-pin plastic DIL (P4)

NOT TO SCALE



Max. Body Length 31.85mm
Max. Body Width 13.82mm

Ordering Information

FX589DW 24-pin plastic S.O.I.C. (D2)

FX589P 24-pin plastic DIL (P4)

CML Semiconductor Products
PRODUCT INFORMATION

FX909 GMSK "Packet Data" Modem

Publication D/909/1 July 1994
Advance Information

Features

- **Automatic Protocol Handling**
  [Bit and Frame Sync, Block Formatting, CRC and FEC, Interleaving and Scrambling]
- **Half-Duplex Operation at 4,000 to 19,200b/s**
- **GMSK Tx Signal Filtering (BT = 0.3)**
- **Low-Power; 3mA [TYP] Operating**
- **'Mobitex' and General-Purpose Packet Data Applications**
- **8-Bit Parallel µController Interface**
- **Bandwidth Efficient**
- **Reduces Host Processing Load**
- **Simple Software Implementation**

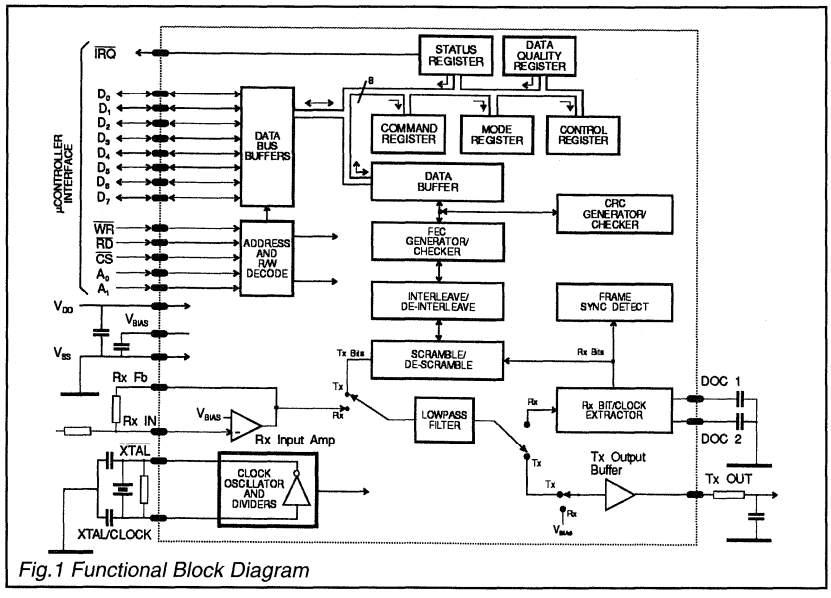


Fig.1 Functional Block Diagram

FX909

Brief Description

The FX909 is a single-chip half-duplex GMSK modem which offers many benefits to the manufacturer and programmer of medium to high-speed radio packet-data links using 'Mobitex' or general-purpose packet protocol.

❍ **Automatic handling (Tx/Rx) of Frame structure and Data Blocks .....** will reduce the processing load on the host µController. Requiring service by the µController only once per Tx or Rx Data Block, the FX909 will perform as much as possible of the computationally intensive work involved in the handling of 'Mobitex' protocol, including CRC and FEC operations, Frame Sync detection, Interleaving and Scrambling.

❍ **Gaussian Minimum Shift Keying (GMSK) modulation .....** provides the basis for an extremely good relationship between the RF bandwidth, Data bit-rate and Bit-error-rate.

❍ **Low-power, high-speed operation .....** selectable 4,000b/s to 19,200b/s with a typical operating requirement of only 3mA at 5 volts.

❍ **Signal acquisition and tracking .....** allows for the rapid acquisition of received messages, followed by automatic tracking of signal variations.
Both PLL bandwidth and Rx signal level measurement circuitry will react automatically as programmed.

Rx and Tx data and control between the host µController and the FX909 is via an 8-bit bi-directional parallel interface; input and output signals to and from the radio system are in analogue form suitable for connection to the radio's discriminator and frequency modulator.

The FX909 is available in both 24-pin DIL and Surface-Mount packages.

Introduction

Table of Contents

FX909 Circuit Descriptions (See Figure 2)

Data Bus Buffers

Eight bi-directional 3-state logic-level buffers between the modem's internal registers and the controlling µController's data-bus lines.

$\overline{RD}$, $\overline{WR}$ $\overline{CS}$ and Address Inputs A_0 and A_1

Control the transfer of data bytes between the µController and the modem's internal registers, according to the state of the Write and Read enable ($\overline{WR}$ and $\overline{RD}$) inputs, the Chip Select ($\overline{CS}$) input and the Register Address inputs (A_0 and A_1).

The Data Bus Buffers and Address & R/W Decode blocks provide a byte-wide parallel µController interface.

Status and Data Quality Registers

8-bit registers which the µController can read to determine the status of the modem and the received data quality.

Command, Mode and Control Registers

The values written by the µController to these 8-bit registers control the operation of the modem.

Data Buffer

An 18-byte buffer used to hold Rx or Tx data to or from the µController.

CRC Generator/Checker

A circuit which generates (transmit mode) or checks (receive mode) the Cyclic Redundancy Checksum bits which are included in transmitted Data Blocks so that the receive modem can detect transmission errors.

FEC Generator/Checker

In transmit mode this circuit calculates and adds the Forward Error Correction information (4 bits) to each byte presented to it. In receive mode the FEC information is used to correct most transmission errors that may have occurred in a Data Block or in Frame Head control bytes.

Tx Output Buffer

A unity-gain amplifier used in the transmit mode to buffer the output of the Tx Lowpass Filter. In receive mode, the input of this buffer is connected to V_{BIAS}. When changing from Rx to Tx mode the input to this buffer will be connected to V_{BIAS} for 2 bit periods to prevent unwanted signals, from the lowpass filter, appearing at the Tx OUT pin.

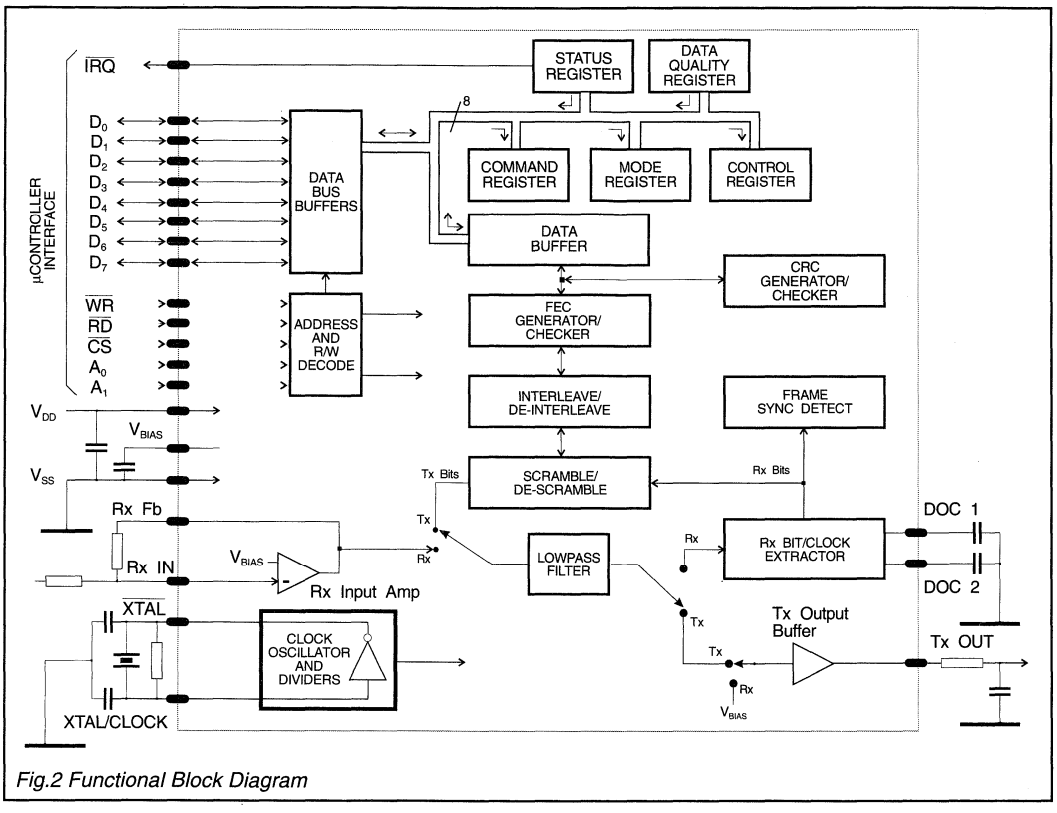


Fig.2 Functional Block Diagram

Rx Input Amp

Allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components.

Interleave/De-Interleave Buffer

Interleaves data bits within a data block before transmission and de-interleaves the received data block so that the FEC system is best able to handle short noise bursts or fades.

Frame Sync Detect

This circuit, which is only active in the receive mode, is used to look for the user-specified 16-bit Frame Synchronisation pattern which is transmitted to mark the start of every frame.

Scramble/De-Scramble

This block may be used to scramble/descramble the transmitted and received Data Block by modulating it with a 511-bit pseudo-random sequence. Scrambling smooths the transmitted spectrum especially when repetitive sequences are to be transmitted.

Rx Bit/Clock Extraction

These circuits, which operate only in receive mode, extract a bit-rate clock from the received signal, and measure the received signal amplitude and its dc offset.

This information is then used to extract the received bits and also to provide an input to the received Data Quality measuring circuit.

Clock Oscillator and Dividers

This circuit derives the transmit bit rate (and the nominal receive bit rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or fed from an external source.

(Tx/Rx) Lowpass Filter

This filter, which is used in both transmit and receive modes, is a low-pass transitional gaussian filter.

In Tx mode the filter bandwidth is set for a loss of 3dB at 0.3 times the selected bit rate (BT = 0.3) and the bits are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In Rx mode this filter is used with an increased BT factor (0.56) to reject HF noise so that the signal is in a suitable condition for extracting the received data.

Pin Functions

FX909 (J4 and L2)	
1	**$\overline{IRQ}$:** A 'wire-ORable' output for connection to the controlling µController's Interrupt Request input. This output has a low-impedance pull-down to V_{SS} when active, and is high-impedance when inactive.
2	**D_7:**
3	**D_6:**
4	**D_5:**
5	**D_4:** 8 bi-directional 3-state µController interface data lines.
6	**D_3:**
7	**D_2:**
8	**D_1:**
9	**D_0:**
10	**$\overline{RD}$:** An active-low logic level input used to control the reading of data from the modem into the controlling µController.
11	**$\overline{WR}$:** An active-low logic level input used to control the writing of data into the modem from the controlling µController.
12	**V_{SS}:** The negative supply rail (ground).
13	**$\overline{CS}$:** An active-low logic level input to the modem used to enable a data Read or Write operation (see Figure 25, Timing).
14	**A_0:** Two logic-level modem register selection inputs.
15	**A_1:**
16	**$\overline{Xtal}$:** The output of the on-chip Xtal oscillator.
17	**Xtal/Clock:** The input to the on-chip Xtal oscillator. Note that attempts at operation of the FX909 without a suitable Xtal or clock input will increase required I_{DD} and place the µController interface into an undefined state.
18	**Doc 2:** Connections to the internal Rx signal level measurement circuitry. Capacitors as described in Figure 3 should be fitted between each of these pins and V_{SS}.
19	**Doc 1:**
20	**Tx Out:** The Tx signal output from the modem.
21	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to V_{SS} by a capacitor mounted close to the device pins.
22	**Rx In:** The input to the Rx input amplifier.
23	**Rx Fb (Rx Feedback):** The output of the Rx input amplifier, and the input to the (Rx) Lowpass Filter.
24	**V_{DD}:** The positive supply. Levels and voltages within the modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the device pins.

Application Information

External Components

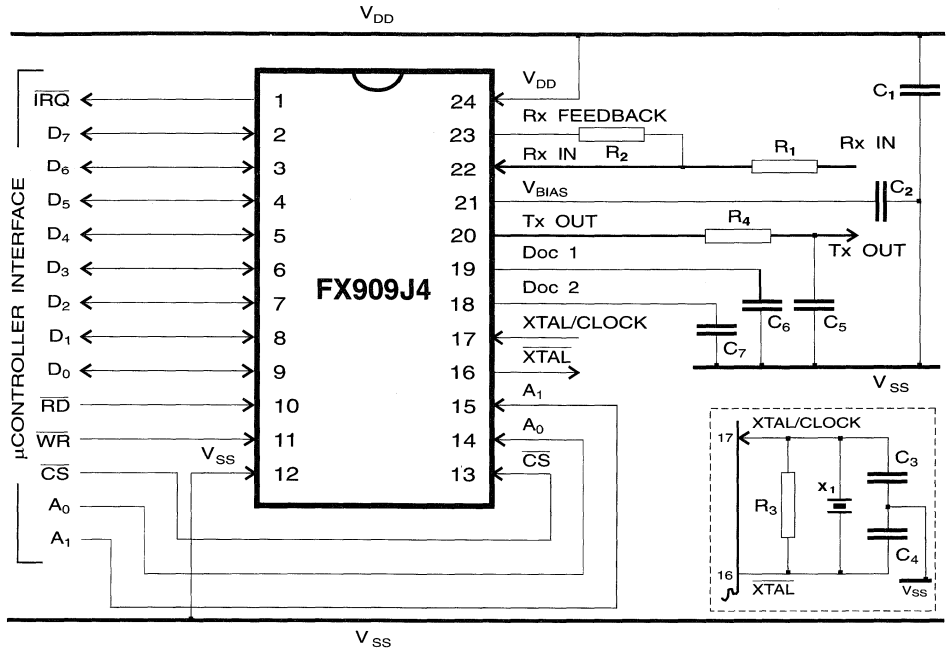


Fig.3 Recommended External Components

Component	Value	Tolerance
R_1	Note 1	±10%
R_2	100kΩ	±10%
R_3	1.0MΩ	±20%
R_4	Note 2	±5%
C_1	0.1µF	±20%
C_2	0.1µF	±20%
C_3	Note 3	±20%
C_4	Note 3	±20%
C_5	Note 2	±10%
C_6	Note 4	±20%
C_7	Note 4	±20%
X_1	Note 5	

Installation Notes

1. Resistors R_1 and R_2, with the Rx Input Amplifier, set the signal input level to the modem.
   The value of R_1 should be calculated to give 1.0v p-p at the Rx Feedback pin for a received 11110000... sequence. The dc level of the received signal should be adjusted so that the signal at the modem's Rx Feedback pin is centred around V_{BIAS}.

2. External components R_4 and C_5 form an RC lowpass filter between the Tx Buffer output (Tx OUT) and the input to the radio's frequency modulator; this is an important part of the Tx signal filtering. These components may form a part of any dc level shifting and gain adjustment circuitry.
   The ground connection (V_{SS}) of C_5 should be positioned to give maximum attenuation of high frequency noise into the modulator.
   R_4 and C_5 should be chosen so that the product of R_4 (Ohms) and C_5 (Farads) is:

$$\frac{0.34}{\text{bit rate}} \text{ bits per sec}$$

   R_4 should be not less than 47kΩ and the value used for C_5 should take into account parasitic capacitance.

Examples	R_4	C_5
8000b/s	100kΩ	430pF
4800b/s	100kΩ	710pF

The 'eye' diagram of the transmitted signal (after the external R_4/C_5 network) is shown in Figure 5.

Continued on next page .....

Application Information .....

Installation Notes .....

3. The values used for C_3 and C_4 should be suitable for the frequency of X_1.
   As a guide:
   $C_3 = C_4 = 33pF$ for $X_1 < 5.0MHz$.
   $C_3 = C_4 = 18pF$ for $X_1 > 5.0MHz$.

4. External capacitors C_6 and C_7 form part of the received signal level measuring circuit; the values of C_6 and C_7 should satisfy the following:
   C (F) x Data Rate (bps) = 120×10^{-6}.

D/Rate(kb/s)	C_6/C_7(nF)	D/Rate(kb/s)	C_6/C_7(nF)
4	30.0	4.8	22.0
8.0	15	9.6	12.0
16.0	6.8	19.2	6.8

5. If the on-chip Xtal oscillator is to be used, then the external components X_1, C_3, C_4, and R_3 are required as shown in Figure 3 (inset).
   If an external clock source is to be used these components are not required; the input should be connected to the Xtal/clock pin and the Xtal pin left unconnected.
   Table 4 (Clock/Data Rates) provides advice on the selection of the correct Xtal value.

External Signal Paths

The diagram below shows signal connections to and from the FX909. Inputs and outputs are shown with dc coupling and level-shifting components; the notes and diagrams on the following page (Figures 6 and 7) describe how, if acceptable, ac coupling may be employed.

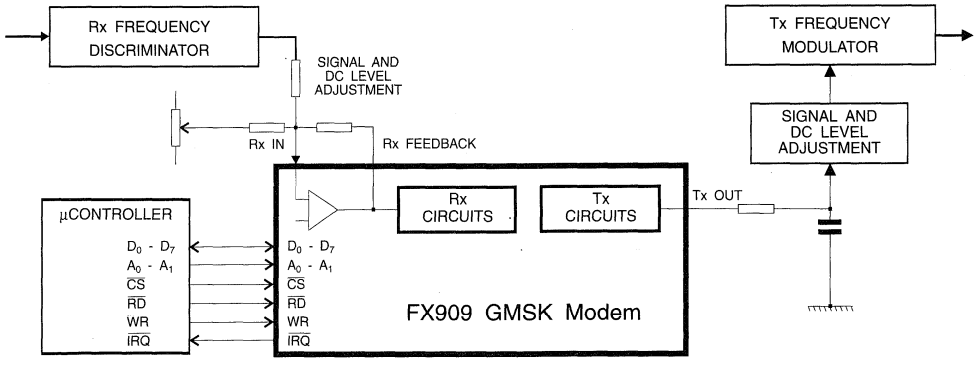


Fig.4 External Signal Paths

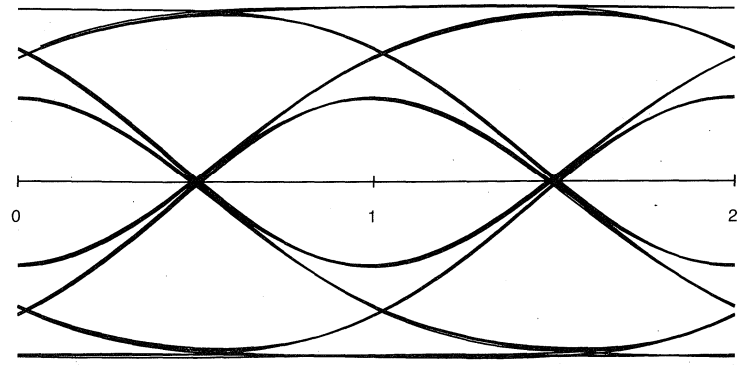


Fig.5 Example Transmit EYE Diagram (after the external RC network)

AC Coupling

For a practical application, ac coupling from the modem's transmit output to the Frequency Modulator and from the receiver's Frequency Discriminator to the receive input of the modem may be desired. There are, however, two problems.

Firstly, ac coupling of the signal degrades the bit-error-rate performance of the modem.
Figure 6 illustrates the typical bit error rates at 8kb/s (without FEC) for differing degrees of ac coupling;

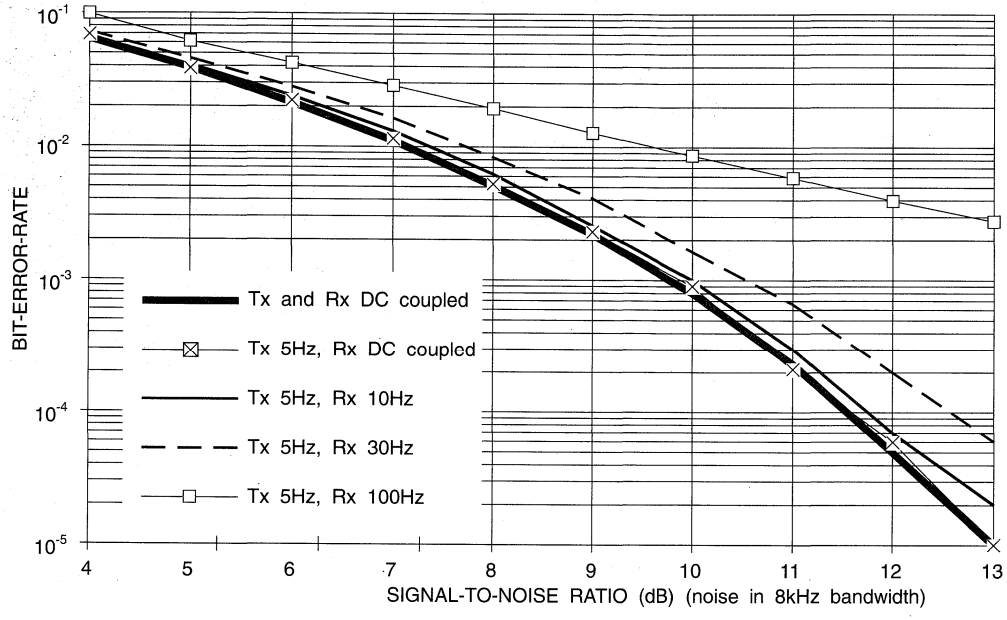


Fig.6 Examples of BER Performance Degradation Due to Varying Degrees of AC Coupling

Secondly, any ac coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits.
As illustrated below, the time for this voltage step to decay to 37% of its original value is:

$$T = \frac{1}{(2\pi \times f)}$$

Where f is the 3dB cut-off frequency of the ac coupling network and is 8 msec (or 64 bit-times at 8000 bits-sec) for a 20Hz network.

For these reasons the maximum -3dB cut-off frequencies would seem to be around 5Hz in the Tx path and 20Hz in receive at 8kb/s.

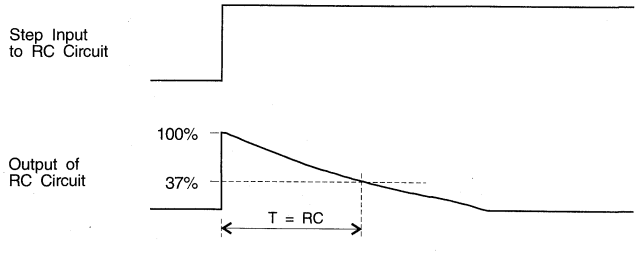


Fig.7 Decay Problems of the AC Coupling Network

Application Information .....

Radio Performance

The maximum data rate that can be transmitted over a radio channel using this modem depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Bit rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracies.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 8000 bits/sec can be achieved - subject to local regulatory requirements - over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ± 2kHz peak for a repetitive ' 1100... ' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 1500Hz.

The modulation scheme employed by this modem is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. This does, however, place constraints on the performance of the radio.

In particular, attention must be paid to:

- Linearity, frequency and phase response of the Tx Frequency Modulator.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a dc offset at the discriminator output.

Viewing the received signal eye (at the FX909 Rx Feedback pin) gives a good indication of the overall transmitter/ receiver performance.

Modem to µController Interface

The Data Bus Buffers and Address and Read/Write Decode blocks form a byte-wide parallel µController interface. The diagram below shows how this function can be memory mapped.

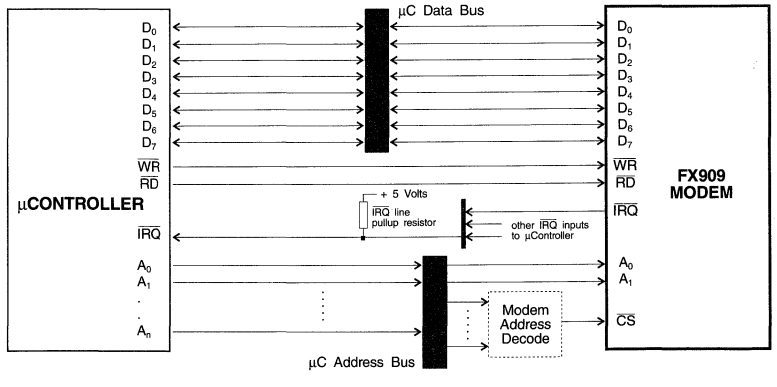


Fig.8 Typical Modem to µController Interface

Application Information .....

Baseband and RF Frequency Requirements

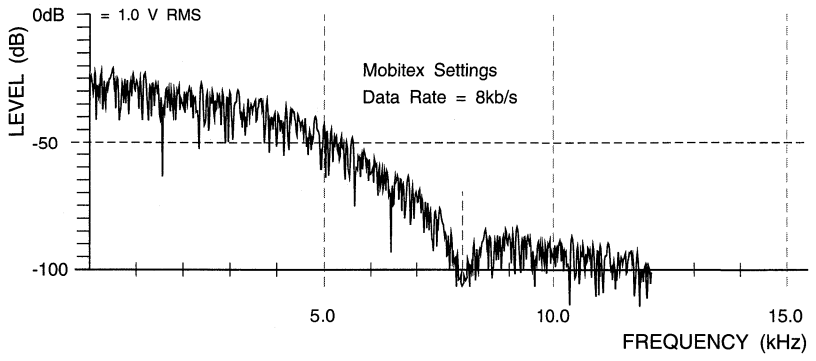


Fig.9 Typical Output Frequency Spectrum for a Random Data Sequence (Tx Out, measured after R_4, C_5 combination)

RF Channel Occupancy

The diagram below shows the theoretical RF bandwidth requirements when interfacing the FX909 baseband (Tx OUT) signal (Figure 9, above) to a radio transmitter. This plot assumes a perfect frequency modulator.

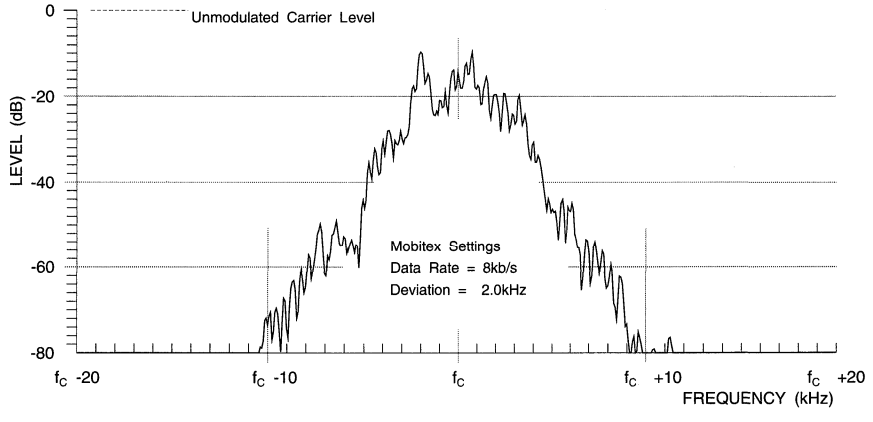


Fig.10 Theoretical Tx RF Frequency Spectrum Resulting from a Random Data Sequence from the FX909

Note that particular repetitive data sequences, such as '1010 ....' will produce spectra which are markedly different to those shown in Figures 9 and 10.

Programming Information

Data Formats

Mobitex Frame and Data Structures

The Mobitex format for transmitted data is in the form of a Frame Head immediately followed by a number of Data Blocks (0 to 32).

The Frame Head consists of 7 bytes .....

2 bytes of Bit Sync:
1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 – from base, or
0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 – from mobile
(sent L to R).

2 bytes of Frame Sync:
System specific.

2 bytes of Control Data:
– System specific ID and control information.

1 byte of FEC Code (generated by the FX909):
– 4 bits for each of the control bytes:
– bits 7 - 4 operate on the first control byte.
– bits 3 - 0 operate on the second control byte.

Each byte in the Frame Head is transmitted bit 7 (MSB) first, bit 0 (LSB) last.

The Data Block consists of .....

18 bytes of Data:
2 bytes of CRC are calculated by the FX909 from the 18 Data Bytes.
4 bits of FEC code are calculated for each of the Data and CRC bytes

The resulting 240 bits are interleaved and scrambled before transmission; see Figure 23, (Interleaving).

Figure 11 shows how the over-air signal is built up from Frame Sync and Bit Sync patterns, Control Bytes and Data Blocks.

The binary data transferred between the modem and the controlling µController is that shown enclosed in the heavily outlined rectangles.

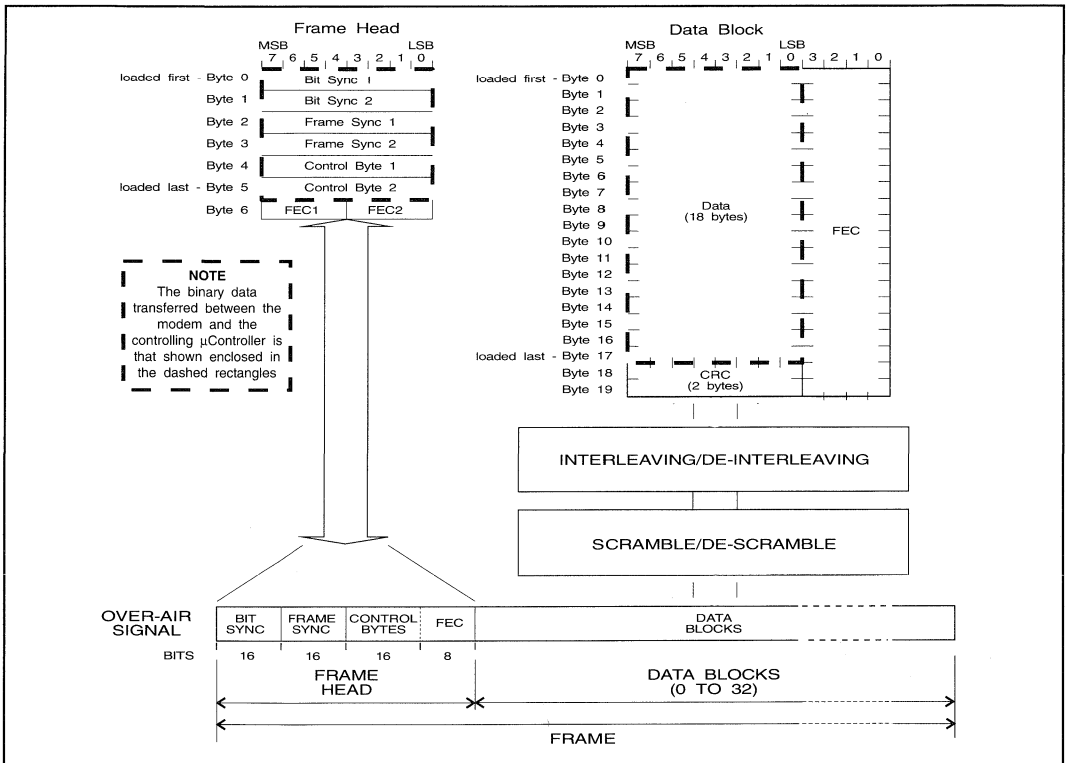


Fig.11 FX909 Mobitex System Data Format

General Purpose Formats

In a proprietary system the user may employ the data elements provided by this device to construct a custom, over-air data structure.

For example, 16 bits of bit sync + 2 bytes of frame sync + 4 bytes of receiver and sender address + n data blocks would be sent as: **TQB (bit and frame sync) + TQB (addresses) + (n x) TDB.**
And received as: **SFS + RSB + RSB + RSB + RSB + (n x) RDB.**

Note that it is important to have established frame synchronization before receiving data to enable the receiving device to decode synchronously. Also the user may add, by way of algorithms performed on the controlling device, additional data correction with the bytes in the data block task

Programming Information .....

Modem/μController Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Head' optionally followed by one or more formatted Data Blocks.

The Frame Head includes a Frame Synchronisation pattern designed to allow the receiving modem to identify the start of a frame.

The following data blocks are constructed from the 'raw' data using a combination of CRC (cyclic redundancy checksum) generation, Forward Error Correction (FEC) coding, Interleaving and Scrambling.

To reduce the processing load on the host μController, the FX909 has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting and de-formatting and, when in receive mode, in searching for and synchronising onto the Frame Sync or Frame Head.

In normal operation the modem will only require servicing by the μController once per received or transmitted data block. Thus, to transmit a block, the controlling μController has only to load the unformatted (raw) binary data into the modem's data buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result with FEC coding, interleave then scramble the bits before transmission.

In receive mode, the FX909 modem can be instructed to assemble a block's worth of received bits, de-scramble and de-interleave the bits, check and correct (using the FEC coding) and check the resulting CRC before placing the received binary data into the Data Buffer for the μController to read. The FX909 modem can also handle the transmission and reception of un-formatted data; to allow for example, the transmission of special Bit and Frame Synchronisation sequences or test patterns.

The Programmer's View

Register Selection

The FX909 modem appears to the programmer as 4 write-only 8-bit registers shadowed by 3 read-only registers.

Individual registers are selected by the A_1 and A_0 inputs; see Read and Write cycle timing diagrams (Figure 25).

Table 1 Register Selection

A_1	A_0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	DQ Register
1	1	Mode Register	not used

Data Buffer

An 18-byte read/write buffer which is used to transfer data (as opposed to Command, Status, Mode, Data-Quality and Control information) between the modem and the controlling μController.

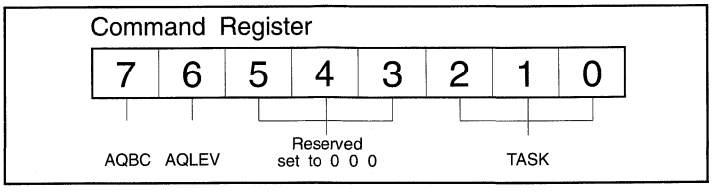
The Data Buffer appears to the μController as a single 8-bit register; the modem ensures that sequential μController 'read' or 'write' actions to the buffer are routed to the correct locations within this buffer.

The μController should only access this buffer when the Status Register BFREE (Buffer Free) bit is at a logic '1'. The buffer should only be written to while in the Tx mode and read from in the Rx mode (except when loading Frame Sync detection bytes in the Rx mode). Data Read/Write Timing information is provided in this document (Figure 25).

Command Register

Writing to this register instructs the modem to perform a specific action or actions, depending upon the setting of the TASK, AQLEV, and AQBC bits (see Figure 12 and Table 2).

Fig.12 The Command Register



When it has no action to perform, the modem will be in an idle state, and if it is in the Tx mode the input to the Tx (Lowpass) Filter will be connected to V_{BIAS}.

When it has no action to perform in the Rx mode the modem will continue to measure the received data quality and extract bits from the received signal, feeding them into the De-Interleave Buffer, but will otherwise ignore the received data.

Command Register

B7 **AQBC**	**Acquire Bit Clock:** This bit has no effect in the Tx mode. In the Rx mode, whenever a byte with the AQBC bit set to logic '1' is written to the Command Register, it initiates an automatic sequence designed to achieve bit-timing synchronisation with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit-timing extraction circuits to their widest bandwidth, then gradually reducing the bandwidth as timing synchronisation is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register. Setting this bit to logic '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQBC bit set to logic '1'. The AQBC bit will normally be set at the same time as an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task, however it may also be used independently to re-establish clock synchronisation quickly after a long fade. Alternatively, an SFS or SFH task may be written to the Command Register with the AQBC bit at logic '0' if it is known that clock synchronisation does not need to be re-established. More details of the Bit Clock Extraction Sequence are given in the Operational Information section of this Data Sheet
B6 **AQLEV**	**Acquire Receive Signal Levels:** This bit has no effect in the Tx mode. In receive mode, whenever a byte with the AQLEV bit set to a logic '1' is written to the Command Register, it initiates an automatic sequence designed to measure the amplitude and dc offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time -hence improving the measurement accuracy- until the 'normal' value set by the LEVRES bits of the Control Register is reached. See Figure 24. Setting this bit to a logic '0' (or changing it from '1' to '0') has no effect; note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQLEV bit set to a logic '1'. The AQLEV bit will normally be set at the same time as an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, a SFS or SFH task may be written to the Command Register with the AQLEV bit at logic '0' if it is known that there is no need to re-establish the received signal levels. Refer to the Clock Extraction (Operational Information section) notes.
B5 **B4** **B3**	These bits should each be set to a logic '0'.
B2 **B1** **B0** **TASK**	**Task:** Operations such as transmitting a data block are treated by the modem as 'tasks'. Information on Task functions is given on the following pages. A task is initiated when the µController writes a byte to the Command Register with the Task bits set to anything other than the 'NULL' ('0' '0' '0') code. The µController should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer if the BFREE (Buffer Free) bit of the Status Register is a logic '0'. Different tasks apply in receive and transmit modes. **Tx Mode:** All tasks other than NULL, RESET and TSO instruct the modem to transmit data from the Data Buffer, formatting it as required. For these tasks the µController should wait until the BFREE (Buffer Free) bit of the Status Register is a logic '1', before writing the data to the Data Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Buffer, byte number '0' of the block should be written first. Once the byte containing the desired task has been written to the Command Register, the modem will: Set the BFREE (Buffer Free) bit of the Status Register to a logic '0', take the data from the Data Buffer as quickly as it can -transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Programming Information .....

Command Register .....

B2 **B1** **B0** **TASK .....**	**Task: .....** Once all data has been transferred from the Data Buffer the modem will set the BFREE and IRQ bits of the Status Register to a logic '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the µController that it may write new data and the next task to the modem. In this way the µController can write a task -and the associated data- to the modem while the modem is still transmitting the data from the previous task. **Rx Mode:** The µController should wait until the BFREE bit of the Status Register is a logic '1', then write the desired task to the Command Register. Once the byte containing the desired task has been written to the Command Register, the modem will: Set the BFREE bit of the Status Register to a logic '0'. Wait until enough received bits are in the De-Interleave Buffer. Decode them as needed, and transfer any resulting data to the Data Buffer. Then the modem will set the BFREE and IRQ bits of the Status Register to logic '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the µController that it may read from the Data Buffer and write the next task to the modem. If more than 1 byte is contained in the Data Buffer, byte number '0' of the data will be read first. In this way the µController can read data and write a new task to the modem while the received bits needed for this new task are being stored in the De-Interleave Buffer. The above is not true for loading the Frame Sync detection bytes (LFSB); the bytes to be compared with the incoming data must be loaded prior to the task bits being written. Detailed timings for the various tasks are given in later sections.

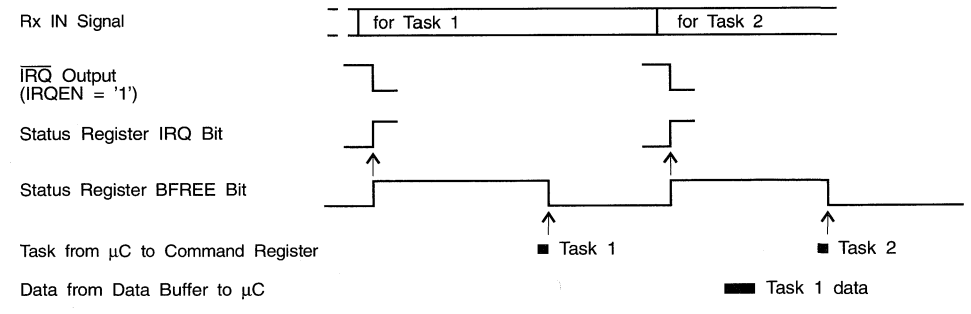


Fig.13 The Receive Process

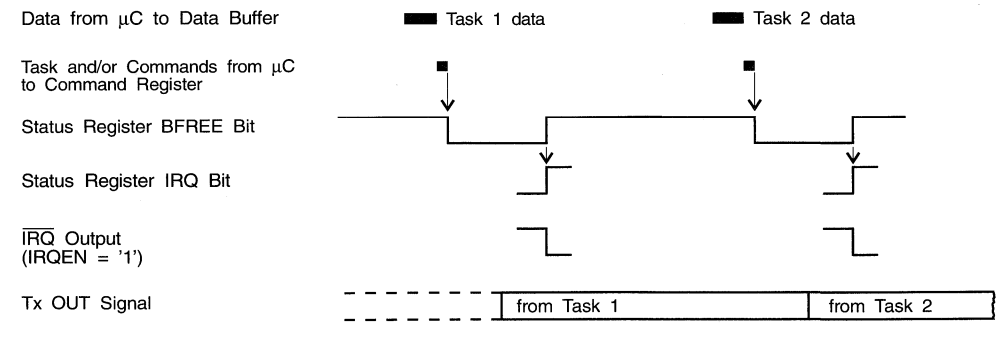


Fig.14 The Transmit Process

Modem Tasks in Detail

The following describes the setting and format of the Command Register 'task' bits (bits 2, 1 and 0). Note that before a task is programmed the Tx/Rx bit in the Mode Register must be set to the required level.

Command Bits 2	1	0	Receive Mode		Transmit Mode	
0	0	0	NULL		NULL	
0	0	1	SFH	Search for Frame Head	T7H	Transmit 7 Byte Frame Head
0	1	0	R3H	Read 3 Byte Frame Head	Reserved	.. ..
0	1	1	RDB	Read Data Block	TDB	Transmit Data Block
1	0	0	SFS	Search for Frame-Sync	TQB	Transmit 4 Bytes
1	0	1	RSB	Read Single Byte	TSB	Transmit Single Byte
1	1	0	LFSB	Load Frame-Sync Bytes	TSO	Transmit Scrambler Output
1	1	1	RESET	Cancel any Current Action	RESET	Cancel any Current Action

Table 2 Modem Task Allocations

Modem Tasks

NULL

No Effect. This task is provided so that an AQBC or AQLEV (Command Register) command can be initiated without loading a new task.

SFH

Search for Frame Head. Causes the modem to search the received signal for a valid Frame Head. The Frame Head will consist of a 16-bit Frame Sync followed by control data which has no uncorrectable errors (see Figure 11 -Data Format).
The search will continue until a valid Frame Head has been found, or until the RESET task is loaded.
The search is carried out by the modem in 3 stages:

1. Attempt to match the incoming bits against the previously programmed (task LFSB) 16-bit Frame Sync pattern (allowing up to any one bit (of 16) in error).
2. When a match has been found, the modem will read the next 3 received bytes as Frame Head bytes; these bytes will be checked using the FEC bits. If the FEC indicates uncorrectable errors the modem will resume the search, looking for a new Frame Sync pattern.
3. If the received bytes are error free or correctable, BFREE and IRQ bits (Status Register) are set to a logic '1' and the CRCFEC bit set to a logic '0'; the two corrected (by the modem) Frame Head Control Data bytes are then placed into the Data Buffer.
   The MOBAN bit (Mobile or Base) in the Status Register will be set according to the polarity of the 3 bits that preceded the Frame Sync pattern.

On detecting that the BFREE bit of the Status Register has gone to a logic '1', the µController should read the 2 Frame Head control data bytes from the Data Buffer and then write the next task to the modem's Command Register.

R3H

Read 3 Byte Frame Head. This task, which would normally follow an SFS task, will cause the modem to place the next 3 bytes directly into the Data Buffer and, concurrently, check those 3 bytes as Frame Head Control Data bytes; the modem will set the CRCFEC bit to a logic '1' (high) if errors are detected. Note: This task will not correct any errors.
The BFREE and IRQ bits of the Status Register will be set to a logic '1' when the task is complete; this is to indicate that the µController may read the data from the Data Buffer and write the next task to the Command Register. The CRCFEC bit in the Status Register will be set according to the validity of the received FEC bits.

RDB

Read Data Block. Causes the modem to read the next 240 bits (see Data Formats -Frame and Data Structures) as a Mobitex data block. This task will de-scramble and de-interleave the received bits, FEC correct and CRC check the resulting 18 data bytes placing them in the Data Buffer. When the task is complete the BFREE and IRQ bits of the Status Register are set to a logic '1' to indicate that the µController may read the data from the Data Buffer and write the next task to the Command Register. The CRCFEC bit in the Status Register will be set according to the outcome of the CRC check. Note that in the receive mode the checksum circuits are initialised (ready for operation) on completion of any task other than NULL.

Programming Information .....

Modem Tasks	
SFS	**Search for Frame Sync.** This task performs the first part only of an SFH task. It causes the modem to search the received signal for a 16-bit sequence which matches the previously programmed Frame Sync pattern (allowing up to any one bit (in 16) in error). When a match is found the modem will set the BFREE and IRQ bits of the Status Register to a logic '1' and update the MOBAN bit. The µController may then write the next task to the Command Register.
RSB	**Read Single Byte.** This task, which is intended for special tests and channel monitoring -perhaps preceded by an SFS task, causes the modem to read the next 8 bits and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Buffer (bit 7 will represent the earliest bit received). The BFREE and IRQ bits of the Status Register will then be set to a logic '1' to indicate that the µController may read the data byte from the Data Buffer and write the next task to the Command Register.
LFSB	**Load Frame Sync Bytes.** This task is unlike other Rx tasks in that the Data Buffer must be loaded (with the 2 Frame Sync bytes) before the task is issued and the task must only be issued 'between' received messages ; i.e. before the first task for receiving a message and after the last data is read out of the Data Buffer. It takes 2 bytes from the Data Buffer and loads them into the FX909's internal Frame Sync pattern store. The MSB of byte 0 represents the first bit of a received Frame Sync pattern and the LSB of byte 1 is compared to the last bit of a received Frame Sync pattern that will be looked for when a SFS or SFH task is executing. The LFSB task itself does not initiate a search for a received Frame Sync pattern. Once the modem has read the Frame Sync bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating that the µController may write the next task to the modem.
T7H	**Transmit 7-Byte Frame Head.** Takes 6 bytes of data from the Data Buffer, calculates and appends 8 bits of FEC from bytes 4 and 5 then transmits the result as a complete Frame Head. Bytes 0 and 1 form the bit -sync pattern, bytes 2 and 3 form the frame-sync pattern and bytes 4 and 5 are the Frame Head control bytes. Bit 7 of byte 0 of the Data Buffer is sent first and bit 0 of the FEC byte last. Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating that the µController may write the next task and its data to the modem.
TQB	**Transmit 4 Bytes.** Takes 4 bytes of data from the Data Buffer and transmits them without adding FEC or interleaving, bit 7 of byte 0 first, bit 0 of byte 3 last. Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating that the µController may write the next task and its data to the modem.
TDB	**Transmit Data Block.** Takes 18 bytes of data from the Data Buffer, calculates and applies a 16-bit CRC and forms the FEC for the 18 data bytes and the CRC; the resulting 240 bits are then interleaved and passed through the scrambler, if enabled, before being transmitted as a Data Block. Note that in transmit mode the CRC checksum circuit is initialised on completion of any task other than NULL. Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating that the µController may write the next task data to the modem.
TSO	**Transmit Scrambler Output.** Intended for channel set-up, this task enables the scrambler and transmits its output (which will be 9-bit pseudo-random). When the modem has started this task the Status Register bits will not be changed and hence an IRQ will not be raised. The µController may write data and the next task to the modem at any time and the scrambler output will stop when the new task has produced its first data. See Mode Register SCREN.
RESET	**Stop any Current Action.** This 'task' takes effect immediately, and terminates any current action (Task, AQBC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to a logic '1', without setting the IRQ bit. RESET should be used when V_{DD} is applied to set the modem into a known state. Note that due to delays in the Tx Lowpass Filter filter, it will take approximately 2 bit-times for any change to become apparent at the Tx Out pin.

Modem Tasks	
TSB	**Transmit Single Byte.** Takes a byte from the Data Buffer and transmits the 8 bits, bit 7 first without adding FEC or interleaving. Once the modem has read the data byte from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

Lowpass Filter Delay

The Task Timing figures detailed in Table 3 are based upon: the signal at the input to the Tx lowpass Filter in the transmit mode, or the signal at the input to the de-interleave circuits in the receive mode. As can be seen from the diagram in Figure 15, there is an additional delay of approximately 2 (two) bit-times in both Tx and Rx modes due to the (Tx/Rx) Lowpass Filter.

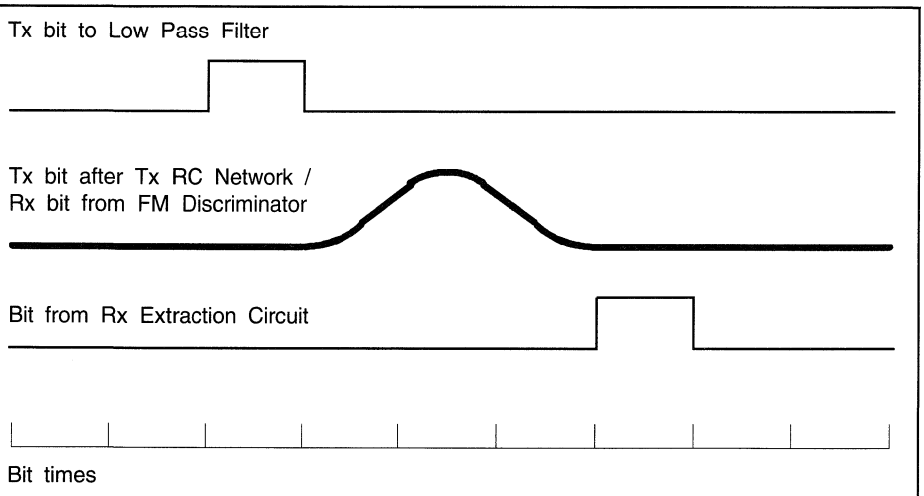


Fig.15 Example of Lowpass Filter Delay Times

Transmit and Receive Task Timing

The diagrams and table on the following page describe Rx and Tx task timing requirements. Note that a new task should not be written to the Command Register for at least 2 bit times after the following operations:
Changing the Rx/Tx bit.
Resetting or after power is applied to the FX909.
This precaution is to ensure that the internal operation of the device is initialised correctly for the new task.
This precaution only applies to the Command Register; other registers may be accessed as normal.

Programming Information .....

Transmit and Receive Task Timing .....

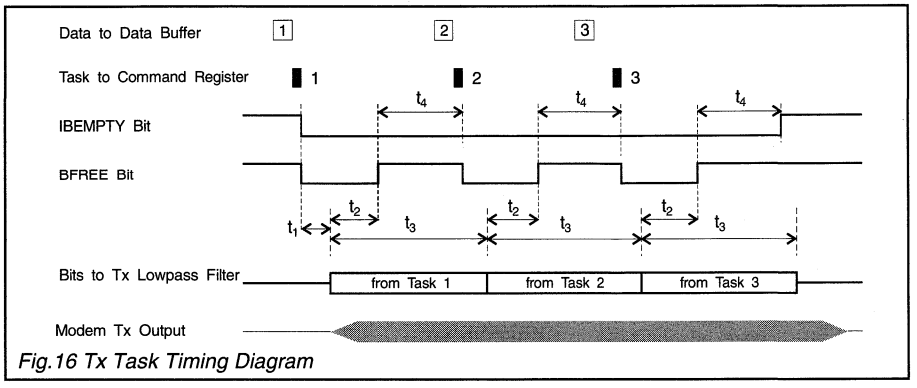


Fig.16 Tx Task Timing Diagram

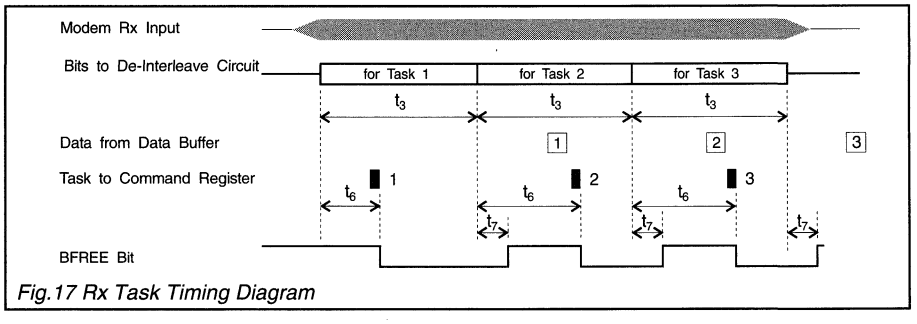


Fig.17 Rx Task Timing Diagram

Timing	Notes	Task	Typical (Bit) Time
t_1	Modem in idle state. Time from writing first task to the application of the first Tx bit to the Tx Lowpass Filter.	Any	1
t_2	Time from the application of the first bit of the task to the Tx Lowpass Filter until BFREE goes to a logic '1' (high).	T7H TQB TDB TSB	36 24 20 1
t_3	Time to transmit all bits of the task. or Time to receive all bits of the task	T7H/SFH TQB R3H TDB/RDB TSB/RSB	56 32 24 240 8
t_4	Maximum time allowed from BFREE going to a logic '1' for the next task (and data) to be written to the modem.	T7H TQB TDB TSB	18 6 218 6
t_6	Maximum time between the first bit of the task entering the de-interleave circuit and the task being written to the modem.	SFH R3H RDB RSB	14 18 218 6
t_7	Time from last bit for task entering the de-interleave circuit to BFREE going to a logic '1'.	Any	1

Table 3 Typical Rx/Tx Task Load Timings

Programming Information .....

Control Register

This 8-bit write-only register controls the modem's bit-rate, response times of the receive clock extraction and signal level measurement circuits and the internal analogue filters.

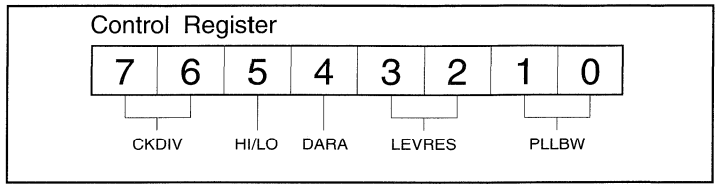


Fig.18 The Control Register

Control Register

Table 4 shows how bit-rates of 4000/8000/16000 or 4800/9600/19200 bits per second may be obtained from common Xtal/clock frequencies.

B7, B6 CKDIV — **Clock Division Ratio:** These bits, together with the HI/LO bit, control a frequency divider driven from the Xtal/clock signal; this ratio and the frequency at the Xtal/Clock pin will determine the transmit and nominal receive bit-rate.

B5 HI/LO — **High or Low Xtal Range Selection:**

		B5		Xtal/Clock Frequency (MHz)					
		'1' High		8.192	9.8304	4.096 (12.288/3)	4.9152	2.048 (6.144/3)	2.4576 (12.288/5)
			'0' Low	4.096 (12.288/3)	4.9152	2.048 (6.144/3)	2.4576 (12.288/5)	1.024	1.2288
B7	**B6**	**Division Ratio: Xtal/Clock Data Rate**		**Data Rate (bits per second)**					
0	0	256	128			16000	19200	8000	9600
0	1	512	256	16000	19200	8000	9600	4000	4800
1	0	1024	512	8000	9600	4000	4800		
1	1	2048	1024	4000	4800				

Table 4 Clock/Data Rates ***Note*** *that device operation is not guaranteed or specified above 19,200 bits/s or below 4,000 bits/s*

B4 DARA — **Data Rate:** Employed in both Rx and Tx, this bit optimises the modem's internal signal filtering circuitry to the relevant bit-rate.
For bit-rates above 10 kb/s this bit (B4) should be set to a logic '1', for bit-rates at or below 10kb/s set to a logic '0'.

B3, B2 LEVRES — **Level Measurement Response Time:** These bits are only used in the Rx mode and have no effect in the Tx mode; they set the 'normal' response time of the Rx signal amplitude and dc offset measuring circuits. This setting will be temporarily overriden by the automatic sequence of an AQLEV command. See Table 5.
For Mobitex systems, and most general-purpose applications using this modem, these bits should be set to 'Peak Averaging', except when the µController detects a receive signal fade, when 'Hold' should be selected.

Continued » » »

Control Register.....

B3, B2 ..... LEVRES

LEVRES .....: The 'Lossy Peak Detect' setting is intended for systems where the µController cannot detect signal fades or the start of a received message; this setting allows the modem to respond quickly to fresh messages and recover rapidly after a fade without µController intervention -this however will be at the cost of reduced Bit-Error-Rate vs Signal-to-Noise performance.
Note that as the measured levels are stored on capacitors C_6 and C_7 via pins Doc 1 and Doc 2, these levels will decay gradually towards V_{BIAS} when the 'Hold' setting is used; the discharge time-constant is approximately 2000 bit-times.
Table 5 details bit-setting application.

B3	B2	Setting	Action
0	0	Hold	Keep current values of amplitude and offset
0	1	Peak Averaging	Track input signal using bit peak averaging
1	0	Peak Detect	Track input signal using peak detection
1	1	Lossy Peak Detect	Track input signal using lossy peak detection

Table 5

B1, B0 PLLBW

PLL Bandwidth: For use in the Rx mode only (no effect in Tx).
In the receive mode these two bits set the 'normal' bandwidth of the Rx Clock Extraction phase locked loop circuit to allow for Rx and Tx Xtal tolerances. This setting will be temporarily overridden by the automatic sequence of an AQBC (Command Register Bit 7) command.

B1	B0	PLL Bandwidth	Suggested Use
0	0	Hold	Signal fades
0	1	Narrow	±20ppm or better Xtals
1	0	Medium	Wide tolerance Xtals or long preamble acquisition
1	1	Wide	Quick acquisition

Table 6

The 'Hold' setting is intended for use during signal fades, otherwise the minimum bandwidth consistent with the Rx and Tx modem bit-rate tolerances should be chosen.
The wide and medium bandwidth settings are intended for systems where the µController cannot detect signal fades or the start of a receive message; as they allow the modem to respond rapidly to fresh messages and recover rapidly after a fade without µController intervention. This action however is at the expense of reduced Bit-Error-Rate vs Signal-to-Noise performance.

Programming Information .....

Mode Register

This 8-bit write-only register controls the basic operating modes of the modem.

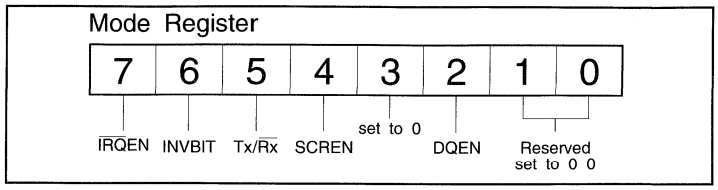


Fig.19 The Mode Register

Mode Register

B7 IRQ EN

IRQ Output Enable: When set to a logic '1' the Interrupt Request output will be pulled low (to V_{SS}) whenever the IRQ bit (BIT 7) of the Status Register is set by the modem to a logic '1'. When set to a logic '0' the Interrupt Request output will not function and will remain in its high-impedance state (see Pin Functions Page).

B6 INVBIT

Invert Bits: When set to a logic '1', all data (sense) voltages to and from the modem's Rx and Tx paths are inverted.

For example:

B6	Tx/Rx Logic '1'	Tx/Rx Logic '0'
'0'	High (above V_{BIAS})	Low (below V_{BIAS})
'1'	Low (below V_{BIAS})	High (above V_{BIAS})

Data will be affected immediately after B6 is set and so this bit should not be changed whilst the modem is decoding or transmitting data. This bit only operates on data bits, there is no effect upon functional logic inputs.

B5 Tx/Rx

Tx/Rx Mode: When set to a logic '1' places the modem in the Transmit mode; when set to a logic '0' places the modem in the Receive mode. To allow the lowpass filter to stabilize, when changing from Rx to Tx there must be a 2 bit pause before setting a new task.
Note that changing between Transmit and Receive modes will cancel any current task.

B4 SCREN

Scramble Enable: Setting this bit to a logic '1' enables data scrambling; setting it to a logic '0' disables scrambling. The scrambler only takes effect during the transmission or reception of a Mobitex Data Block (see Figure 11 -System Data Format) and during TSO (Transmit Scrambler Output) task.
The scrambler is only operative, if enabled by this mode bit (B4), during TSO, RDB or TDB (see Modem Tasks), it is held in the reset state at all other times. This bit should not be changed whilst the modem is decoding or transmitting a Data Block.

B3

This bit should be set to a logic '0'.

B2 DQEN

Data Quality IRQ Enable: For use in the Rx mode only (no effect in Tx).
In the Rx mode, setting this bit to a logic '1' causes the IRQ bit (of the Status Register) to be set to a logic '1' whenever a new Data Quality reading is ready; the DQRDY bit of the Status Register will also be set to a logic '1' at the same time.

B1 B0

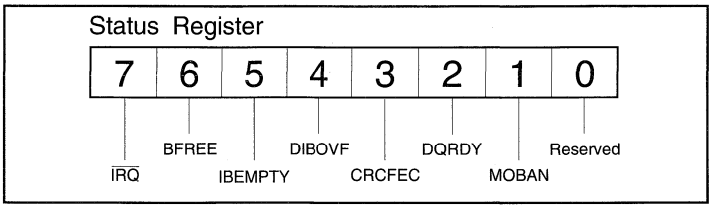
These bits should be set to a logic '0'.

Programming Information .....

Status Register

This register may be read by the µController to determine the current state of the modem.

Fig.20 The Status Register



Status Register

B7 IRQ

Interrupt Request: This bit is set to a logic '1' by:

The Status Register BFREE bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's Tx/Rx bit.

or

The Status Register IBEMPTY bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's Tx/Rx bit.

or

The Status Register DQRDY bit going from a logic '0' to '1' (if DQEN = '1').

or

The Status Register DIBOVF bit going from a logic '0' to '1'.

This (IRQ) bit is cleared to a logic '0' immediately after a read of the Status Register.
If the IRQEN bit of the Mode Register is a logic '1', the FX909 $\overline{IRQ}$ output pin will be pulled low (to V_{SS}) whenever the Status Register IRQ bit is a logic '1'.

B6 BFREE

Data Buffer Free: BFREE reflects the availability of the Data Buffer; BFREE is cleared to a logic '0' *(Buffer NOT Free)* whenever a task other than NULL, RESET or TSO is written to the Command Register.
In Transmit mode, the BFREE bit will be set to a logic '1' (setting the Status Register IRQ bit to a logic '1) when the modem is ready for the µController to write new data to the Data Buffer and the next task to the Command Register.
In Receive mode, the BFREE bit is set to a logic '1' (setting the Status Register IRQ bit to a logic '1) when it has completed a task and any data associated with that task has been placed into the Data Buffer. The µController may then read that data and write the next task to the Command Register.
The BFREE bit is also set to a logic '1' (but without setting the IRQ bit) by a RESET task or when the Mode Register Tx/Rx bit is changed.

B5 IBEMPTY

Interleave Buffer Empty: **In Transmit mode**, IBEMPTY is set to a logic '1' (also setting the IRQ bit) when less than two bits remain in the Interleave Buffer. Any transmit task written to the modem after IBEMPTY goes to a logic '1' will be too late to avoid a gap in the transmit output signal (see Figure 16 and Table 3, Tx Task Timing)
IBEMPTY is also set to a logic '1' by a RESET task and by a change of the Mode Register's Tx/Rx bit, but in this case the IRQ bit will not be set.
IBEMPTY is cleared to a logic '0' by writing a task other than NULL, RESET or TSO to the Command Register.
Note that when the modem is in the transmit mode and the Interleave Buffer is empty, a mid-level (V_{BIAS}) voltage will be fed to the Tx Lowpass Filter.
In Receive mode this bit is a logic '0'.

Status Register .....

B4 DIBOVF	**De-Interleave Buffer Overflow: In Receive mode** DIBOVF is set to a logic '1' (also setting the IRQ bit) when a task is written to the Command Register too late to allow continuous reception (see Figure 17 and Table 3 Rx Task Timing). DIBVOF is cleared to a logic '0' by reading the Status Register, by writing a RESET task to the Command Register or by changing the Tx/Rx bit of the Mode Register. **In Transmit mode** this bit is a logic '0'.
B3 CRCFEC	**CRC or FEC Error: In Receive mode** CRCFEC will be updated at the end of every Data Block task, after checking the CRC, and at the end of receiving Frame Head control bytes, after checking the FEC. A logic '0' indicates that the CRC was received correctly or that the FEC found no uncorrectable errors. A logic '1' indicates that errors are present. CRCFEC is cleared to a logic '0' by a RESET task, or by changing the Tx/Rx bit of the Mode Register. **In Transmit mode** this bit is a logic '0'.
B2 DQRDY	**Data Quality Reading Ready: In Receive mode** DQRDY is set to a logic '1' whenever a Data Quality reading has been completed (see Figure 21 Data Quality graph). DQRDY is cleared to a logic '0' by a read of the Data Quality Register, or by changing the Tx/Rx bit of the Mode Register.
B1 MOBAN	**Mobile or Base Bit-Sync Received: In Receive mode** the MOBAN bit is updated at the end of the SFS and SFH tasks. MOBAN is set to a logic '1' whenever the 3 bits immediately preceding a detected Frame Sync are '0' '1' '1' (received left to right), with up to any one bit in error. MOBAN is set to a logic '0' if the bit pattern is '1' '0' '0', again with up to any one bit in error. Thus if this bit is set to a logic '1' then the received message is likely to have originated from a mobile station, and if set to a logic '0' the call is likely to have originated from a base station. The Data Formats section of this document describes the different mobile and base sync structures. **In Transmit mode** this bit is a logic '0'.
B0	This bit is always set to a logic '0'.

Programming Information .....

The Data Quality Register

The information presented in this 8-bit register is intended to indicate the quality of the receive signal during a Data Block or 30 single bytes.

In Receive Mode, the modem measures the quality of the received signal by comparing the actual received zero-crossing time against an internally generated time. This value is averaged over 240 bits and at the end of the measurement the Data Quality Register and the Data Quality Reading Ready (DQRDY) bit in the Status Register are updated. An interrupt will only occur at this time if the DQEN bit in the Mode Register = logic '1'.

In Transmit Mode all bits are set to a logic '0'.

To provide synchronisation with Data Blocks, and hence ensure that the DQ Register is updated ready to be read when the RDB task finishes, the measurement process is reset at the end of Tasks SFH, SFS, RDB and R3H.

Figure 21 shows how the value (0 - 240) read from the Data Quality Register varies with received signal-to-noise ratio.

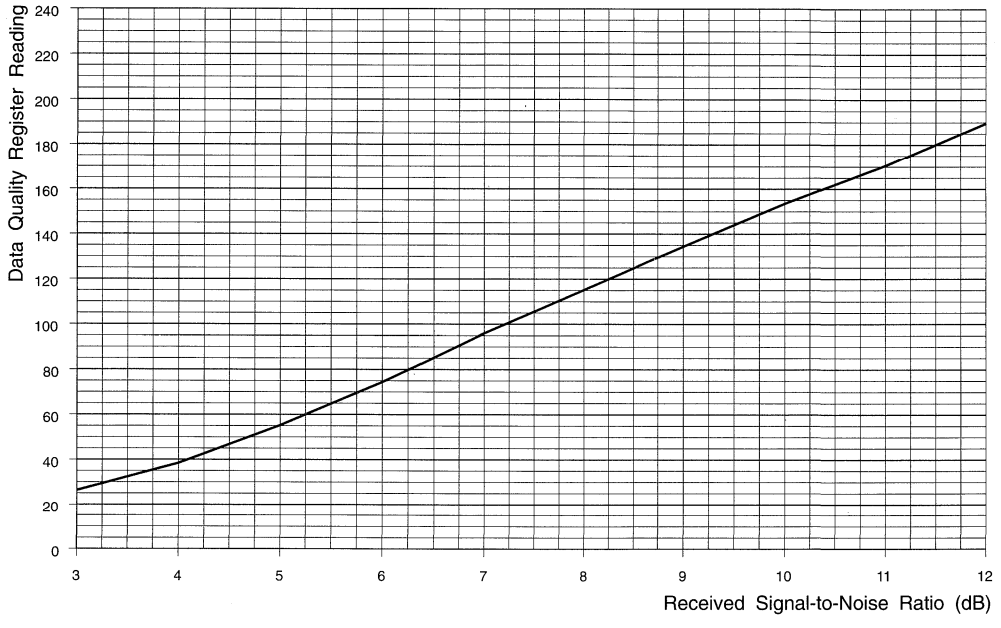


Fig.21 Typical Data Quality Reading vs Rx Signal-to-Noise Ratio (calculated for noise in a bit-rate bandwidth)

Programming Information .....

FX909 Registers

This diagram may provide a useful quick-reference to FX909 register allocations.

Register Selection

Write to Modem	A_1	A_0	Read from Modem
Data Buffer	0	0	Data Buffer
Command Register	0	1	Status Register
Control Register	1	0	DQ Register
Mode Register	1	1	not used

Command Register

7	6	5	4	3	2	1	0
AQBC	AQLEV	Reserved set to 0 0 0				TASK	

AQBC - Acquire Bit Clock
AQLEV - Acquire Receive Signal Levels
TASK:

B2	B1	B0	Rx Mode	
0	0	0	NULL	
0	0	1	SFH	Search For Frame Head
0	1	0	R3H	Read 3-byte Frame Head
0	1	1	RDB	Read Data Block
1	0	0	SFS	Search For Frame Sync
1	0	1	RSB	Read Single Byte
1	1	0	LFSB	Load Frame Sync Bytes
1	1	1	RESET	

B2	B1	B0	Tx Mode	
0	0	0	NULL	
0	0	1	T7H	Transmit 7-Byte Frame Head
0	1	0		Reserved
0	1	1	TDB	Transmit Data Block
1	0	0	TQB	Transmit 4 Bytes
1	0	1	TSB	Transmit Single Byte
1	1	0	TSO	Transmit Scrambler Output
1	1	1	RESET	

Control Register

7	6	5	4	3	2	1	0
CKDIV		HI/LO	DARA	LEVRES		PLLBW	

CKDIV - Clock Division Ratio

B7	B6	B5 = 1	B5 = 0	
0	0	256	128	Xtal / Bit-Rate
0	1	512	256	
1	0	1024	512	
1	1	2048	1024	

HI/LO - High or Low Xtal Range Selection
DARA - Data Rate
LEVRES - Level Measurement Response Time

B3	B2	
0	0	Hold
0	1	Peak Averaging
1	0	Peak Detect
1	1	Lossy Peak Detect

PLLBW - PLL Bandwidth

B1	B0	Bandwidth
0	0	Hold
0	1	Narrow
1	0	Medium
1	1	Wide

Mode Register

7	6	5	4	3	2	1	0
$\overline{IRQEN}$	INVBIT	Tx/$\overline{Rx}$	SCREN	set to 0	DQEN	Reserved set to 0 0	

$\overline{IRQEN}$ - $\overline{IRQ}$ Output Enable
INVBIT - Invert Bit
Tx/Rx - Transmit or Receive Mode
SCREN - Scramble Enable
DQEN - Data Quality IRQ Enable

Status Register

7	6	5	4	3	2	1	0
$\overline{IRQ}$	BFREE	IBEMPTY	DIBOVF	CRCFEC	DQRDY	MOBAN	Reserved

$\overline{IRQ}$ - Interrupt Request
BFREE - Data Buffer Free
IBEMPTY- Interleave Buffer Empty
DIBOVF - De-Interleave Buffer Overflow
CRCFEC - CRC or FEC Error
DQRDY - Data Quality Reading Ready
MOBAN - Mobile or Base Bit-Sync Received

Fig.22 Ready-Use Guide to Register Functions

Operational Information

Operation Details

Cyclic Redundancy Code (CRC)

A 16-bit CRC code is used in the Mobitex Data Block.

In Transmit Mode the CRC is calculated by the modem from the 18 data bytes (see Figure 11 Mobitex System Data Format) using the following generator polynomial:

$$g(x) = x^{16} + x^{12} + x^5 + 1 \qquad \text{[CCITT CRC-16]}$$

This code detects all (single) error bursts of up to 16 bits in length and about 99.998% of all other error patterns.

The CRC Register is intialised to all logic '1's and the CRC is calculated octet by octet starting with the LSB of byte 0. The CRC calculated is bit-wise inverted and appended to the data bytes with the MSB transmitted earliest.

In Receive Mode a 16-bit CRC code is generated from the 18 data bytes of each Mobitex Data Block as described above and the bit-wise inverted value is compared with the received CRC bytes, if a mis-match is present then an error has been detected.

Forward Error Correction (FEC)

In Transmit Mode, during T7H and TDB, the modem generates a 4-bit Forward Error Correction code for each coded byte.

The FEC is defined by the following H matrix:

	DATA BYTE								*FEC*			
	MSB							LSB	MSB			LSB
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**3**	**2**	**1**	**0**
H =	1	1	1	0	1	1	0	0	1	0	0	0
	1	1	0	1	0	0	1	1	0	1	0	0
	1	0	1	1	1	0	1	0	0	0	1	0
	0	1	1	1	0	1	0	1	0	0	0	1

Generation of the FEC consists of logically ANDing the byte to be transmitted with bits 7 to 0 of each row of the H matrix. Even parity is generated for each of the 4 results and these 4 parity bits, in the positions indicated by the last 4 columns of the H matrix, form the FEC code.

Receive Mode: In checking the FEC the received 12-bit word is logically ANDed with each row of the H matrix (earliest bit received compared with the first column). Again even parity is generated for the 4 resulting words and these parity bits form a 4-bit nibble. If this nibble = 0 then no errors have been detected. Other results 'point' to the bit in error or indicate that uncorrectable errors have occured.

This code can correct any single error that has occured in each 12-bit (8 data + 4 FEC) section of the message.

Example of FEC Generation

If the byte to be coded is **'0 0 1 0 1 1 0 0'**, then the FEC is derived as follows:

H Matrix Row	1	2	3	4
A	1 1 1 0 1 1 0 0	1 1 0 1 0 0 1 1	1 0 1 1 1 0 1 0	0 1 1 1 0 1 0 1
B	**0 0 1 0 1 1 0 0**	**0 0 1 0 1 1 0 0**	**0 0 1 0 1 1 0 0**	**0 0 1 0 1 1 0 0**
A 'AND' B	0 0 1 0 1 1 0 0	0 0 0 0 0 0 0 0	0 0 1 0 1 0 0 0	0 0 1 0 0 1 0 0
Even Parity	1	0	0	0

With reference to the table above, Row A is bit 7 to 0 of one row of the H matrix and Row B is the byte to be coded. The Even Parity bits refer to the result of 'A' AND 'B'.

Therefore the word formed will be: **'0 0 1 0 1 1 0 0 1 0 0 0'** -sent left to right.

When the same process is carried out on these 12 bits (**'0 0 1 0 1 1 0 0 1 0 0 0'**), using all 12 bits of each H matrix row, the resulting parity bits will be **'0 0 0 0'.**

Operational Information .....

Operation Details .....

Interleaving

The 240 bits of a Data Block are interleaved by the modem before transmission to give protection against noise bursts and short fades. Interleaving is not performed on any bits in the Frame Head.

Considering the 240 bits to be numbered sequentially before interleaving as 0 to 239 (0 = bit 7 of byte 0, 11 = bit 0 of the FEC for byte 0, and ..... ,239 = bit 0 of the FEC for byte 19), then they will be transmitted as shown in Figure 23.

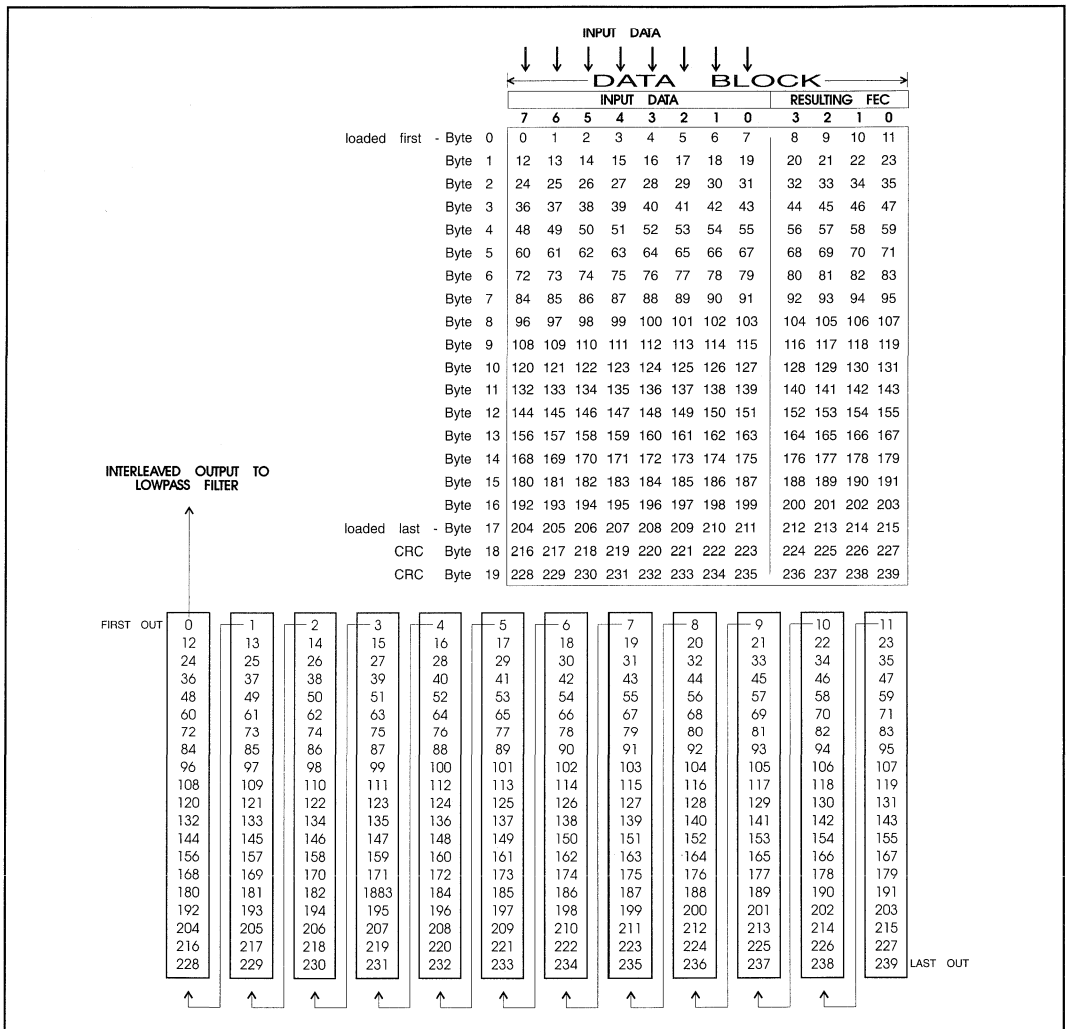


Fig.23 Interleaving - Input/Output

Scrambling

The Data Block may be transmitted or received as scrambled information in accordance with the setting of the Scramble Enable bit (Mode Register SCREN).

All formatted bits of a Data Block are passed through a 9-bit scrambler. This scrambler is initialised at the beginning of the first data block in every frame.

The 511-bit sequence is generated with a 9-bit shift register with the output of the 5th and 9th stages being Exclusive OR'd and fed back to the input of the 1st stage. The scrambler is enabled when SCREN = logic '1' or when the Transmit Scrambler Output (TSO) task is selected but disabled during all others.

Operational Information .....

Rx/Tx Note

The filtering required to reduce the transmitted bandwidth causes energy from each bit of information to be smeared across 3 bit-times. To ensure that the last bit transmitted is received correctly it is necessary to add an 8 bit 'hang byte' to the end of each message. Thus the tasks required to transmit an isolated Mobitex frame are:

$$T7H + (n \times)TDB + TSB$$

When receiving this data the extra byte can be ignored as its only function is to ensure integrity of the last bit and not to carry any information itself.

It is suggested that a '00110011' or '11001100' pattern is used for this 'hang byte'.

"Receive Frame" Example

If the FX909 is required to receive a Mobitex Frame the following sequences of control and data will have to be issued:

Sequence Explanation	Action
Prerequisites: V_{DD} Applied; PLLBW, LEVRES, DARA, CKDIV and SCREN set as required; Tx/Rx set to Rx mode - Carrier has been detected	Tx/Rx = '0'
Steps	
1 Set AQLEV and AQBC bits, 2 bit-periods after the carrier has been detected, to initiate the level acquisition and bit clock extraction sequences -	AQLEV = '1' AQBC = '1'
2 2 Frame Sync bytes loaded to Data Buffer followed by setting LFSB task -	Write to Data Buffer LFSB
3 FX909 interrupts with IRQ when the 2nd byte is read from the Data Buffer -	IRQ
4 Status Register is read - Task is set to search for a Mobitex Frame Head -	BFREE = '1' Task = SFH
5 FX909 will interrupt with IRQ when a valid frame sync is detected and the header bytes decoded with no uncorrectable errors -	IRQ
6 Status Register is read - MOBAN bit checked and 2 frame head control bytes read -	BFREE = '1' MOBAN = '1' or '0' Read from Data Buffer
7 Task is set to receive a Mobitex Data Block	Task = RDB
8 FX909 will interrupt with IRQ when a data block has been received and the CRC has been calculated -	IRQ
9 Status Register is read, CRC validity checked and 18 data block bytes read -	BFREE = '1' CRCFEC = '1' Read from Data Buffer
10 Set task if more information is expected: GOTO Step 4 if last data block received and another Frame Head is imminently expected GOTO Step 7 if another Mobitex Data Block is expected	 Step 4 Step 7
If the last data block has been decoded and no more information is expected then the task bits need not be set as the FX909 will automatically select the idle state.	

"Transmit Frame" Example

If the FX909 is required to send a Mobitex Frame the following sequences of control and data will have to be issued:

Sequence Explanation	Action
Prerequisites: V_{DD} Applied; SCREN, DARA and CKDIV set as required; Tx/Rx set to Tx mode -	Tx/Rx = '1'
Steps	
1 6 bytes forming the frame head are loaded into the data buffer -	Write to Data Buffer
followed by a 2 bit-period pause to let the filter stabilise -	
followed by setting the Transmit 7-Byte Frame Head task -	Task T7H
2 FX909 interrupts with IRQ when the 6th byte is read from the data buffer -	IRQ
3 Status Register is read -	BFREE = '1'
18 bytes of data are loaded into the data buffer -	Write to Data Buffer
followed by setting the Transmit Data Byte task -	TDB
4 FX909 interrupts with IRQ when the 18th byte is read from the data buffer -	IRQ
5 Status Register is read -	BFREE = '1'
Host may load data and set next task as required:	
GOTO Step 1 if the last data block for this frame has been transmitted and another frame is to be immediately transmitted -	Step 1
GOTO Step 3 if another data block in this frame is to be transmitted -	Step 3
GOTO Step 6 if the last data block for this frame has been transmitted and no more data is to be immediately sent -	Step 6
6 1 byte representing the 'hang byte' is loaded into the Data Buffer -	Write to Data Buffer
followed by setting the Transmit Single Byte task -	TSB
After the 'hang byte' has been transmitted and no more data is to be sent then a new task need not be written and the µController can wait for the IBEMPTY interrupt when it can, if required, shut down the Tx RF circuits.	

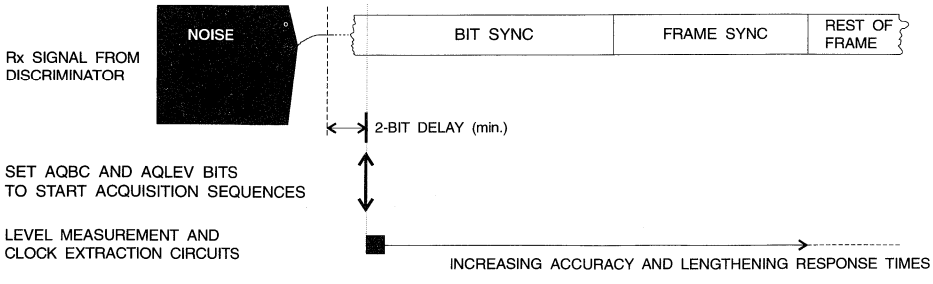


Fig.24 Bit-Clock and Level Acquisition Example

Operational Information .....

Received Signal Acquisition

Level Measurement and Clock Extraction

To achieve reasonable error rates the FX909 modem needs to make accurate measurements of the received signal amplitude, dc offset and bit-timing. Accurate measurements, especially in the presence of noise, are best made by averaging over a relatively long time period.

In most cases the modem will be used to receive isolated messages from a distant transmitter that is only turned on for a very short time before the message starts; also, the received baseband signal from the radio's frequency discriminator will have a dc offset due to small differences between the receiver and transmitter reference oscillators and hence their 'carrier' frequencies.

To cater for this situation, AQBC and AQLEV (Acquire Bit Clock and Level) commands are provided which, when triggered, cause the modem to follow an automatic sequence designed to perform the measurements as quickly as possible.

Note that due to the delay through the Rx lowpass filter, the AQBC and AQLEV sequences should not be started until about 2-bit times after the Rx carrier has been detected.

In a system where the controlling µController is not able to detect the Rx carrier, the AQBC and AQLEV sequences may be started at any time; possibly when no carrier is being received. However in this case the clock and level acquisition operation will take longer as the circuits will have to recover from the change from a large amplitude noise signal at the output of the frequency discriminator to the wanted signal, probably with a dc offset. In this type of system the time between the turn-on of the transmitter and the start of the Frame Sync pattern should be extended -preferably by extending the Bit Sync sequence to 32 or even 48 bits.

Warning: Clock extraction circuits work by detecting the timing of received edges, i.e. a change from '0' to '1' or '1' to '0'. They will eventually fail if logic '1's' or logic '0's' are transmitted continuously. Similarly, the level measuring circuits require '00' and '11' bit-pairs to be received at reasonably frequent intervals.

Guides to AQBC and AQLEV sequences are given below. See Figure 24.

Acquire Receive Signal Levels (AQLEV)

The Acquire Receive Signal Levels (AQLEV) sequence starts with a measurement of the average signal voltage over a period of 1 bit-time. The sequence continues by measuring the positive-going and negative-going peaks of the signal. The attack and decay times used in this 'lossy peak detect' mode are such that a sufficiently accurate measurement can be made within 16 bits of a '11001100 ...' pattern (i.e the bit-sync sequence) to allow the bit-clock extraction circuits to operate.

Once the device has detected frame sync. or, if SFH or SFS has not been set, after 30 bits, then the the level measurement circuits will switch to the residual setting: 'Lossy Peak Detect', 'Peak Detect', 'Peak Averaging' or 'Hold'. Note that for normal operation the LEVRES bits would only be set to 'Hold' for the duration of a fade.

Sequence

SFH or SFS is set; Frame Sync is being searched for:
- 1 bit of clamp
- Lossy Peak detect until Frame Sync is detected
- Residual setting.

SFH or SFS is not set; Frame Sync is not being searched for:
- 1 bit of clamp.
- 30 bits of Lossy Peak Detect.
- Residual setting.

Acquire Bit Clock (AQBC)

The Acquire Bit Clock (AQBC) sequence follows a similar pattern; starting with a very fast initial estimate of the received bit timing (Wide), when the AQBC bit is set.

When the device has detected Frame Sync. or, if SFH or SFS has not been set after 16 bits, then the bandwidth is set to Medium. 30 bits later the clock extraction circuits will change to the residual value.

Sequence

SFH or SFS is set; Frame Sync is being searched for:
- 'Wide' setting until Frame Sync detected.
- 30 bits of 'Medium' setting.
- Residual setting.

SFH or SFS is not set; Frame Sync is not being searched for:
- 16 bits of 'Wide' setting.
- 30 bits of 'Medium' setting.
- Residual setting.

Control and Data Load Timing

Control Instructions, Task and Data is loaded to the FX909 in a parallel form as detailed in the relevant Programming Information sections of this Data Sheet. Timing information for Read and Write operations is given in Figure 25; timing parameters are provided in the Specification section.

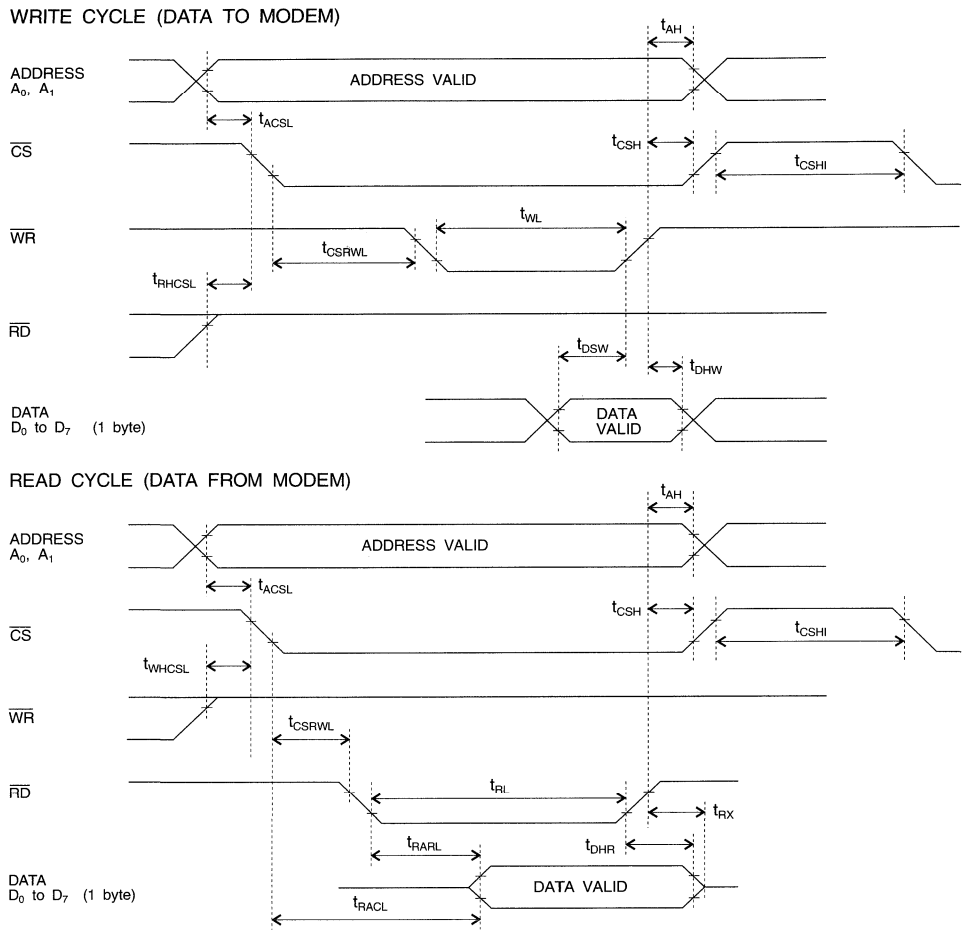


Fig.25 FX909 - µProcessor Read/Write Timing

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating temperature range: **FX909J4/L2**	-40°C to +85°C
Storage temperature range: **FX909J4/L2**	-40°C to +85°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Remarks	Min.	Max.	Unit
Supply Voltage (V_{DD})		4.5	5.5	V
Operating Temperature (T_{OP})		-40.0	+85.0	°C
Bit Rate		4,000	19,200	bits/sec
Xtal/Clock Frequency		1.0	10.0	MHz

Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 4.5 to 5.5V, T_{OP} = -40°C to +85°C. Xtal/Clock Frequency = 4.096MHz. Bit Rate = 8,000 bits/sec. Noise Bandwidth = Bit Rate.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
I_{DD}	1	-	3.0	-	mA
Tx Output *See also Figure 26*					
Impedance	2	-	1.0	2.5	kΩ
Signal Level	3	0.9	1.0	1.1	Vp-p
Tx Data Delay	4	-	4.0	6.0	bits
Rx Input					
Impedance (Rx In pin)		10.0	-	-	MΩ
Rx Input Amp Voltage Gain		-	500	-	V/V
Input Signal Level	5	0.7	1.0	1.3	Vp-p
Rx Data Delay	6	-	3.5	-	bits
Xtal/Clock					
'High' pulse Width	7	40.0	-	-	ns
'Low' pulse Width	7	40.0	-	-	ns
Input Impedance		10.0	-	-	MΩ
Inverter Gain (I/P = 1mV rms @ 1kHz)		20.0	-	-	dB
µController Interface					
Input logic '1' Level	8, 9	V_{DD} -1.5	-	-	V
Input Logic '0' Level	8, 9	-	-	1.5	V
Input Leakage Current (V_{IN} = 0V to V_{DD})	8, 9	-5.0		+5.0	µA
Input Capacitance	8,9	-	10.0	-	pF
Output Logic '1' Level (IOH = 120µA	9	V_{DD} -0.4			V
Output Logic '0' Level (IOL = 360µA)	9,10	-	-	0.4	V
'Off' State Leakage Current (V = V_{DD})	10	-	-	10	µA

Specification .....

Modem Read/Write Load Timing

Description		Spec. Page Note	Min.	Typ.	Max.	Unit
t_{ACSL}	"Address Valid" to "CS Low" time		0	-	-	ns
t_{AH}	"Address Hold" time		0	-	-	ns
t_{CSH}	"CS Hold" time		0	-	-	ns
t_{CSHI}	"CS High" time	12	6.0	-	-	Xtal/Clock Cycles
t_{CSRWL}	"CS" to "WR" or "RD" Low time		0	-	-	ns
t_{DHR}	"Read-Data Hold" time		0	-	-	ns
t_{DHW}	Write-Data Hold time		0	-	-	ns
t_{DSW}	Write-Data Set-Up" time		90.0	-	-	ns
t_{RHCSL}	"RD High" to "CS Low" time (write cycle)		0	-	-	ns
t_{RACL}	"Read Access" time from "CS Low"	11	-	-	175	ns
t_{RARL}	"Read Access" time from "RD Low"	11	-	-	145	ns
t_{RL}	"RD" Low time		200	-	-	ns
t_{RX}	"RD High" to "D_0-D_7 3-State" time		-	-	50.0	ns
t_{WHCSL}	"WR High" to "CS Low" time (read cycle)		0	-	-	ns
t_{WL}	"WR" Low time		200	-	-	ns

Notes:

1. Not including any current drawn from the modem pins by external circuitry.
2. Small signal impedance (dynamic measurement).
3. Measured after external CR (R_4/C_6) filter, for 1111000011110000.. bit sequence; at V_{DD} = 5.0V (output level is proportional to V_{DD}).
4. Measured between issuing first task after idle and the centre of the first bit at Tx Out (see Figure 14, 'The Transmit Process').
5. For optimum performance, measured at the Rx Feedback pin, for a '...11110000...' bit sequence.
6. Measured between centre of last bit of an Rx single byte or Frame Sync at Rx In and an IRQ interrupt to the µController.
7. Timing for an external input to the Xtal/Clock pin.
8. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A_0 and A_1 pins.
9. D_0 - D_7 pins.
10. $\overline{IRQ}$ pin.
11. With 30pF (Max.) to V_{SS} on D_0 - D_7 pins.
12. Xtal/Clock cycles at the Xtal/clock pin.

Specification .....

Lowpass Filter Response

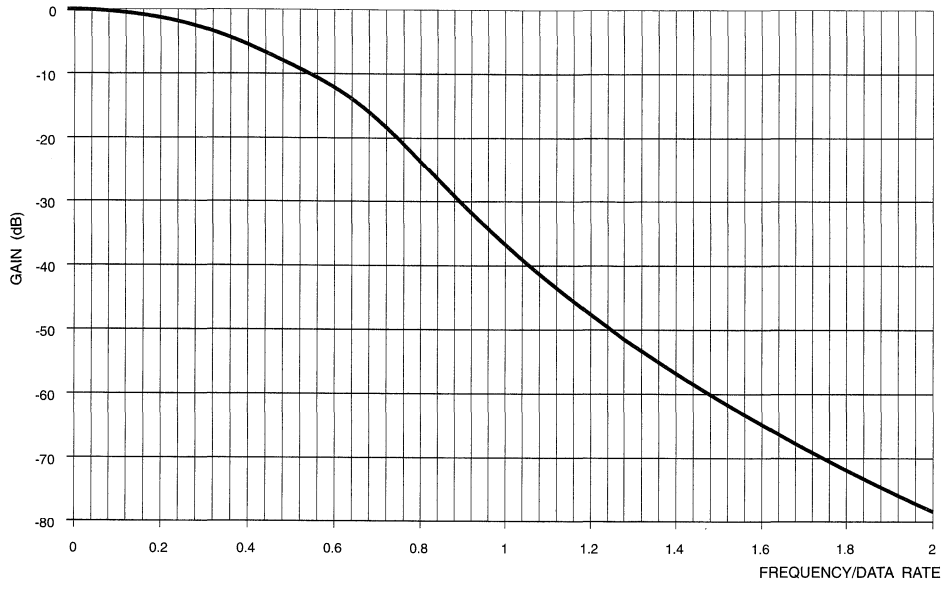


Fig.26 Lowpass Filter Response (Including the External RC Filter Components) in the Tx Mode

Signal-to-Noise Performance

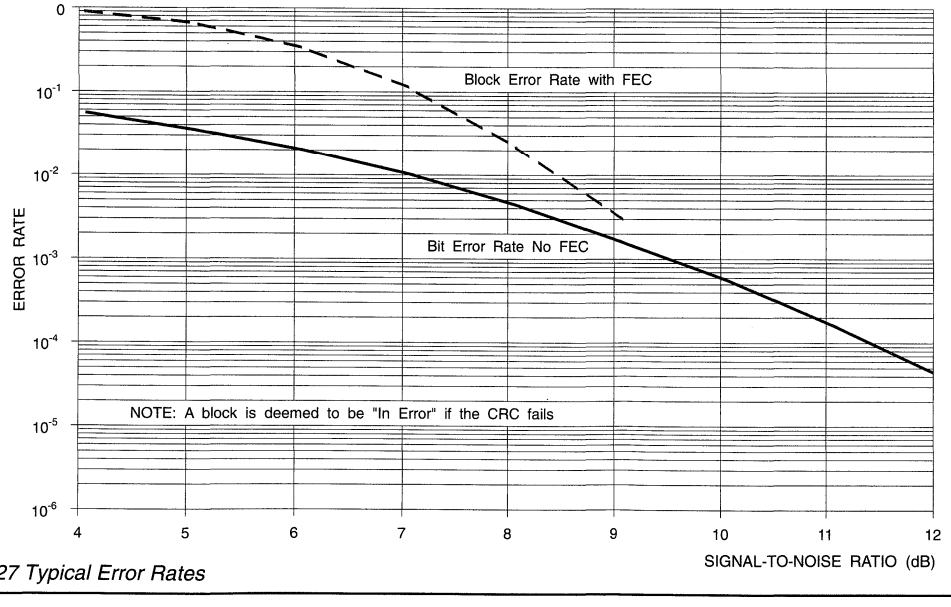


Fig.27 Typical Error Rates

Bit and Block Errors

The figure above shows both bit and block error possibilities for a received signal with a specific signal-to-noise performance. Bit Errors are individually detected errors in the raw data stream.

Block Errors are those where a complete block of data (240 bits; see Figure 11 Data Format) is in error (as indicated by the CRC).

Note that signal-to-noise ratios illustrated in this Data Sheet are calculated for noise in a bit-rate bandwidth.

Package Outlines

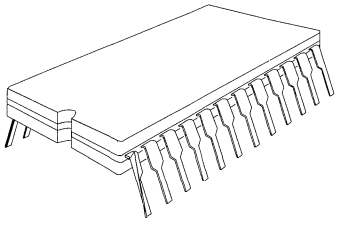
The FX909 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX909 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX909J 24-pin cerdip DIL (J4)

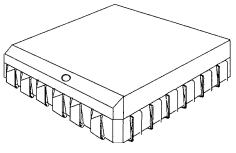
NOT TO SCALE



Max. Body Length 32.03mm
Max. Body Width 14.81mm

FX909LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX909J	24-pin cerdip DIL	(J4)
FX909LS	24-lead plastic leaded chip carrier	(L2)

CML Semiconductor Products

PRODUCT INFORMATION

FX919 Four-Level FSK "Packet Data" Modem

Publication D/919/1 July 1994
Advance Information

Features

- **FM Radio Packet Data Applications**
  - Wireless Data Systems
  - Radio Telemetry
  - Mobile Data Links
  - Wireless LANs
  - Point-Of-Sale and 'Swipe' Terminals
  - Bar-Code Readers and Stock Control
- **Flexible Message Formatting**
- **Automatic Protocol Handling**
  - Symbol and Frame Sync
  - Block Formatting
  - Forward Error Correction
  - CRC Check and Generation
  - Interleaving
- **4-Level FSK - 4800 to 19200b/s**
- **5mA at 5 Volt; Low-Power**

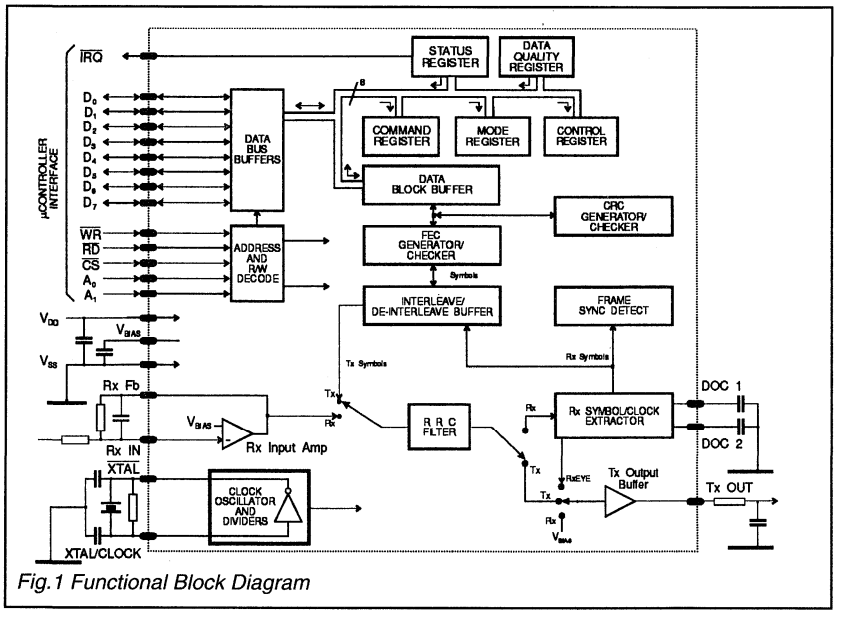


Fig.1 Functional Block Diagram

FX919

Brief Description

The FX919 performs the baseband signal processing and most of the data formatting/de-formatting required to implement a 4-level FSK modem for use with FM radio and data links. Having a low power requirement of 5.0mA at 5 volts, this modem provides:

❍ A versatile frame structure for general-purpose applications.

❍ Automatic handling of frame structures, including Rx symbol and frame synchronization, block formatting, CRC generation and checking, Forward Error Correction and Interleaving to reduce the processing load on the host µController.

❍ Selectable data rates of 2400 to 9600 symbols/s (4800 to 19200bits/s) in high-speed, half-duplex operation.

❍ 4-Level FSK (2 bits per baud) enabling economical data-rates in a narrow RF bandwidth.

❍ On-chip baseband processing and filtering.

❍ Pre-selectable signal acquisition and tracking permits the rapid acquisition of received signals, followed by automatic tracking of signal dc level variations.

Clock recovery PLL bandwidth and Rx signal level measurement circuitry will react automatically.

Rx and Tx data and control between the host µController and this microcircuit is via an 8-bit bi-directional parallel interface; input and output signals to and from the radio system are in analogue form suitable for connection to the radio's discriminator and frequency modulator.

The FX919 is available in both 24-pin DIL and Surface Mount packages.

Introduction

Table of Contents

FX919 Circuit Descriptions (See Figure 2)

Data Bus Buffers

Eight bi-directional 3-state logic-level buffers between the modem's internal registers and the controlling µController's data-bus lines.

Address and R/W Decode

Control the transfer of data bytes between the µController and the modem's internal registers, according to the state of the Write and Read Enable ($\overline{WR}$ and $\overline{RD}$) inputs, the Chip Select ($\overline{CS}$) input and the Register Address inputs (A_0 and A_1).

The Data Bus Buffers and Address with R/W Decode blocks provide a byte-wide parallel µController interface.

Status and Data Quality Registers

8-bit registers which the µController can read to determine the status of the modem and the received data quality.

Command, Mode and Control Registers

The values written by the µController to these 8-bit registers control the operation of the modem.

Data Block Buffer

A 12-byte buffer used to hold Rx or Tx data to or from the µController.

CRC Generator/Checker

A circuit which generates (transmit mode) or checks (receive mode) the Cyclic Redundancy Checksum bits which may be included in transmitted data blocksto allow the receive modem to detect transmission errors.

FEC Generator/Checker

In transmit mode, this circuit adds Forward Error Correction bits to the transmitted data, then converts the resulting binary data to 4-level symbols. In receive mode, it translates received 4-level symbols to binary data, using the FEC information to correct a large proportion of transmission errors. The 4 possible levels of a symbol are referred to in this Data Sheet as: +3, +1, -1 and -3.

Interleave/De-interleave Buffer

Interleaves data symbols within a data block before transmission and de-interleaves the received data so that the FEC system is best able to handle short noise bursts or fades.

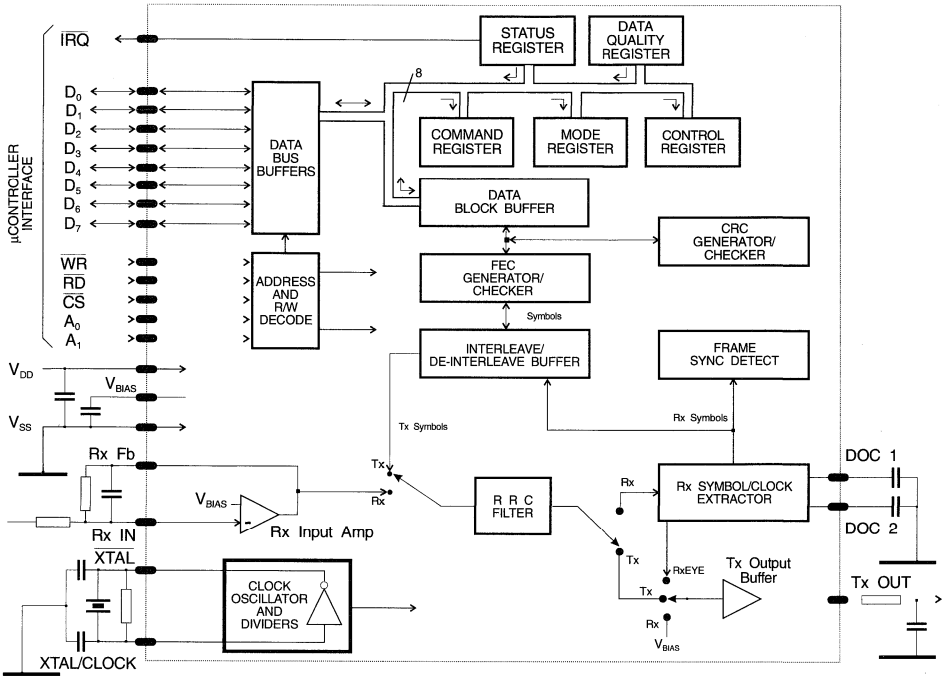


Fig.2 FX919 Functional Block Diagram

Rx Input Amp

The amplifier that allows the received signal input to the modem to be set to the optimum level by the selection of suitable external components.

Frame Sync Detect

This circuit, which is only active in the receive mode, is used to look for the 24-symbol Frame Synchronisation pattern which is transmitted to mark the start of every frame.

Root Raised Cosine (RRC) Filter See Figure 27

This filter, which is used in both transmit and receive modes, is a linear-phase lowpass filter with a 'Root Raised Cosine' frequency response.

In Tx mode, the 4-level symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In Rx mode this filter is used to reject HF noise and to equalise the received signal to a form suitable for extracting the 4-level symbols.

Rx Symbol/Clock Extraction

These circuits, which operate only in receive mode, extract a symbol-rate clock from the received signal, and measure the received signal amplitude and its dc offset.

This information is then used to extract the received 4-level symbols and also to provide an input to the received Data Quality measuring circuit.

Clock Oscillator and Dividers

This circuit derives the transmit symbol-rate (and the nominal receive symbol-rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or fed from an external source.

Tx Output Buffer

A unity-gain amplifier used in the transmit mode to buffer the output of the RRC filter. In receive mode, the input of this buffer is normally connected to V_{BIAS} unless the RxEYE bit of the Mode Register is set. When the FX919's mode is changed from receive to transmit, the input to this buffer will remain connected to V_{BIAS} for a period of 8 symbol times while the RRC filter settles. See Programming Information section.

Pin Functions

FX919 (J4 and L2)	
1	**$\overline{IRQ}$:** A 'wire-ORable' output for connection to the controlling µController's Interrupt Request input. This output has a low-impedance pull-down to V_{SS} when active, and is high-impedance when inactive.
2	**D_7:**
3	**D_6:**
4	**D_5:**
5	**D_4:** 8 bi-directional 3-state µController interface data lines.
6	**D_3:**
7	**D_2:**
8	**D_1:**
9	**D_0:**
10	**$\overline{RD}$:** An active-low logic level input used to control the reading of data from the modem into the controlling µController.
11	**$\overline{WR}$:** An active-low logic level input used to control the writing of data into the modem from the controlling µController.
12	**V_{SS}:** The negative supply rail (ground).
13	**$\overline{CS}$:** An active-low logic level input to the modem used to enable a data Read or Write operation (see Figure 26, Timing).
14	**A_0:** Two logic-level modem register selection inputs.
15	**A_1:**
16	**$\overline{Xtal}$:** The output of the on-chip Xtal oscillator. Note that since the FX919 uses dynamic logic internally, operation without a suitable Xtal or clock input for more than a few milli-seconds will cause the current taken from V_{DD} to rise slowly to about twice its normal value, and may cause the state of the µController interface to become undefined.
17	**Xtal/Clock:** The input to the on-chip Xtal oscillator.
18	**Doc 2:** Connections to the internal Rx signal level measurement circuitry. Capacitors as described in Figure 3 should be fitted from each of these pins to V_{SS}. Any test equipment connected to these pins should have an input resistance of at least 100MΩ to V_{SS} to avoid disturbance of the measured levels.
19	**Doc 1:**
20	**Tx Out:** The Tx signal output from the modem.
21	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to V_{SS} by a capacitor mounted close to the device pins.
22	**Rx In:** The input to the Rx input amplifier.
23	**Rx Fb (Rx Feedback):** The output of the Rx Input Amplifier, and the input to the (Rx) Lowpass Filter.
24	**V_{DD}:** The positive supply. Levels and voltages within the modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the device pins.

Application Information

External Components

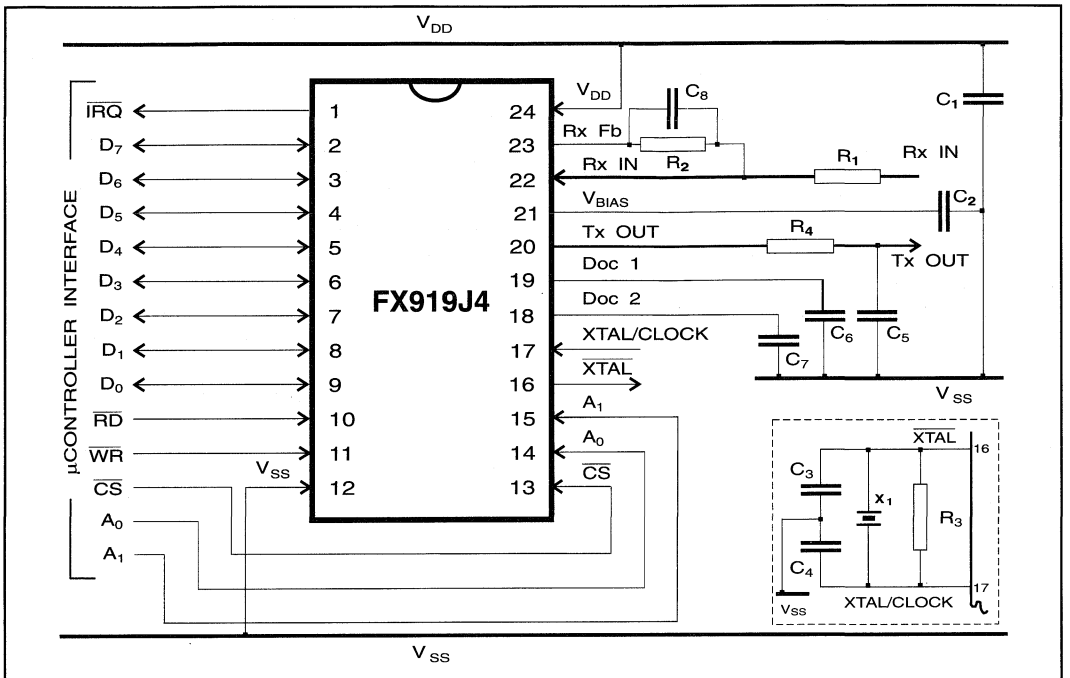


Fig.3 Recommended External Components

Component	Value	Tolerance
R_1	Note 1	±5%
R_2	100kΩ/Note 1	±5%
R_3	1.0MΩ	±20%
R_4	100kΩ/Note 2	±5%
C_1	0.1µF	±20%
C_2	0.1µF	±20%
C_3	Note 3	±20%
C_4	Note 3	±20%
C_5	Note 2	±5%
C_6	Note 4	±20%
C_7	Note 4	±20%
C_8	Note 1	±5%
X_1	4.9152MHz/Table 4	

Installation Notes

1. Resistors R_1 and R_2, with the Rx Input Amplifier, set the signal input level to the modem.
   The value of R_1 should be calculated to give 1.0v p-p at the Rx Feedback pin for a received +3 +3 -3 -3 +3 +3 -3 -3 sequence. The dc level of the received signal should be such that under nominal conditions the signal at the modem's Rx Feedback pin is centred around V_{BIAS}. Suggested values for R_2 and C_8 (including stray capacitance) for differing symbol-rates are:

Symbol-rate (s/s)	R_2	C_8
2,400	100kΩ	330pF
4,800	100kΩ	150pF
9,600	100kΩ	82.0pF

2. External components R_4 and C_5 form an RC lowpass filter between the Tx Buffer output and the input to the radio's frequency modulator; this is an important part of the Tx signal filtering. These components may form a part of any dc level shifting and gain adjustment circuitry.
   The ground connection (V_{SS}) of C_5 should be positioned to give maximum attenuation of high frequency noise into the modulator.
   Suggested values for R_4 and C_5 (including stray capacitance) for differing symbol-rates are:

Symbol-rate (s/s)	R_4	C_5
2,400	100kΩ	330pF
4,800	100kΩ	150pF
9,600	100kΩ	82.0pF

3. The values used for C_3 and C_4 should be suitable for the particular Xtal used as X_1.
   As a guide, values (including stray capacitances) of 33pF at 1.0MHz falling to 18pF at 10MHz will generally prove suitable.
   The equivalent series resistance of X_1 should be less than 2.0kΩ for a frequency of 1.0MHz, falling to 150Ω (max.) for X_1 = 10.0MHz. For optimum performance the frequency tolerance of X_1 should be ±10ppm or better, although tolerances as wide as ±50ppm may be used at the cost of slightly reduced bit-error-rate performance. .....

Installation Notes (Note 3) continue on the next page .....

Application Information .....

Installation Notes .....

3.....

...If the on-chip Xtal oscillator is to be used, then the external components X_1, C_3, C_4, and R_3 are required as shown in Figure 3 (inset). If an external clock source is to be used these components are not required; the input should be connected to the Xtal/clock pin and the $\overline{\text{Xtal}}$ pin left unconnected. Table 4 (Clock/Data Rates) provides advice on the selection of the correct Xtal value.

4. External capacitors C_6 and C_7 form part of the received signal level measuring circuit (Doc1 and Doc 2). For optimum performance the values of these components should be as shown below.

Operation	C_6 and C_7
2400 symbols/sec	22.0nF
4800 symbols/sec	10.0nF
9600 symbols/sec	4.7nF

Binary to Symbol Translation

Although the over-air signal, and hence the signals at the modem Tx Out and Rx In pins, consists of 4-level symbols, the raw data passing between the modem and the µController is in binary form. The FX919 translates between binary data and the 4-level symbols in one of two ways, depending on the task being performed:

Direct

The simplest form, which converts between 2 binary bits and one symbol according to the table below.

Symbol	MSB	LSB
+3	1	1
+1	1	0
-1	0	0
-3	0	1

This scheme can be expanded so that an 8-bit byte translates to four symbols:

	MSB							LSB
Bits	7	6	5	4	3	2	1	0
Symbols	a		b		c		d	
	sent first						sent last	

With Forward Error Correcting (FEC)

This is more complicated, but essentially translates 3 binary bits to two 4-level symbols using an FEC coding scheme which lets the receiving modem detect and correct a large proportion of transmission errors.

Further details are given in the Operational Information section of this document.

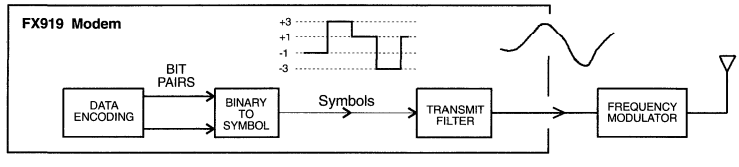


Fig.4 Transmit Signal Flow

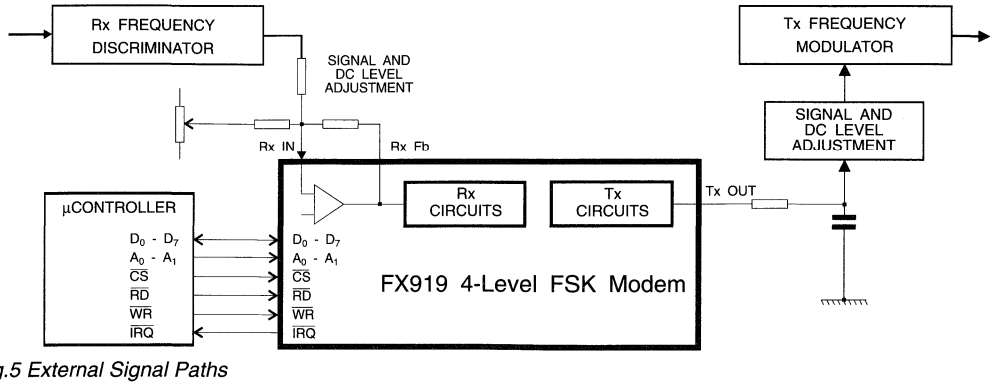


Fig.5 External Signal Paths

Application Information .....

AC Coupling

For a practical application, ac coupling from the modem's transmit output to the Frequency Modulator and from the receiver's Frequency Discriminator to the receive input of the modem may be desired. There are, however, two problems.

Firstly, ac coupling of the signal degrades the bit-error-rate performance of the modem.
Figure 6 illustrates the typical bit error rates at 4800 symbols/sec (without FEC) for differing degrees of a.c coupling;

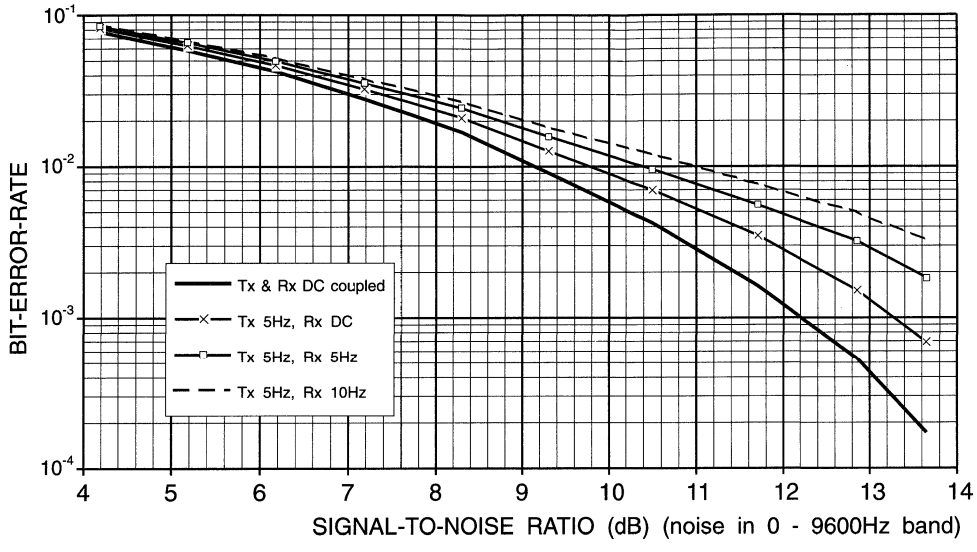


Fig.6 Examples of BER Performance Degradation Due to Varying Degrees of AC Coupling

Secondly, any ac coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits.
As illustrated below, the time for this voltage step to decay to 37% of its original value is:

Where f is the 3dB cut-off frequency of the ac coupling network; RC is 32msec (or 153 symbol-times at 4800symbols/sec) for a 20Hz network.

In general, it will be best to dc couple the receive discriminator to the modem, and to ensure that any ac coupling to the transmitter's frequency modulator has a -3dB cut-off frequency of no higher than 5Hz (for 4800symbols/sec).

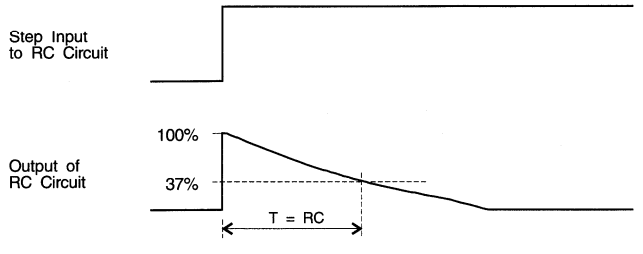


Fig.7 Decay Problems of the RC Network

Application Information .....

Radio Performance

The maximum data rate that can be transmitted over a radio channel using this modem depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Symbol rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracies.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 4800 symbols/sec can be achieved (subject to local regulatory requirements) over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ±2.5kHz peak for a repetitive +3 +3 -3 -3 pattern and the maximum difference between transmitter and receiver "carrier" frequencies is less than 2400Hz.

The modulation scheme employed by this modem is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. This does, however, place constraints on the performance of the radio.

In particular, attention must be paid to:

- Linearity, frequency and phase response of the Tx Frequency Modulator. For a 4800 symbol/sec system, the frequency response should be within ±2dB over a range 3Hz to 5Hz, relative to 2400Hz.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a dc offset at the discriminator output.

Viewing the received signal EYE (using the Mode Register RxEYE function) gives a good indication of the overall transmitter/receiver performance.

Rx Mode, RxEYE bit = '1'

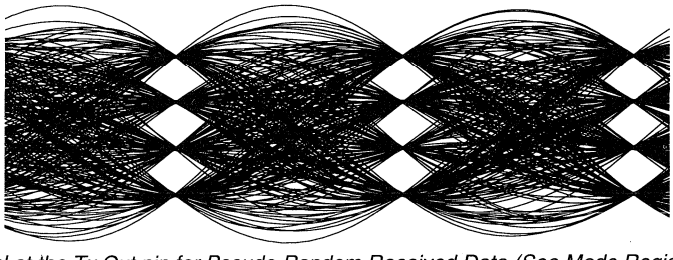


Fig.8 Rx Eye Signal at the Tx Out pin for Pseudo-Random Received Data (See Mode Register)

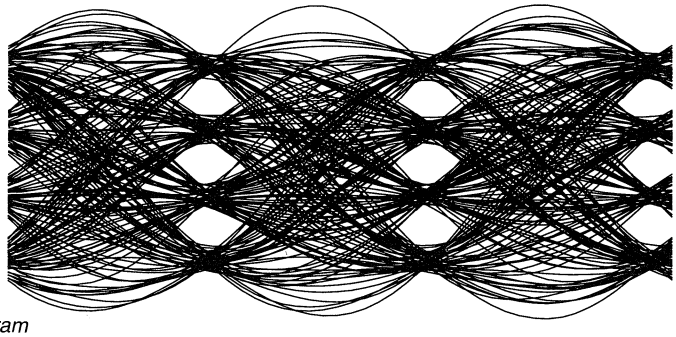


Fig.9 Tx Eye Diagram

Application Information .....

Baseband and RF Frequency Requirements

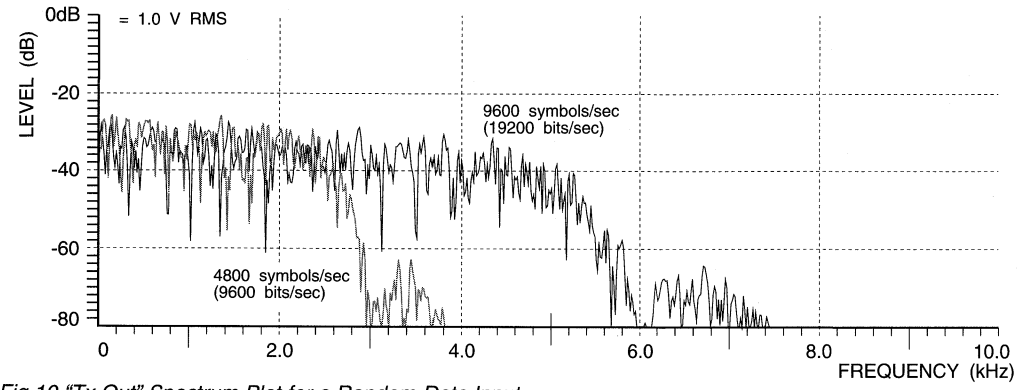


Fig.10 "Tx Out" Spectrum Plot for a Random Data Input

RF Channel Occupancy

The diagram below shows the theoretical RF bandwidth requirements when interfacing the FX919 baseband (Tx OUT) signal (Figure 10, above) to a radio transmitter. This plot assumes a perfect frequency modulator.

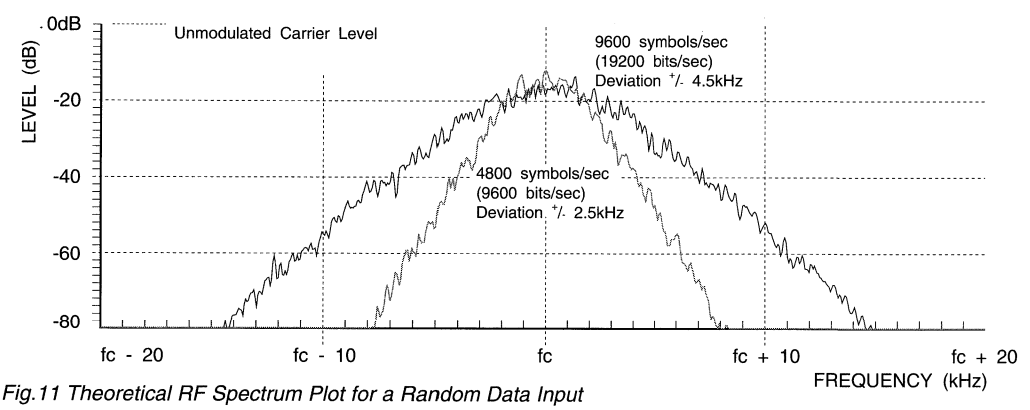
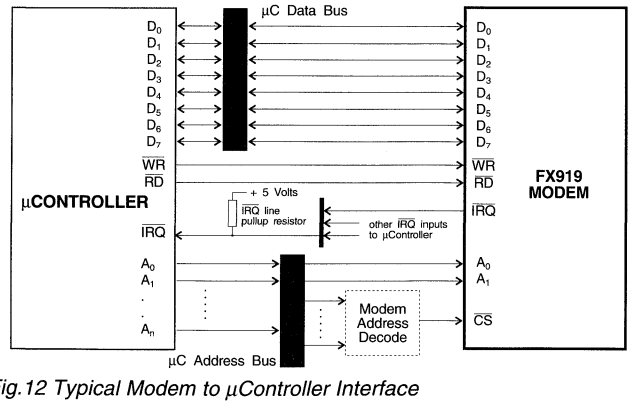


Fig.11 Theoretical RF Spectrum Plot for a Random Data Input

Note that particular repetitive data sequences, such as '+3 +3 -3 -3 +3 +3 ....' will produce spectra which are markedly different to those shown in Figures 10 and 11.



The Data Bus Buffers and Address and Read/Write Decode blocks form a byte-wide parallel µController interface.
This diagram shows how this function can be memory mapped.

Fig.12 Typical Modem to µController Interface

Programming Information

Data Formats

Frame and Data Structures

The FX919 Frame and data structures are illustrated in Figure 13 and consist of a Frame Preamble (comprising Symbol and Frame Synchronisation patterns) followed by one or more 'Header', 'Intermediate' or 'Last' blocks; the binary data transferred between the modem and the controlling µController is that shown in the shaded areas near the top of the diagram.

The 'Header' block is self-contained in that it includes its own CRC, and would normally carry information such as: The addresses of the called and calling parties. The number of following blocks in the frame (if any), and miscellaneous control information.

The 'Intermediate' block(s) contain only data, the CRC checksum for all of the data in the 'Intermediate' and 'Last' blocks being contained at the end of the 'Last' block.

This arrangement, whilst efficient in terms of data capacity, may not be optimum for poor signal-to-noise conditions, since a reception error in any one of the 'Intermediate' or 'Last' blocks would invalidate the whole frame. In these conditions, increased throughput may be obtained by using the 'Header' block format for all blocks of the frame, so that blocks which are received correctly can be identified, and need not be retransmitted.

Further information is given in the Operational Information section of this data sheet.

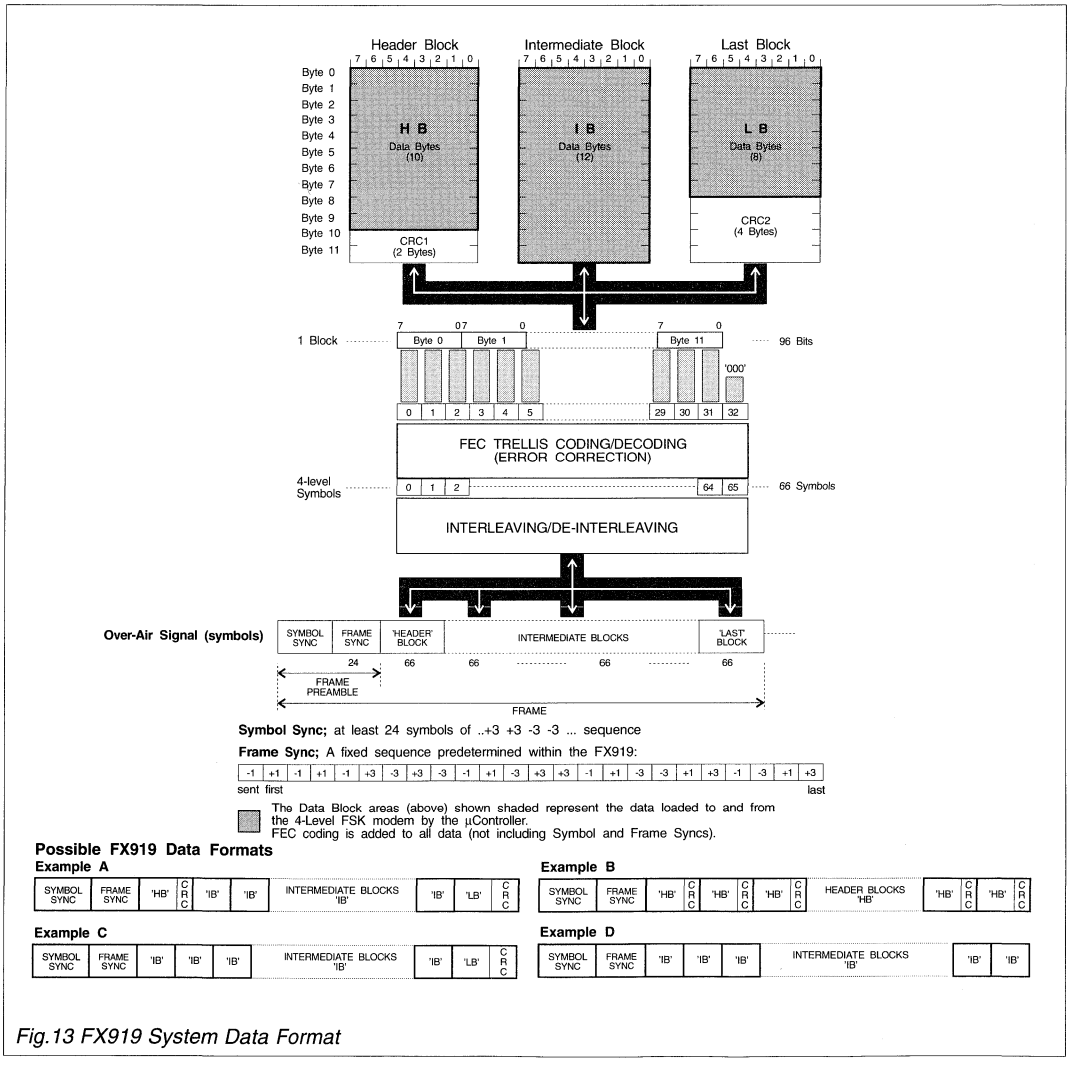


Fig.13 FX919 System Data Format

Programming Information .....

Modem/µController Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronisation pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (cyclic redundancy checksum) generation, Forward Error Correction coding and Interleaving. Details of the message format handled by this modem are shown in Figure 13.

To reduce the processing load on the associated µController, the FX919 has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting and de-formatting and - when in receive mode - in searching for and synchronising onto the Frame Preamble. In normal operation the modem will only require servicing by the µController once per received or transmitted block.

Thus, to transmit a block, the controlling µController has only to load the unformatted -'raw'- binary data into the modem's Data Block Buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result as 4-level symbols (with Forward Error Correction coding) and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary -using the FEC coding to correct as many errors as possible- and check the resulting CRC before placing the received binary data into the Data Block Buffer for the µController to read.

The FX919 can also handle the transmission and reception of unformatted data -to allow for example the transmission of Symbol and Frame Synchronisation sequences or special test patterns.

The Programmer's View

Register Selection

The FX919 modem appears to the programmer as 4 write-only 8-bit registers shadowed by 3 read-only registers. Individual registers are selected by the A_1 and A_0 inputs.

Table 1 Register Selection

A_1	A_0	Write to Modem	Read from Modem
0	0	Data Block Buffer	Data Block Buffer
0	1	Command Register	Status Register
1	0	Control Register	D Q Register
1	1	Mode Register	not used

Note that there is a minimum allowable time between accesses of the modem's registers. See Read and Write cycle timing diagrams.

Data Block Buffer

A 12-byte read/write buffer which is used to transfer data (as opposed to Command, Status, Mode, Data-Quality and Control information) between the modem and the controlling µController.

The Data Block Buffer appears to the µController as a single 8-bit register; the modem ensures that sequential µController 'read' or 'write' actions to the buffer are routed to the correct locations within this buffer.

When the modem is in the Tx mode, any attempt by the µController to 'read' from this buffer will have no effect. Similarly, any attempt to 'write' to this buffer will have no effect when the modem is in the Rx mode.

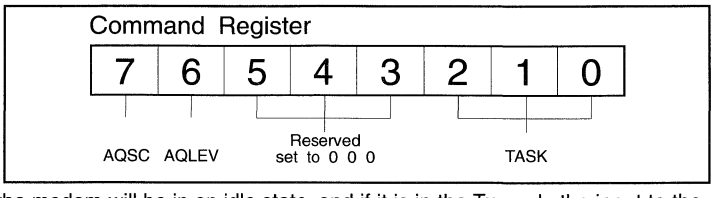
Note that when in Rx mode the modem will function correctly even if the received data is not read from the Data Block Buffer by the µController.

The µController should only access this buffer when the Status Register BFREE bit is '1'.

Command Register

Writing to this register instructs the modem to perform a specific action or actions, depending upon the setting of the TASK, AQLEV, and AQSC bits.

Fig.14 The Command Register



When it has no action to perform, the modem will be in an idle state, and if it is in the Tx mode the input to the Tx Filter will be connected to a voltage mid-way between the '+1' and '-1' symbol voltages.

In the Rx mode the modem will continue to measure the received data quality and extract symbols from the received signal, feeding them into the De-Interleave Buffer, but will otherwise ignore the received data.

Command Register

B7 **AQSC**	**Acquire Symbol Clock:** This bit has no effect in the Tx mode. In the Rx mode, whenever a byte with the AQSC bit set to logic '1' is written to the Command Register, it initiates an automatic sequence designed to achieve timing synchronisation with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received symbol-timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronisation is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register. Setting this bit to logic '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be restarted every time that a byte written to the Command Register has the AQSC bit set to logic '1'. The AQSC bit will normally be set at the same time as a SFS (Search for Frame Sync) or SFSH (Search for Frame Sync + Header) task, however it may also be used independently to re-establish clock synchronisation quickly after a long fade. Alternatively, an SFS or SFSH task may be written to the Command Register with the AQSC bit at logic '0' if it is known that clock synchronisation does not need to be re-established.
B6 **AQLEV**	**Acquire Receive Signal Levels:** This bit has no effect in the Tx mode. In receive mode, whenever a byte with the AQLEV bit set to a logic '1' is written to the Command Register, it initiates an automatic sequence designed to measure the amplitude and dc offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time -hence improving the measurement accuracy- until the 'normal' value set by the LEVRES bits of the Control Register is reached. Setting this bit to a logic '0' (or changing it from '1' to '0') has no effect; note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQLEV bit set to a logic '1'. The AQLEV bit will normally be set at the same time as an SFS (Search for Frame Sync) or SFSH (Search for Frame Sync + Head) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, a SFS or SFSH task may be written to the Command Register with the AQLEV bit at logic '0' if it is known that there is no need to re-establish the received signal levels.
B5 **B4** **B3**	These bits should each be set to a logic '0'.
B2 **B1** **B0** **TASK**	**Task:** Operations such as transmitting a data block are treated by the modem as 'Tasks'. Information on Task functions is given on the following pages. A task is initiated when the µController writes a byte to the Command Register with the Task bits set to anything other than the 'NULL' code. The µController should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is a logic '0'. Different tasks apply in receive and transmit modes. **Tx Mode:** All tasks other than NULL, RESET instruct the modem to transmit data from the Data Block Buffer, formatting it as required. For these tasks the µController should wait until the BFREE (Buffer Free) bit of the Status Register is a logic '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number '0' of the block should be written first. Once the byte containing the desired task has been written to the Command Register, the modem will: Set the BFREE (Buffer Free) bit of the Status Register to a logic '0', take the data from the Data Buffer as quickly as it can -transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Programming Information .....

Command Register

B2 **B1** **B0** **TASK**	**Task: .....** Once all of the data has been transferred from the Data Block Buffer the modem will set the BFREE and IRQ bits of the Status Register to a logic '1', (causing the interrupt output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the µController that it may write new data and the next task to the modem. In this way the µController can write a task -and the associated data- to the modem while the modem is still transmitting the data from the previous task. **Rx Mode:** The µController should wait until the BFREE bit of the Status Register is a logic '1', then write the desired task to the Command Register. Once the byte containing the desired task has been written to the Command Register, the modem will: Set the BFREE bit of the Status Register to a logic '0'. Wait until enough received bits are in the De-Interleave Buffer. Decode them as needed, and transfer any resulting data to the Data Block Buffer. Then the modem will set the BFREE and IRQ bits of the Status Register to logic '1', (causing the interrupt output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the µController that it may read from the Data Buffer and write the next task to the modem. In this way the µController can read data and write a new task to the modem while the received symbols needed for this new task are being stored in the De-Interleave Buffer.

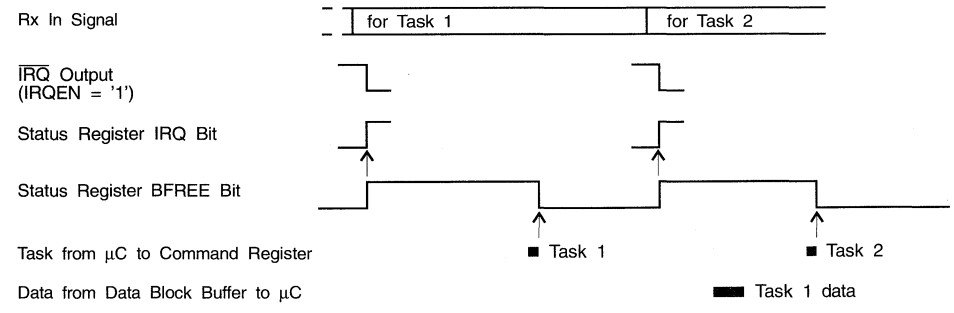


Fig.15 The Receive Process

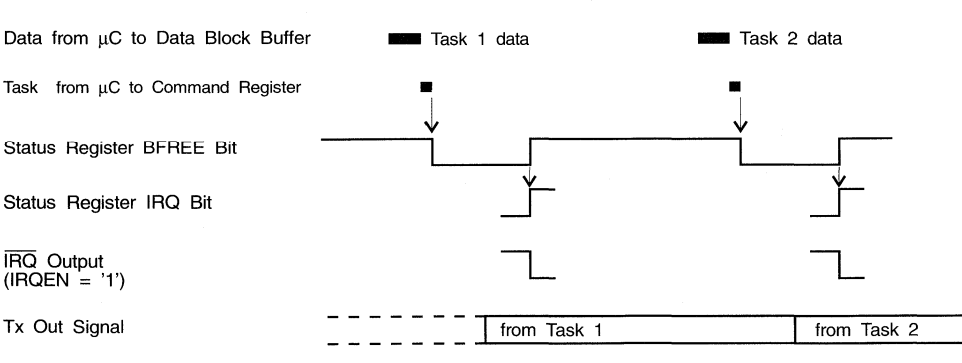


Fig.16 The Transmit Process

Modem Tasks in Detail

The following describes the setting and format of the Command Register 'task' bits (bits 2, 1 and 0). Note that before a task is programmed the Tx/Rx bit in the Mode Register must be placed in the relevant position.

Command Bits						
2	1	0		Receive Mode		Transmit Mode
0	0	0	NULL	.. ..	NULL	.. ..
0	0	1	SFSH	Search for Frame Sync + Header	T24S	Transmit 24 Symbols
0	1	0	RHB	Read Header Block	THB	Transmit Header Block
0	1	1	RILB	Read Intermediate or Last Block	TIB	Transmit Intermediate Block
1	0	0	SFS	Search for Frame Sync	TLB	Transmit Last Block
1	0	1	R4S	Read 4 Symbols	T4S	Transmit 4 Symbols
1	1	0	NULL	.. ..	NULL	.. ..
1	1	1	RESET	Cancel any Current Action	RESET	Cancel any Current Action

Table 2 Modem Task Details

Modem Tasks

NULL

No Effect. This task is provided so that an AQSC or AQLEV (Command Register) command can be initiated without loading a new task.

SFSH

Search for Frame Sync + Header Block. Causes the modem to search the received signal for a valid 24-symbol Frame Sync sequence followed by a Header Block which has a correct CRC1 checksum.
This task continues until a valid Frame Sync + Header Block has been found.
The search consists of two stages:

1. The modem will attempt to match the incoming symbols against the General Purpose Modem Frame Synchronisation pattern to within the tolerance defined by the Frame Sync Tolerance (FSTOL) bits of the Control Register.
2. Once a match has been found, the modem will read-in the next 66 symbols as if they were a 'Header' block, decoding the symbols and checking the CRC1 checksum. If the CRC1 checksum is incorrect the modem will resume the search, looking for a fresh Frame Sync pattern.
   If the CRC1 is correct, the 10 decoded data bytes will be placed into the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1' and the CRC Checksum Error (CRCERR) bit cleared low to a logic '0'.

On detecting the BFREE bit of the Status Register has gone to a logic '0', the µController should read the 10 bytes from the Data Block Buffer and then write the next task to the modem's Command Register.

RHB

Read Header Block. Causes the FX919 to read the next 66 symbols as a 'Header' block, decoding them, placing the resulting 10 data bytes and the 2 received CRC bytes into the Data Block Buffer, and setting the BFREE and IRQ bits of the Status Register high to a logic '1' when the task is complete to indicate that the µController may read the data from the Data Block Buffer and write the next task to the modem's Command Register.
The CRCERR bit of the Status Register will be set to a logic '1' or '0' depending on the validity of the received CRC1 checksum bytes.

RILB

Read 'Intermediate' or 'Last' Block. Causes the modem to read the next 66 symbols as an 'Intermediate' or 'Last' block (the µController should be able to tell from the received 'Header' block how many blocks are in the frame, and hence when to receive the 'Last' block).
In each case, the modem will decode the 66 symbols and place the resulting 12 bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register high to a logic '1' when the task is complete to indicate that the µController may read the data from the Data Block Buffer and write the next task to the modem's Command Register. If an 'Intermediate' Block is received then the µController should read-out all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µController need only read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum. Note that in the Rx mode the CRC2 checksum circuits are initialised on completion of any task other than NULL or RILB.

Modem Tasks .....

SFS

Search for Frame Sync. Causes the modem to search the received signal for a 24-symbol sequence which matches the Frame Synchronisation pattern to within the tolerance defined by the FSTOL bits of the Mode Register.
When a match is found the modem will set the BFREE and IRQ bits of the Status Register high to a logic '1' to indicate to the µController that it should write the next task to the Command Register.

R4S

Read 4 Symbols. This task is intended for special tests and channel monitoring -perhaps preceded by an SFS task.
Causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set high to a logic '1' to indicate that the µController may read the data byte from the Data Block Buffer and write the next task to the Command Register.

T24S

Transmit 24 Symbols. This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC, FEC or interleaving.
Byte '0' of the Data Block Buffer is sent first, byte '5' last.
Once the modem has read all the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the µController that it may write the next task and its data to the modem.
The tables prepared below show what data has to be written to the Data Block Buffer to transmit the modem Symbol and Frame Sync Sequences:

'Symbol Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
+3	+3	-3	-3	Byte 0 :	11110101	F5
+3	+3	-3	-3	Byte 1 :	11110101	F5
+3	+3	-3	-3	Byte 2 :	11110101	F5
+3	+3	-3	-3	Byte 3 :	11110101	F5
+3	+3	-3	-3	Byte 4 :	11110101	F5
+3	+3	-3	-3	Byte 5 :	11110101	F5

'Frame Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
-1	+1	-1	+1	Byte 0 :	00100010	22
-1	+3	-3	+3	Byte 1 :	00110111	37
-3	-1	+1	-3	Byte 2 :	01001001	49
+3	+3	-1	+1	Byte 3 :	11110010	F2
-3	-3	+1	+3	Byte 4 :	01011011	5B
-1	-3	+1	+3	Byte 5 :	00011011	1B

THB

Transmit Header Block. Takes 10 bytes of data (Address & Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Header' Block.
Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

TIB

Transmit Intermediate Block. Takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Intermediate' Block. Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the µController that it may write the next task and its data to the modem.
Note that in Tx mode the CRC2 checksum circuits are initialised on completion of any task other than NULL, TIB or TLB.

Modem Tasks	
TLB	**Transmit 'Last' Block.** Takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12-bytes to 4-level symbols with (FEC), interleaves the symbols and transmits the result as a formatted 'Last' Block. Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the µController that it may write the next task and its data to the modem.
T4S	**Transmit 4 Symbols.** This task is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.
RESET	**RESET.** Stop any current action. This 'task' takes effect immediately, and terminates any current action (task , AQSC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register high to a logic '1', without setting the IRQ bit. RESET should be used to set the modem into a known state when V_{DD} is applied. *Note that due to delays in the transmit filter, it will take several symbol-times for any change to become apparent at the TxOp pin.*

RRC Filter Delay

The Task Timing figures detailed in Table 3 are based upon: the signal at the input to the RRC Filter in the transmit mode, or the signal at the input to the de-interleave circuits in the receive mode. As can be seen from the diagram in Figure 17, there is an additional delay of approximately 8 (eight) symbol-times in both Tx and Rx modes due to the (Tx/Rx) RRC Filter.

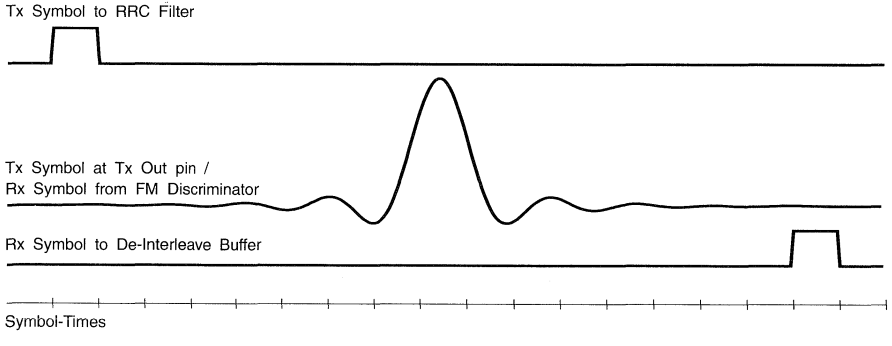


Fig.17 Examples of Filter Delay Times

Transmit and Receive Task Timing

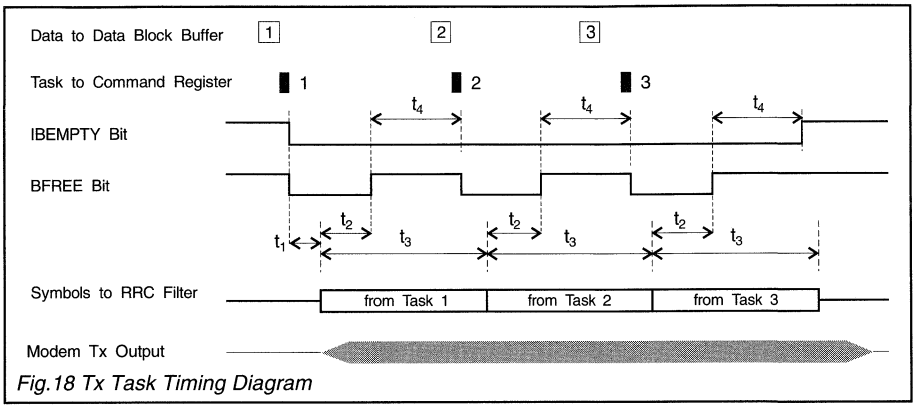


Fig.18 Tx Task Timing Diagram

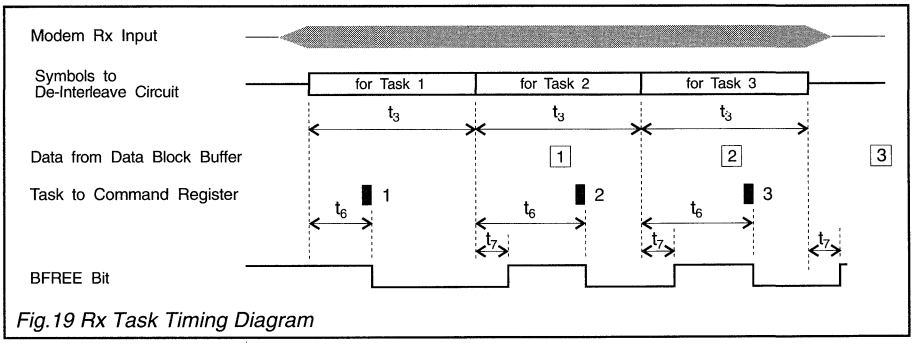


Fig.19 Rx Task Timing Diagram

Timing	Notes	Task	Time (symbol-times)
t_1	Modem in idle state. Time from writing first task to the application of the first Tx symbol to the RRC Filter.	Any	1 to 2
t_2	Time from the application of the first symbol of the task to the RRC Filter until BFREE goes to a logic '1' (high).	T24S THB/TIB/TLB T4S	5 16 0
t_3	Time to transmit all symbols of the task. or Time to receive all symbols of the task	T24S THB/TIB/TLB RHB/RILB T4S SFS SFSH R4S	24 66 66 4 24 (Min.) 90 (Min.) 4
t_4	Maximum time allowed from BFREE going to a logic '1' for the next task (and data) to be written to the modem.	T24S THB/TIB/TLB T4S	18 49 3
t_6	Maximum time between the first symbol of the task entering the de-interleave circuit and the task being written to the modem.	SFSH RHB/RILB SFS R4S	21 49 21 3
t_7	Time from last symbol of task entering the de-interleave circuit to BFREE going to a logic '1'.	Any	1

Table 3 Typical Rx/Tx Task Load Timings

Programming Information .....

Control Register

This 8-bit write-only register controls the modem's symbol-rate, the response times of the receive clock extraction and signal level measurement circuits and the Frame Sync pattern recognition tolerance.

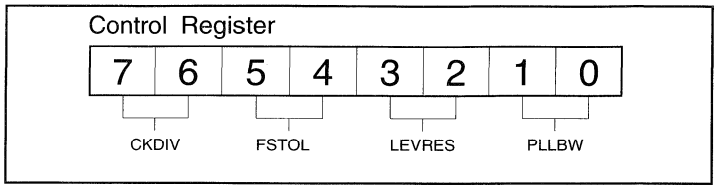


Fig.20 The Control Register

Control Register

Table 4 shows how bit-rates of 2400/4800/9600 symbols per second may be obtained from common Xtal/clock frequencies.

B7, B6 CKDIV

Clock Division Ratio: These bits control a frequency divider driven from the clock signal present at the Xtal pin; this ratio and Xtal input will determine the nominal symbol-rate.

			Xtal Frequency (MHz)		
			2.4576	4.9152	9.8304
		Division Ratio Xtal Freq. / Symbol Rate	Symbol Rate (symbols/sec.)		
B7	B6				
0	0	512	4,800	9,600	
0	1	1,024	2,400	4,800	9,600
1	0	2,048		2,400	4,800
1	1	4,096			2,400

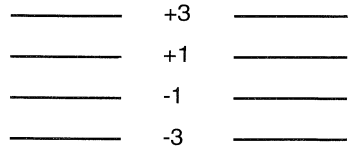
Table 4 Clock/Data Rates ***Note*** *that device operation is not guaranteed or specified above 9,600symbols/s or below 2,400symbols/s*

B5, B4 FSTOL

Frame Sync Tolerance: For use in the Rx mode only; these bits have no effect in the Tx mode. These bits define the maximum number of mismatches which will be allowed during a search for the Frame Sync pattern:

B5	B4	Mismatches Allowed
0	0	0
0	1	2
1	0	4
1	1	6

Note that a single 'mismatch' is defined as the difference between two adjacent symbol levels; if the symbol '+1' were expected, then the received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2.



Symbol Levels

Control Register .....

B3, B2
LEVRES

Level Measurement Modes: These bits are only used in the Rx mode and have no effect in the Tx mode; they set the 'normal' operating mode of the Rx signal amplitude and dc offset measuring circuits. This setting will be temporarily overridden by the automatic sequencing of an AQLEV command.

For most applications these two bits should be set to 'Slow Peak Detect' mode, in which the peak positive and peak negative excursions of the received signal (after filtering) are measured to establish the amplitude and dc offset of the signal. The decay time-constant of the peak rectifier circuits used in this mode is approximately 1000 symbol-times.

The 'Hold' setting freezes the stored values of the current amplitude and offset measurements and may therefore be used to improve performance during short fades or for while the radio is switched from Rx mode for the transmission of a short acknowledgement. It should be noted, however, that the measured amplitude and offset values are stored on the external "Doc" capacitors and will decay gradually when the 'Hold' setting is chosen, the discharge-time constant being approximately 1000 symbol-times.

The 'Lossy Peak Detect' setting is similar to 'Slow Peak Detect' except that the decay time-constants of the peak detectors are reduced to approximately 75 symbol-times to give a faster response to signal changes at the expense of BER performance. This mode is used by the automatic level measurement acquisition sequence but may also be useful in non-standard systems.

The 'Clamp' setting is primarily intended for use by the automatic level measurement acquisition sequence, but may also be useful in non-standard systems. In this mode the Doc 1 and Doc 2 pins are connected directly to the output of the circuit that normally drives the peak detectors.

B1, B0
PLLBW

B3	B2	Setting
0	0	Hold
0	1	Slow Peak Detect
1	0	Lossy Peak Detect
1	1	Clamp

Table 5

PLL BW; Phase-Locked Loop Modes: For use in the Rx mode only (no effect in Tx).
In the receive mode these two bits set the 'normal' bandwidth of the Rx Clock Extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the automatic sequence of an AQSC command.

B1	B0	PLL Mode	Working Bandwidth (± ppm)
0	0	Hold	0
0	1	Narrow Bandwidth	20
1	0	Medium Bandwidth	100
1	1	Wide Bandwidth	650

Note: 'Working Bandwidths' are the maximum difference between the actual received symbol rate and the nominal rate determined by the tolerance of the modem's Xtal frequency, to give minimal degradation of a reasonably random received signal.

Table 6

The minimum bandwidth consistent with the transmit and receive modem symbol rate tolerances should be chosen, i.e. if the Xtals used with both modems have accuracies of within ±50ppm, then the PLLBW bits should be set to '1' '0' (Medium Bandwidth).
The 'Wide Bandwidth' setting is intended for message acquisition in systems where the µController cannot detect the start of the received message, as it allows the modem to respond rapidly to fresh messages and recover rapidly after a fade without µController intervention - although at the cost of reduced Bit Error Rate vs Signal to Noise performance.
The 'Hold' setting disables the PLL feedback loop, and may be used during signal fades.

The 'Narrow' setting should preferably not be applied until about 200 symbols after an AQSC, to allow time for the PLL to settle.

Programming Information .....

Mode Register

This 8-bit write-only register controls the basic operating modes of the modem.

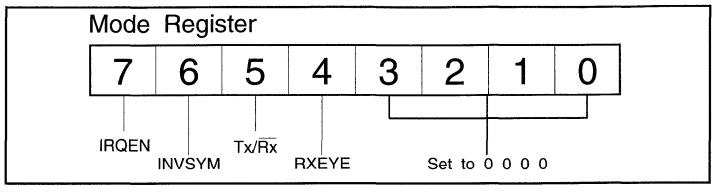


Fig.21 The Mode Register

Mode Register	
B7 IRQEN	**IRQ Output Enable:** When set to a logic '1' the Interrupt Request output is pulled low (to V_{SS}) whenever the IRQ bit (BIT 7) of the Status Register is set by the modem to a logic '1'. When set to a logic '0' the Interrupt Request output will not function and will remain in its high-impedance state (see Pin Functions and Figure 12 - µController Interface).
B6 INVSYM	**Invert Symbols:** Controls the polarity (sense) inversion of transmitted and received symbol voltages.

B6	Symbol	Signal at Tx Out	Signal at Rx Fb
'0'	'+3'	above V_{BIAS}	below V_{BIAS}
'0'	'-3'	below V_{BIAS}	above V_{BIAS}
'1'	'+3'	below V_{BIAS}	above V_{BIAS}
'1'	'-3'	above V_{BIAS}	below V_{BIAS}

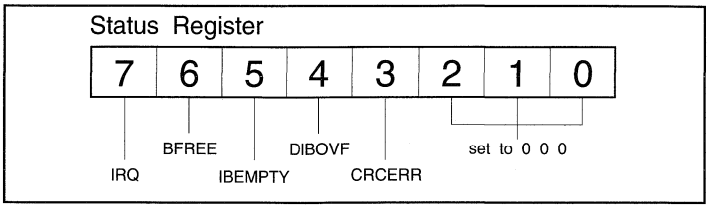
B5 Tx/Rx	**Tx/$\overline{Rx}$ Mode:** When set to a logic '1' places the modem in the Transmit mode; when set to a logic '0' places the modem in the Receive mode. Note that changing between Transmit and Receive modes will cancel any current task.
B4 RxEYE	**Show Rx Eye:** This bit should be set to a logic '0' for normal Rx operation and always for Tx operation. Setting this bit to a logic '1' in the receive mode configures the modem into a special test mode, in which the input to the Tx Output Buffer is connected to the Rx Symbol/Clock Extraction circuit at a point which carries the equalised receive signal. This may be monitored with an oscilloscope (at the Tx Out pin *before* the external RC filter), to assess the quality of the complete radio channel including the Tx and Rx modem filters, the Tx modulator and the Rx IF filters and FM demodulator. The resulting 'eye' diagram (for reasonably random data) should ideally be as shown in Figure 8, with 4 'crisp' and equally spaced crossings.
B3 B2 B1 B0	These bits should always be set to a logic '0'.

Programming Information .....

Status Register

This register may be read by the µController to determine the current state of the modem.

Fig.22 The Status Register



Status Register

B7 IRQ

Interrupt Request: This bit is set to a logic '1' by:

The Status Register BFREE bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's Tx/Rx bit.

or

The Status Register IBEMPTY bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's Tx/Rx bit.

or

The Status Register DIBOVF bit going from a logic '0' to '1'.

This (IRQ) bit is cleared to a logic '0' immediately after a read of the Status Register.
If the IRQEN bit of the Mode Register is a logic '1', the FX919 $\overline{IRQ}$ output pin will be pulled low (to V_{SS}) whenever the Status Register IRQ bit is a logic '1'.

B6 BFREE

Data Block Buffer Free: BFREE reflects the availability of the Data Block Buffer; BFREE is cleared to a logic '0' *(Buffer NOT Free)* whenever a task other than NULL or RESET is written to the Command Register.
In Transmit mode, the BFREE bit will be set to a logic '1' (also setting the Status Register IRQ bit to a logic '1) when the modem is ready for the µController to write new data to the Data Block Buffer and the next task to the Command Register.
In Receive mode, the BFREE bit is set to a logic '1' (also setting the Status Register IRQ bit to a logic '1) by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The µController may then read that data and write the next task to the Command Register.
The BFREE bit is also set to a logic '1' (but without setting the IRQ bit) by a RESET task or when the Mode Register's Tx/Rx bit is changed.

B5 IBEMPTY

Interleave Buffer Empty: In Transmit mode, IBEMPTY is set to a logic '1' (also setting the IRQ bit) when less than two symbols remain in the Interleave Buffer or the Interleave Buffer is empty. Any transmit task written to the modem after IBEMPTY goes to a logic '1' will be too late to avoid a gap in the transmit output signal (see Figure 18 and Table 3, Tx Task Timing)
IBEMPTY is also set to a logic '1' by a RESET task and by a change of the Mode Register's Tx/Rx bit, but in this cases the IRQ bit will not be set.
IBEMPTY is cleared to a logic '0' within 1-symbol time after a task other than NULL or RESET is written to the Command Register.
Note that when the modem is in the transmit mode and the Interleave Buffer is empty, a mid-level (half-way between '+1' and '-1') will be fed to the RRC Filter.
In Receive mode this bit is a logic '0'.

Programming Information .....

Status Register	
B4 DIBOVF	**De-Interleave Buffer Overflow: In Receive mode** DIBOVF is set to a logic '1' (also setting the IRQ bit) when an RHB, RILB, RSID or R4S task is written to the Command Register too late to allow continuous reception (see Figure 19 and Table 3 Rx Task Timing). DIBVOF is cleared to a logic '0' by reading the Status Register, by writing a RESET task to the Command Register or by changing the Tx/Rx bit of the Mode Register. **In Transmit mode** this bit is a logic '0'.
B3 CRCERR	**CRC Checksum Error: In Receive mode** CRCFEC will be updated at the end of an SFSH, RHB, or RILB task to reflect the result of the receive CRC check. A logic '0' indicates that the CRC was received correctly. A logic '1' indicates that an error is present. Note that this bit should be ignored when an 'Intermediate' Block (which does not have an integral CRC) is received. CRCERR is cleared to a logic '0' by a RESET task, or by changing the Tx/Rx bit of the Mode Register. **In Transmit mode** this bit is a logic '0'.
B2, B1, B0	These bits will always be '0'.

The Data Quality Register

In Receive mode, the modem continuously measures the quality of the received signal by comparing the actual received waveform over the previous 64 symbol times against an internally generated "ideal". The result is placed into bits 3 to 7 of the Data Quality Register for the µController to read at any time, bits 0 to 2 being always set to '0'. Figure 23 shows how the value (0 to 255) read from the Data Quality Register varies with the received signal-to-noise ratio.

In Transmit mode, and for 64 symbol-times after enabling Receive mode, the value will be invalid.

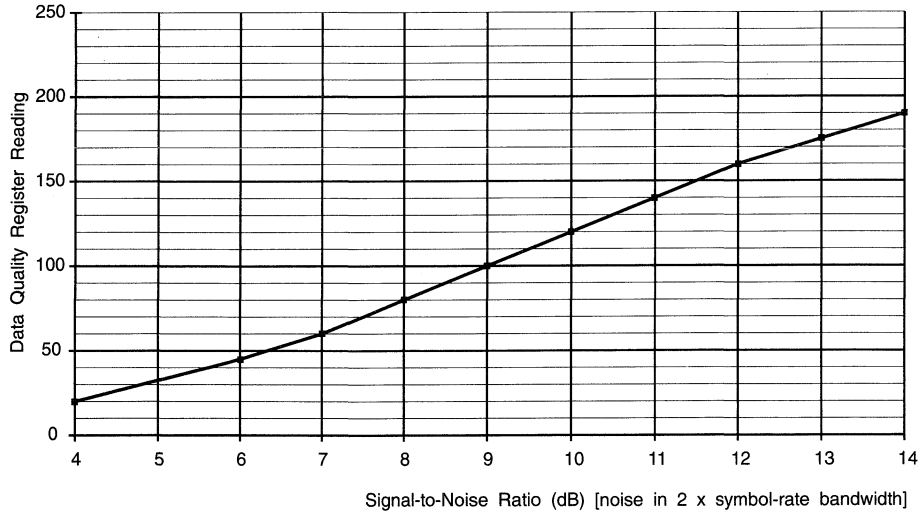


Fig.23 Typical Data Quality Reading vs Rx Signal-to-Noise Ratio

Programming Information .....

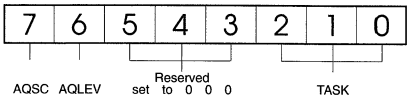
Registers

This diagram may provide a useful quick-reference to FX919 register allocations.

Register Selection

Write to Modem	A_1	A_0	Read from Modem
Data Block Buffer	0	0	Data Block Buffer
Command Register	0	1	Status Register
Control Register	1	0	DQ Register
Mode Register	1	1	not used

Command Register

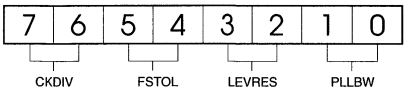


AQSC - Acquire Symbol Clock
AQLEV - Acquire Receive Signal Levels
TASK:

B2	B1	B0	Rx Mode	
0	0	0	NULL	
0	0	1	SFSH	Search For Frame Sync + Head
0	1	0	RHB	Read Header Block
0	1	1	RILB	Read Intermediate or Last Block
1	0	0	SFS	Search For Frame Sync
1	0	1	R4S	Read 4 Symbols
1	1	0	NULL	
1	1	1	RESET	Cancel any Current Action

B2	B1	B0	Tx Mode	
0	0	0	NULL	
0	0	1	T24S	Transmit 24 Symbols
0	1	0	THB	Transmit Header Block
0	1	1	TIB	Transmit Intermediate Block
1	0	0	TLB	Transmit Last Block
1	0	1	T4S	Transmit 4 Symbols
1	1	0	NULL	
1	1	1	RESET	Cancel any Current Action

Control Register



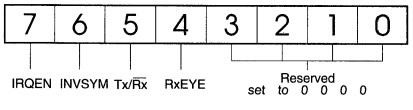
CKDIV - Clock Division Ratio
FSTOL - Frame Sync Tolerance
LEVRES - Level Measurement Response Time

B3	B2	
0	0	Hold
0	1	Slow Peak Detect
1	0	Lossy Peak Detect
1	1	Clamp

PLLBW - PLL Bandwidth

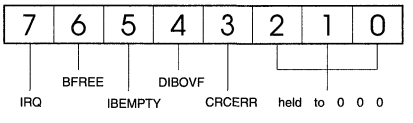
B1	B0	Bandwidth	+/-ppm
0	0	Hold	0
0	1	Narrow	20
1	0	Medium	100
1	1	Wide	650

Mode Register



IRQEN - IRQ Output Enable
INVSYM - Invert Symbol
Tx/Rx - Transmit or Receive Mode
RxEYE - Show Rx Eye

Status Register



IRQ - Interrupt Request
BFREE - Data Block Buffer Free
IBEMPTY - Interleave Buffer Empty
DIBOVF - De-Interleave Buffer Overflow
CRCERR - CRC Checksum Error

Fig.24 Ready-Use Guide to Register Functions

Operational Information

"Transmit Frame" Example

The operations needed to transmit a single Frame consisting of Symbol and Frame Sync sequences and one each Header, Intermediate and Last blocks are shown below.

Sequence Explanation	
Prerequisites: Ensure that the Control Register has been loaded with a suitable CKDIV value, and that the IRQEN and Tx/Rx bits of the Mode Register are '1', the RxEYE bit is '0' and the INVSYM bit is set appropriately-	
Steps	
1 Read Status Register to ensure BFREE = '1'	BFREE = '1'
2 Write 6 Symbol Sync bytes to the Data Block Buffer - and a Transmit 24 Symbols task to the Command Register -	Write to Data Block Buffer T24S
3 Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ BFREE = '1' IRQ = '1'
4 Write 6 Frame Sync bytes to the Data Block Buffer - and a Transmit 24 Symbols task to the Command Register -	Write to Data Block Buffer T24S
5 Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ BFREE = '1' IRQ = '1'
6 Write 10 Header Block bytes to the Data Block Buffer - and Transmit Header Block task to the Command Register -	Write to Data Block Buffer THB
7 Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ BFREE = '1' IRQ = '1'
8 Write 12 Intermediate Block bytes to the Data Block Buffer - and a Transmit Intermediate Block task to the Command Register -	Write to Data Block Buffer TIB
9 Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ BFREE = '1' IRQ = '1'
10 Write 8 Last Block bytes to the Data Block Buffer - and a Transmit Last Block task to the Command Register -	Write to Data Block Buffer TLB
11 Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ BFREE = '1' IRQ = '1'
12 Wait for another Interrupt - Read Status Register, check that the IRQ, BFREE and IBEMPTY bits are '1' -	IRQ BFREE = '1' IRQ = '1' IBEMPTY = '1"
Note that the final symbol of the frame will start to appear at the Tx OUT pin approximately 2 symbol-times after the Status Register IBEMPTY bit goes to a '1'; a further 16 symbol-times should be allowed for the symbol to pass completely through the RRC Filter.	

Note that this example uses only the minimum 24-symbol "Symbol Synchronisation" pattern. Overall system performance may be improved by increasing this to 48 symbols (by repeating steps 2 and 3).

Operational Information .....

"Receive Frame" Example

The operations needed to receive a single frame consisting of Symbol and Frame Sync sequences and one each Header, Intermediate and Last blocks are shown below.

Sequence Explanation	
Prerequisites: Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values, that the Mode Register IRQEN bit is '1' and the RxEYE and Tx/Rx bits are '0', and that the INVSYM bit is set appropriately. Wait until the received carrier has been present for at least 8 symbol-times.	
Steps	
1 Read Status Register, check that the IRQ and BFREE bits are '1'. -	IRQ = '1' BFREE = '1'
2 Write a byte containing an SFSH task and with the AQSC and AQLEV bits set to '1' to the Command Register -	SFSH task AQSC and AQLEV = '1'
3 Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ IRQ = '1' BFREE = '1'
4 Check that the Status Register CRCERR bit was '0' Read 10 Header Block bytes from the Data Block Buffer -	CRCERR '0' Read from Data Block Buffer
5 Write a Read Intermediate or Last Block task to the Command Register -	RILB
6 Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ IRQ = '1' BFREE = '1'
7 Read 12 Intermediate Block bytes from the Data Block Buffer - (The state of the Status Register CRCERR bit should be ignored as this is an intermediate block)	Read from Data Block Buffer
8 Write a Read Intermediate or Last Block task to the Command Register -	RILB
9 Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1'. -	IRQ IRQ = '1' BFREE = '1'
10 Check the CRCERR bit of the Status Register is '0' - and read the 8 Last Block bytes from the Data Block Buffer -	CRCERR = '0' Read from Data Block Buffer

Forward Error Correction

Transmit Mode, the FX919 uses a Trellis Encoder to translate the 96 bits (12 bytes) of a Header, Intermediate or Last Block into a 66-symbol sequence which includes Forward Error Correction information.

Receive Mode, the FX919 decodes the received 66-symbol block into 12 bytes of binary data using a Viterbi algorithm to take advanyage of the encoded FEC information

Cyclic Redundancy Codes

CRC1

This is a sixteen-bit cyclic redundancy checksum which uses the generator polynomial: $X^{16} + X^{12} + X^5 + 1$

CRC2

This is a 32-bit cyclic redundancy checksum which uses the generator polynomial:

$$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$$

Interleaving

The 66 symbols of a 'Header', 'Intermediate' or 'Last' block are interleaved by the modem before transmission to give protection against noise bursts and short fades.

In the receive mode, the modem de-interleaves the received symbols prior to decoding.

Level Measurement and Clock Extraction

The FX919 is intended for use in systems where the Symbol Sync pattern is transmitted immediately on startup of the transmitter.

When the carrier is detected by the receiver or when the receiver is switched to another channel, the controlling µController should wait approximately 8 symbol-times for the received signal to propagate through the modem's RRC filter then issue a SFS or SFSH task with the AQSC and AQLEV bits set to '1'.

The 8-symbol delay can usefully be included in the carrier detect circuitry.

Setting the AQSC and AQLEV bits to '1' triggers the modem's automatic Symbol Clock Extraction and Level Measurement acquisition sequences, which are designed to measure the received symbol timing, amplitude and dc offset as quickly as possible during the Symbol Sync period before switching to more accurate - but slower - measurement modes for the remainder of the received message. Note that if the acquisition sequences are triggered after the Symbol Sync period - as can happen when the receiver is switched to another channel- they will still function correctly, but will take longer to acquire accurate level and timing information.

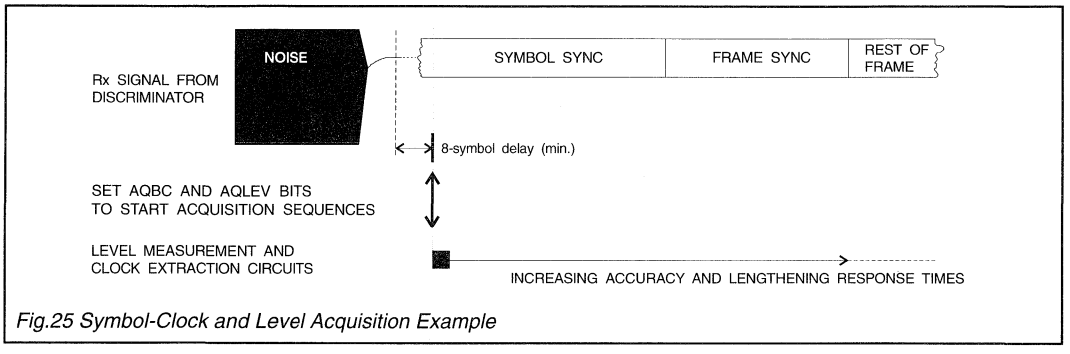


Fig.25 Symbol-Clock and Level Acquisition Example

The operation of the Level Acquisition Sequence depends on the settings of the Control Register LEVRES bits:

LEVRES Setting ---	B3	B2	Details of Level Acquisition Sequence
'Hold'	0	0	1 symbol-time of 'Clamp' mode then 15 symbol-times of 'Lossy Peak Detect' mode before reverting to 'Hold' mode
'Slow Peak Detect'	0	1	1 symbol-time of 'Clamp' mode then 15 symbol-times of 'Lossy Peak Detect' mode before reverting to 'Slow Peak Detect' mode
'Lossy Peak Detect'	1	0	1 symbol-time of 'Clamp' mode before reverting to 'Lossy Peak Detect' mode
'Clamp'	1	1	Remain in 'Clamp' mode

The 1-symbol 'Clamp' time at the start of these sequences is used to make an initial measurement of the dc offset present on the received signal, after which the 'Lossy Peak Detect' period is used to estimate the signal amplitude.

The operation of the Symbol Clock Acquisition Sequence depends on the settings of the Control Register PLLBW bits:

PLLBW Setting ---	B1	B0	Details of Symbol Clock Acquisition Sequence
'Hold'	0	0	16 symbol-times of 'Extra-wide BW mode' followed by 30 symbol-times of 'Wide BW' mode before reverting to 'Hold' mode
'Narrow Bandwidth'	0	1	16 symbol-times of 'Extra-wide BW mode' followed by 30 symbol-times of 'Wide BW' mode before reverting to 'Narrow BW' mode
'Medium Bandwidth'	1	0	16 symbol-times of 'Extra-wide BW mode' followed by 30 symbol-times of 'Wide BW' mode before reverting to 'Medium BW' mode
'Wide Bandwidth'	1	1	16 symbol-times of 'Extra-wide BW mode' before reverting to 'Wide BW' mode

The 'Extra-wide BW' PLL mode is designed to synchronise rapidly to the '+3 +3 -3 -3 ...' Symbol Sync pattern and is available only as part of an automatic acquisition sequence. Although not recommended, it is possible to use the FX919 in a non-standard system where there is an indeterminate delay between the transmitter startup and the Symbol Sync pattern, or where an Rx carrier detect signal is not available to the controlling µC. In these cases the Symbol Sync pattern should be extended to about 100 symbols, the Control Register LEVRES bits set to 'Lossy Peak Detect' and the PLLBW bits to 'Wide BW' before initating an 'SFS + AQSC + AQLEV' task. Once the Frame Sync pattern has been detected, the Control Register settings may be changed to 'Slow Peak Detect' and 'Medium' or 'Narrow' PLL BW for the remainder of the received message.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating temperature range: **FX919J4/L2**	-40°C to +85°C
Storage temperature range: **FX919J4/L2**	-40°C to +85°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Remarks	Min.	Max.	Unit
Supply Voltage (V_{DD})		4.5	5.5	V
Operating Temperature (T_{OP})		-40.0	+85.0	°C
Symbol Rate		2400	9600	symbols/sec
Xtal/Clock Frequency		1.0	10.0	MHz

Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 4.5 to 5.5V, T_{OP} = -40°C to +85°C. Xtal/Clock Frequency = 4.9152MHz.
Symbol Rate = 4800 symbols/sec.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
I_{DD}	1	-	5.0	-	mA
Tx Output					
Impedance	2	-	1.0	2.5	kΩ
Signal Level	3	0.8	1.0	1.2	Vp-p
Output DC Offset (wrt V_{DD}/2)	9	-0.25	-	0.25	V
Rx Input					
Impedance (Rx In pin)		-	10.0	-	MΩ
Rx Input Amp Voltage Gain		-	300	-	V/V
Input Signal Level	4	0.7	1.0	1.3	Vp-p
Input DC Offset (wrt V_{DD}/2)	4	-0.5	-	0.5	V
Xtal/Clock Input					
'High' pulse Width	5	40.0	-	-	ns
'Low' pulse Width	5	40.0	-	-	ns
Input Impedance		10.0	-	-	MΩ
Inverter Gain (I/P = 1mV rms @ 1kHz)		20.0	-	-	dB
µController Interface					
Input logic '1' Level	6, 7	V_{DD} -1.5	-	-	V
Input Logic '0' Level	6, 7	-	-	1.5	V
Input Leakage Current (V_{IN} = 0V to V_{DD})	6, 7	-5.0		+5.0	µA
Input Capacitance	6, 7	-	10.0	-	pF
Output Logic '1' Level (IOH = 120µA	7	V_{DD} -0.4			V
Output Logic '0' Level (IOL = 360µA)	7, 8	-	-	0.4	V
'Off' State Leakage Current (V = V_{DD})	8	-	-	10	µA

Specification .....

µController Interface Timings

Conditions: V_{DD} = 4.5 to 5.5V; T_{OP} = -40°C to +85°C; with a maximum load of 30pF to V_{SS} on pins D_0 toD_7.

Description		Note	Min.	Typ.	Max.	Unit
t_{ACSL}	"Address Valid" to "CS Low" time		0	-	-	ns
t_{AH}	"Address Hold" time		0	-	-	ns
t_{CSH}	"CS Hold" time		0	-	-	ns
t_{CSHI}	"CS High" time		6.0	-	-	Xtal/Clock Cycles
t_{CSRWL}	"CS" to "WR" or "RD" Low time		0	-	-	ns
t_{DHR}	"Read-Data Hold" time		0	-	-	ns
t_{DHW}	Write-Data Hold time		0	-	-	ns
t_{DSW}	Write-Data Set-Up" time		90.0	-	-	ns
t_{RHCSL}	"RD High" to "CS Low" time (write cycle)		0	-	-	ns
t_{RACL}	"Read Access" time from "CS Low"		-	-	175	ns
t_{RARL}	"Read Access" time from "RD Low"		-	-	145	ns
t_{RL}	"RD" Low time		200	-	-	ns
t_{RX}	"RD High" to "D_0-D_7 3-State" time		-	-	50.0	ns
t_{WHCSL}	"WR High" to "CS Low" time (read cycle)		0	-	-	ns
t_{WL}	"WR" Low time		200	-	-	ns

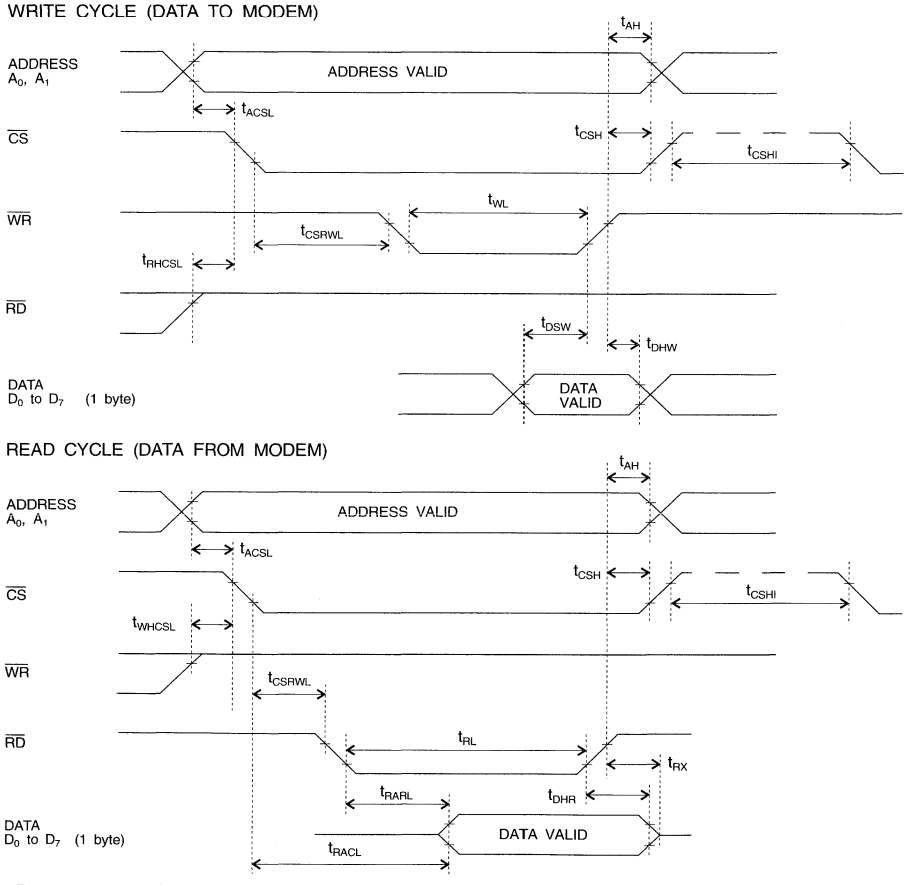


Fig.26 µProcessor Interface Read/Write Timing

Notes Overleaf .....

Specification .....

Notes:

1. V_{DD} = 5.0V, T_{OP} = 25°C; not including any current drawn from the modem pins by external circuitry.
2. Small signal impedance at 1kHz.
3. Measured after the external CR filter, for a '+3 +3 -3 -3 +3 +3 -3 -3 ... symbol sequence; at V_{DD} = 5.0V (output level is proportional to V_{DD}).
4. For optimum performance, measured at the Rx Feedback pin, for a '+3 +3 -3 -3 +3 +3 -3 -3 ... symbol sequence.
5. Timing for an external input to the Xtal/Clock pin.
6. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A_0 and A_1 pins.
7. D_0 - D_7 pins.
8. $\overline{IRQ}$ pin.
9. Measured at the Tx Out pin with the modem in the Tx (idle) mode.

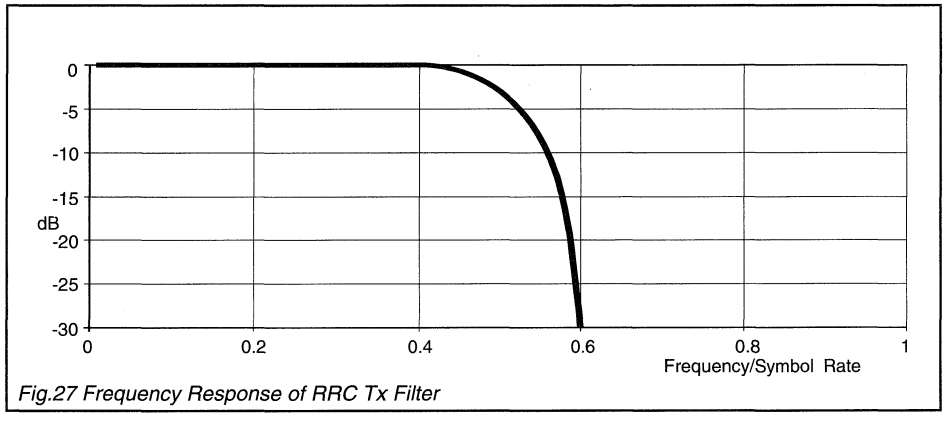


Fig.27 Frequency Response of RRC Tx Filter

Signal-to-Noise Performance

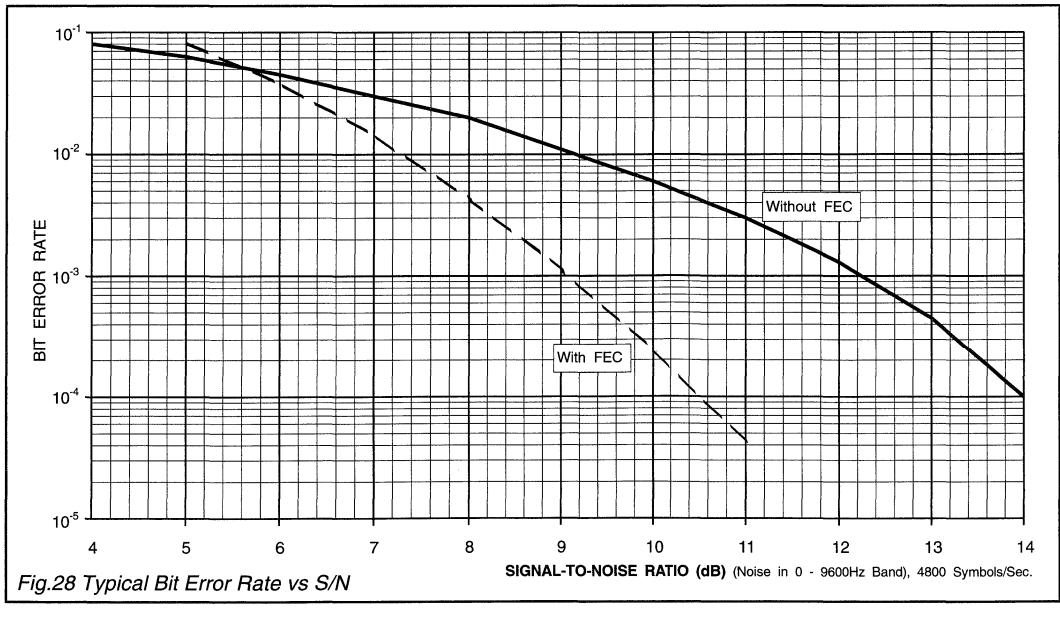


Fig.28 Typical Bit Error Rate vs S/N

Package Outlines

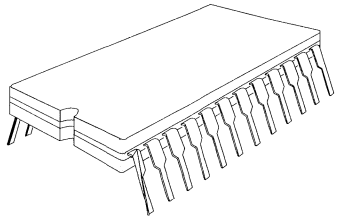
The FX919 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX919 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX919J4 24-pin cerdip DIL **(J)**

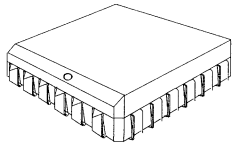
NOT TO SCALE



Max. Body Length 32.03mm
Max. Body Width 14.81mm

FX919L2 24-lead plastic leaded chip carrier **(LS)**

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX919J4 28-pin cerdip DIL **(J)**

FX919L2 24-lead plastic leaded chip carrier **(LS)**

CML Semiconductor Products

PRODUCT INFORMATION

FX929 Four-Level FSK "Packet Data" Modem for RD-LAP Systems

Publication D/929/1 July 1994
Advance Information

Features

- **Packet Data Transfer using RD-LAP Compatible Terminals**
  - **'Modacom' and 'Ardis' 9.6 and 19.2kb/s Data Links**
- **Half-Duplex Operation**
- **4-Level FSK - 4800 to 19,200b/s**
- **Rx/Tx Baseband Signal Filtering**
- **Automatic Protocol Handling**
  - **Symbol and Frame Sync**
  - **Block Formatting (Station ID, Header, Intermediate and Last)**
  - **Forward Error Correction**
  - **CRC Check and Generation**
  - **Interleaving**
- **5mA at 5 Volts; Low-Power**

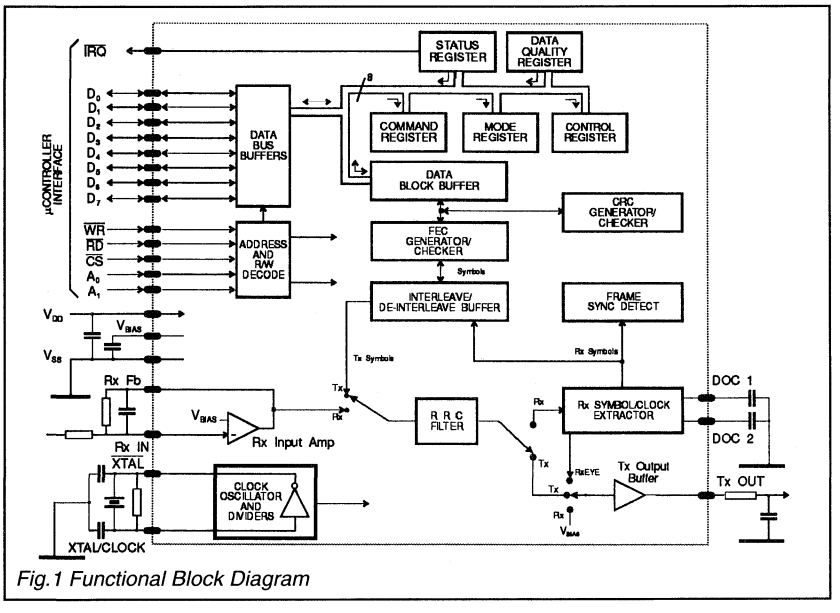


Fig.1 Functional Block Diagram

FX929

❍ Radio Data-Link Access Procedure (RD-LAP) is a data communications air interface protocol developed by Motorola Inc. ❍

Brief Description

The FX929 performs the baseband signal processing and most of the data formatting/de-formatting required to implement a 4-level FSK modem for use with FM radio and data links employing the RD-LAP protocol. Having a low power requirement of 5.0mA at 5 volts, this modem provides:

❍ Automatic handling of RD-LAP frame structures, including Rx symbol and frame synchronization, block formatting (Station ID, Header, Intermediate and Last blocks), CRC generation and checking, Forward Error Correction and Interleaving to reduce the processing load on the host µController.

❍ Half-duplex operation with selectable data rates of 2400 to 9600 symbols/s (4800 to 19,200bits/s).

❍ 4-Level FSK (2 bits per baud) enabling economical data-rates in a narrow RF bandwidth.

❍ On-chip baseband processing and filtering.

❍ Pre-selectable signal level acquisition and tracking permits the rapid acquisition of received signals, followed by automatic tracking of signal dc level variations.

Clock recovery PLL bandwidth and Rx signal level measurement circuitry will react automatically.

Rx and Tx data and control between the host µController and this microcircuit is via an 8-bit bi-directional parallel interface; input and output signals to and from the radio system are in analogue form suitable for connection to the radio's discriminator and frequency modulator.

The FX929 is available in both 24-pin DIL and Surface Mount packages.

Introduction

Table of Contents

FX929 Circuit Descriptions (See Figure 2)

Data Bus Buffers

Eight bi-directional 3-state logic-level buffers between the modem's internal registers and the controlling µController's data-bus lines.

Address and R/W Decode

Control the transfer of data bytes between the µController and the modem's internal registers, according to the state of the Write and Read Enable ($\overline{WR}$ and $\overline{RD}$) inputs, the Chip Select ($\overline{CS}$) input and the Register Address inputs (A_0 and A_1).

The Data Bus Buffers and Address and R/W Decode blocks provide a byte-wide parallel µController interface.

Status and Data Quality Registers

8-bit registers which the µController can read to determine the status of the modem and the received data quality.

Command, Mode and Control Registers

The values written by the µController to these 8-bit registers control the operation of the modem.

Data Block Buffer

A 12-byte buffer used to hold Rx or Tx data to or from the µController.

CRC Generator/Checker

A circuit which generates (transmit mode) or checks (receive mode) the Cyclic Redundancy Checksum bits which may be included in transmitted data blocks to allow the receive modem to detect transmission errors.

FEC Generator/Checker

In transmit mode, this circuit adds Forward Error Correction bits to the transmitted data, then converts the resulting binary data to 4-level symbols. In receive mode, it translates received 4-level symbols to binary data, using the FEC information to correct a large proportion of transmission errors. The 4 possible levels of a symbol are referred to in this Data Sheet as: +3, +1, -1 and -3.

Interleave/De-interleave Buffer

Interleaves data symbols within a data block before transmission and de-interleaves the received data so that the FEC system is best able to handle short noise bursts or fades.

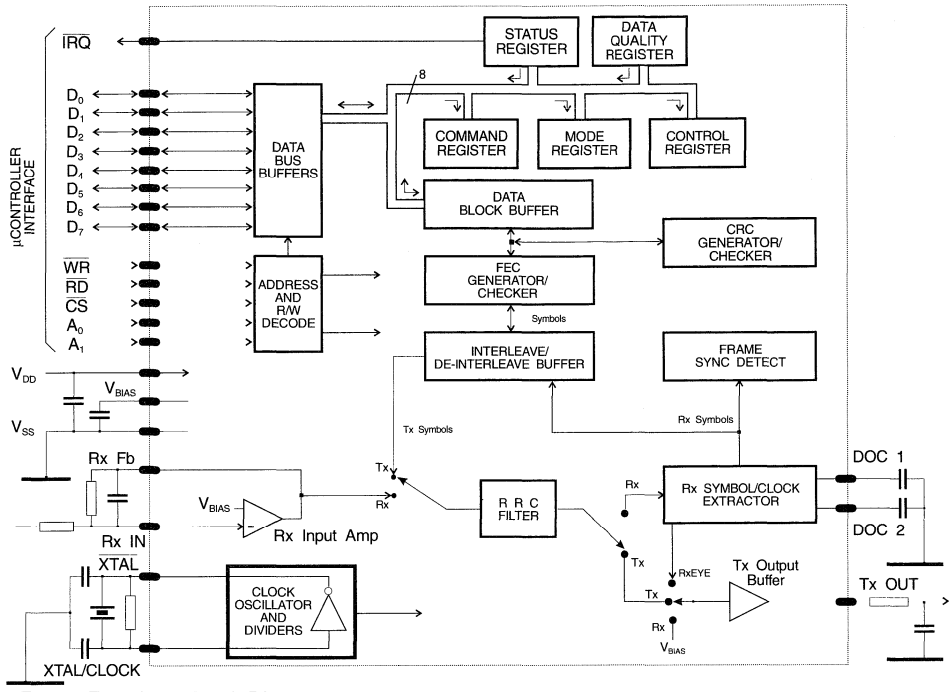


Fig.2 FX929 Functional Block Diagram

Rx Input Amp

The amplifier that allows the received signal input to the modem to be set to the optimum level by the selection of suitable external components.

Frame Sync Detect

This circuit, which is only active in the receive mode, is used to look for the 24-symbol Frame Synchronisation pattern which is transmitted to mark the start of every frame.

Root Raised Cosine (RRC) Filter

See Figure 27

This filter, which is used in both transmit and receive modes, is a linear-phase lowpass filter with a 'Root Raised Cosine' frequency response.

In Tx mode, the 4-level symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In Rx mode this filter is used to reject HF noise and to equalise the received signal to a form suitable for extracting the 4-level symbols.

Rx Symbol/Clock Extraction

These circuits, which operate only in receive mode, extract a symbol-rate clock from the received signal, and measure the received signal amplitude and its dc offset.

This information is then used to extract the received 4-level symbols and also to provide an input to the received Data Quality measuring circuit.

Clock Oscillator and Dividers

This circuit derives the transmit symbol-rate (and the nominal receive symbol-rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or fed from an external source.

Tx Output Buffer

A unity-gain amplifier used in the transmit mode to buffer the output of the RRC filter. In receive mode, the input of this buffer is normally connected to V_{BIAS} unless the RxEYE bit of the Mode Register is set. See Programming Information section. When the device's mode is changed from receive to transmit, the input to the buffer will remain connected to V_{BIAS} for a period of 8 symbol times while the RRC filter settles.

Pin Functions

FX929 (J4 and L2)	
1	**$\overline{IRQ}$:** A 'wire-ORable' output for connection to the controlling µController's Interrupt Request input. This output has a low-impedance pull-down to V_{SS} when active, and is high-impedance when inactive.
2	**D_7:**
3	**D_6:**
4	**D_5:**
5	**D_4:** 8 bi-directional 3-state µController interface data lines.
6	**D_3:**
7	**D_2:**
8	**D_1:**
9	**D_0:**
10	**$\overline{RD}$:** An active-low logic level input used to control the reading of data from the modem into the controlling µController.
11	**$\overline{WR}$:** An active-low logic level input used to control the writing of data into the modem from the controlling µController.
12	**V_{SS}:** The negative supply rail (ground).
13	**$\overline{CS}$:** An active-low logic level input to the modem used to enable a data Read or Write operation (see Figure 26, Timing).
14	**A_0:** Two logic-level modem register selection inputs.
15	**A_1:**
16	**$\overline{Xtal}$:** The output of the on-chip Xtal oscillator. Note that since the FX929 uses dynamic logic internally, operation without a suitable Xtal or clock input for more than a few milli-seconds will cause the current taken from V_{DD} to rise slowly to about twice its normal value, and may cause the state of the µController interface to become undefined.
17	**Xtal/Clock:** The input to the on-chip Xtal oscillator.
18	**Doc 2:** Connections to the internal Rx signal level measurement circuitry. Capacitors as described in Figure 3 should be fitted from each of these pins to V_{SS}. Any test equipment connected to these pins should have an input resistance of at least 100MΩ to V_{SS} to avoid disturbance of the measured levels.
19	**Doc 1:**
20	**Tx Out:** The Tx signal output from the modem.
21	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to V_{SS} by a capacitor mounted close to the device pins.
22	**Rx In:** The input to the Rx input amplifier.
23	**Rx Fb (Rx Feedback):** The output of the Rx Input Amplifier, and the input to the (Rx) Lowpass Filter.
24	**V_{DD}:** The positive supply. Levels and voltages within the modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the device pins.

Application Information

External Components

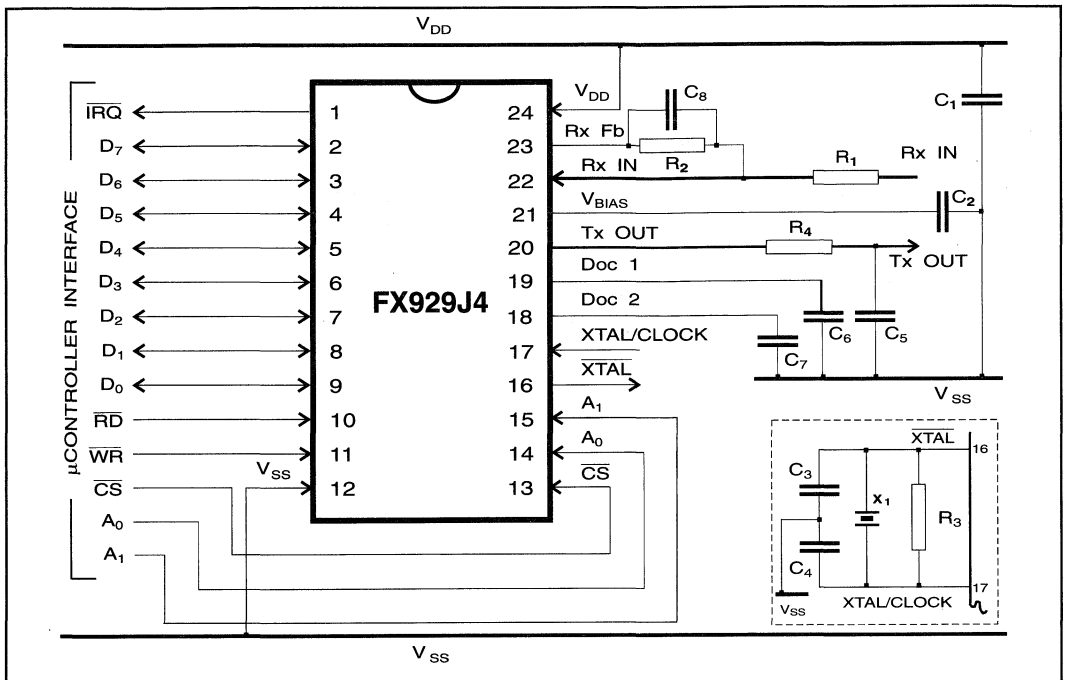


Fig.3 Recommended External Components

Component	Value	Tolerance
R_1	Note 1	±5%
R_2	100kΩ/Note 1	±5%
R_3	1.0MΩ	±20%
R_4	100kΩ/Note 2	±5%
C_1	0.1µF	±20%
C_2	0.1µF	±20%
C_3	Note 3	±20%
C_4	Note 3	±20%
C_5	Note 2	±5%
C_6	Note 2	±20%
C_7	Note 4	±20%
C_8	Note 1	±5%
X_1	4.9152MHz/Table 4	

Installation Notes

1. Resistors R_1 and R_2, with the Rx Input Amplifier, set the signal input level to the modem. The value of R_1 should be calculated to give 1.0v p-p at the Rx Feedback pin for a received +3 +3 -3 -3 +3 +3 -3 -3 sequence. The dc level of the received signal should be such that under nominal conditions the signal at the modem's Rx Feedback pin is centred around V_{BIAS}. Suggested values for R_2 and C_8 (including stray capacitance) for differing symbol-rates are:

Symbol-rate (s/s)	R_2	C_8
2,400	100kΩ	330pF
4,800	100kΩ	150pF
9,600	100kΩ	82.0pF

2. External components R_4 and C_5 form an RC lowpass filter between the Tx Buffer output and the input to the radio's frequency modulator; this is an important part of the Tx signal filtering. These components may form a part of any dc level shifting and gain adjustment circuitry.
The ground connection (V_{SS}) of C_5 should be positioned to give maximum attenuation of high frequency noise into the modulator.
Suggested values for R_4 and C_5 (including stray capacitance) for differing symbol-rates are:

Symbol-rate (s/s)	R_4	C_5
2,400	100kΩ	330pF
4,800	100kΩ	150pF
9,600	100kΩ	82.0pF

3. The values used for C_3 and C_4 should be suitable for the particular Xtal used as X_1.
As a guide, values (including stray capacitances) of 33pF at 1.0MHz falling to 18pF at 10MHz will generally prove suitable.
The equivalent series resistance of X_1 should be less than 2.0kΩ for a frequency of 1.0MHz, falling to 150Ω (max.) for X_1 = 10.0MHz. For optimum performance the frequency tolerance of X_1 should be ±10ppm or better, although tolerances as wide as ±50ppm may be used at the cost of slightly reduced bit-error-rate performance. .....

Installation Notes continue on the next page .....

Application Information .....

Installation Notes .....

3. .... If the on-chip Xtal oscillator is to be used, then the external components X_1, C_3, C_4, and R_3 are required as shown in Figure 3 (inset).
If an external clock source is to be used these components are not required; the input should be connected to the Xtal/clock pin and the Xtal pin left unconnected.Table 4 (Clock/Data Rates) provides advice on the selection of the correct Xtal value.

4. External capacitors C_6 and C_7 form part of the received signal level measuring circuit (Doc1 and Doc 2). For optimum performance the values of these components should be as shown below.

Operation	C_6 and C_7
2,400 symbols/sec	22.0nF
4,800 symbols/sec	10.0nF
9,600 symbols/sec	4.7nF

Binary to Symbol Translation

Although the over-air signal, and hence the signals at the modem Tx Out and Rx In pins, consists of 4-level symbols, the raw data passing between the modem and the µController is in binary form. The FX929 translates between binary data and the 4-level symbols in one of two ways, depending on the task being performed:

Direct

The simplest form, which converts between 2 binary bits and one symbol according to the table below.

Symbol	MSB	LSB
+3	1	1
+1	1	0
-1	0	0
-3	0	1

This scheme can be expanded so that an 8-bit byte translates to four symbols:

	MSB							LSB
Bits	7	6	5	4	3	2	1	0
Symbols	a		b		c		d	
	sent first						sent last	

With Forward Error Correcting (FEC)

This is more complicated, but essentially translates 3 binary bits to two 4-level symbols using an FEC coding scheme which lets the receiving modem detect and correct a large proportion of transmission errors.

Further details are given in the Operational Information section of this document.

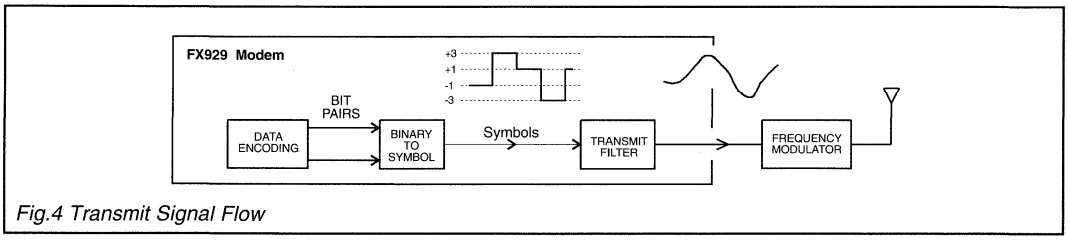


Fig.4 Transmit Signal Flow

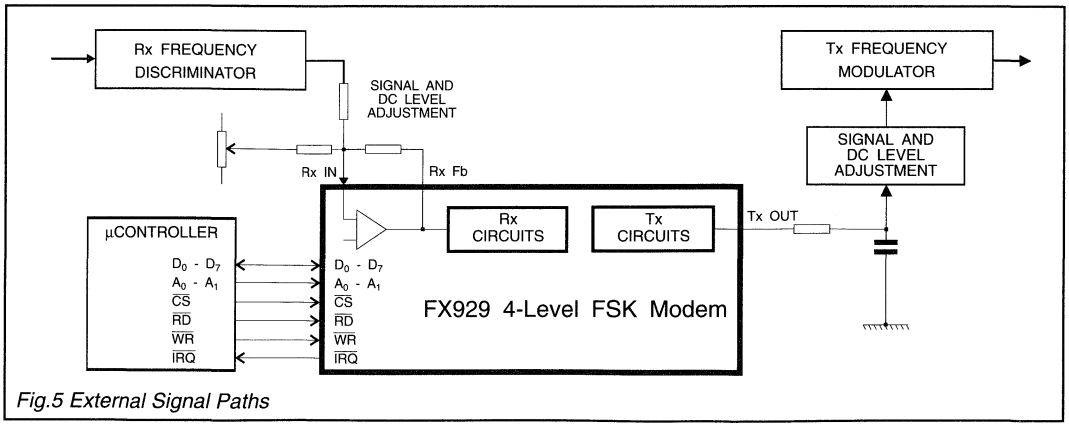


Fig.5 External Signal Paths

Application Information .....

AC Coupling

For a practical application, ac coupling from the modem's transmit output to the Frequency Modulator and from the receiver's Frequency Discriminator to the receive input of the modem may be desired. There are, however, two problems.

Firstly, ac coupling of the signal degrades the bit-error-rate performance of the modem.
Figure 6 illustrates the typical bit error rates at 4,800 symbols/sec (without FEC) for differing degrees of ac coupling;

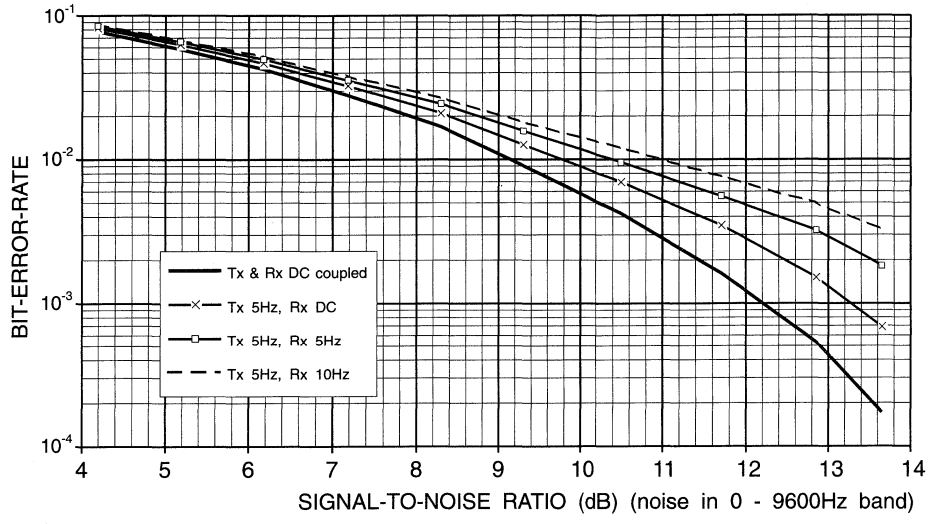


Fig.6 Examples of BER Performance Degradation Due to Varying Degrees of AC Coupling

Secondly, any ac coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits.
As illustrated below, the time for this voltage step to decay to 37% of its original value is:

Where f is the 3dB cut-off frequency of the ac coupling network; RC is 32msec (or 153 symbol-times at 4,800symbols/sec) for a 20Hz network.

In general, it will be best to dc couple the receive discriminator to the modem, and to ensure that any ac coupling to the transmitter's frequency modulator has a -3dB cut-off frequency of no higher than 5Hz (for 4,800 symbols/sec).

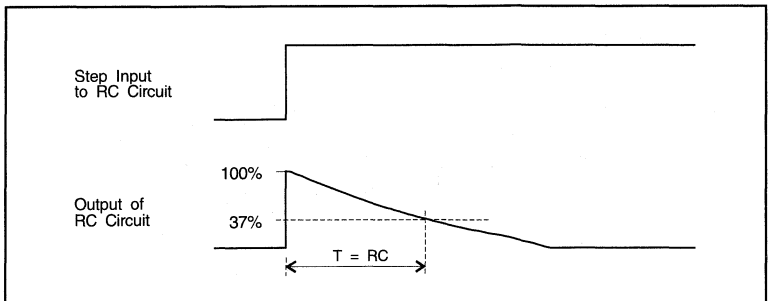


Fig.7 Decay Problems of the RC Network

Application Information .....

Radio Performance

The maximum data rate that can be transmitted over a radio channel using this modem depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Symbol rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracies.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 4,800 symbols/sec can be achieved (subject to local regulatory requirements) over a system with 12.5 kHz channel spacing if the transmitter frequency deviation is set to ±2.5kHz peak for a repetitive +3 +3 -3 -3 pattern and the maximum difference between transmitter and receiver "carrier" frequencies is less than 2,400Hz.

The modulation scheme employed by this modem is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. This does, however, place constraints on the performance of the radio.

In particular, attention must be paid to:

- Linearity, frequency and phase response of the Tx Frequency Modulator. For a 4,800 symbol/sec system, the frequency response should be within ±2dB over a range 3Hz to 5Hz, relative to 2,400Hz.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a dc offset at the discriminator output.

Viewing the received signal EYE (using the Mode Register RxEYE function) gives a good indication of the overall transmitter/receiver performance.

Rx Mode, RxEYE bit = '1'

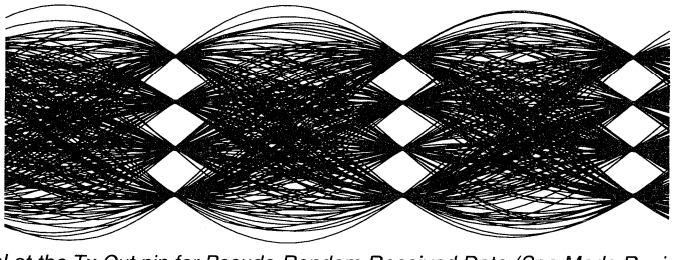


Fig.8 Rx Eye Signal at the Tx Out pin for Pseudo-Random Received Data (See Mode Register)

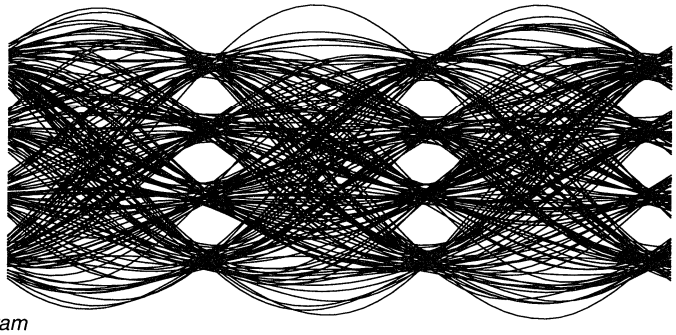


Fig.9 Tx Eye Diagram

Application Information .....

Baseband and RF Frequency Requirements

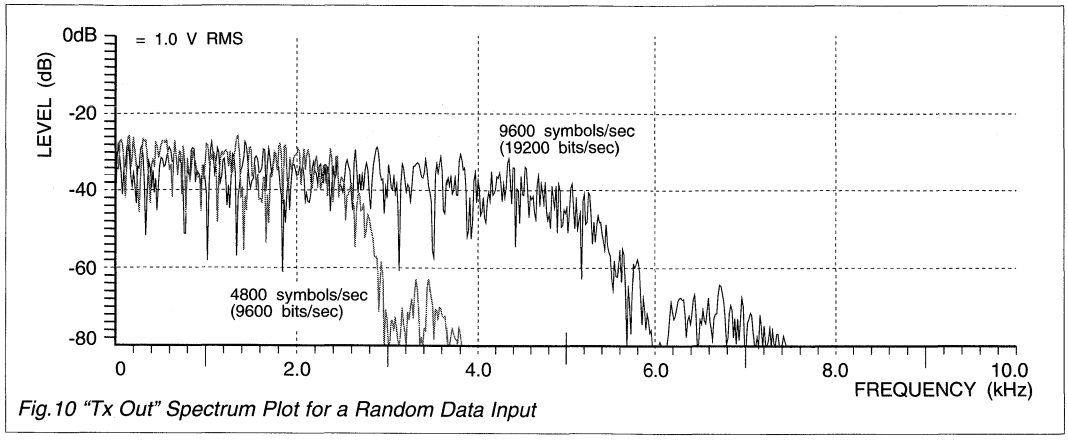


Fig.10 "Tx Out" Spectrum Plot for a Random Data Input

RF Channel Occupancy

The diagram below shows the theoretical RF bandwidth requirements when interfacing the FX929 baseband (Tx OUT) signal (Figure 10, above) to a radio transmitter. This plot assumes a perfect frequency modulator.

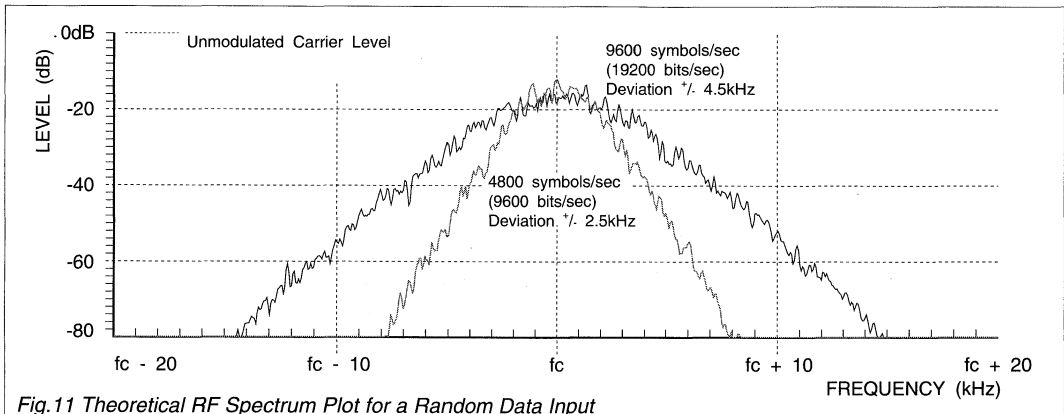
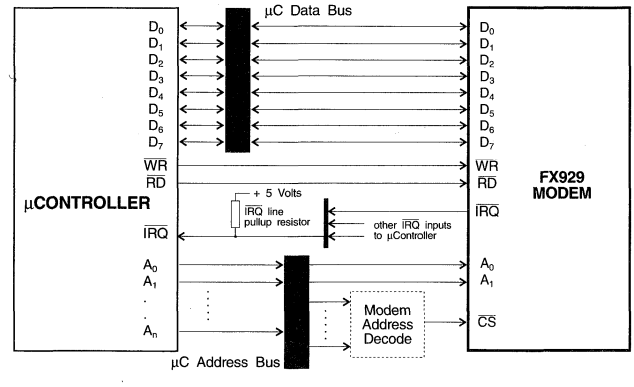


Fig.11 Theoretical RF Spectrum Plot for a Random Data Input

Note that particular repetitive data sequences, such as '+3 +3 -3 -3 +3 +3 ....' will produce spectra which are markedly different to those shown in Figures 10 and 11.



The Data Bus Buffers and Address and Read/Write Decode blocks form a byte-wide parallel µController interface. This diagram shows how this function can be memory mapped.

Fig.12 Typical Modem to µController Interface

Programming Information

Data Formats

Frame and Data Structures

The FX929 Frame structure is illustrated in Figure 13, and consists of a Frame Preamble (comprising a 24-symbol Frame Synchronization pattern and Station ID block), followed by a 'Header Block', one or more 'Intermediate Blocks' and a 'Last Block. Channel Status (S) symbols are included at regular intervals. The first Frame of any transmission is preceded by a Symbol Synchronization pattern.

The 'Header' block is self-contained in that it includes its own CRC, and would normally carry information such as: The addresses of the called and calling parties; the number of following blocks in the frame (if any), and miscellaneous control information.

The 'Intermediate' block(s) contain only data, the CRC checksum for all of the data in the 'Intermediate' and 'Last' blocks being contained at the end of the 'Last' block.

The FX929 performs all the necessary block formatting and de-formatting, the binary data transferred between the modem and its µController being that shown in the shaded areas of Figure 13.

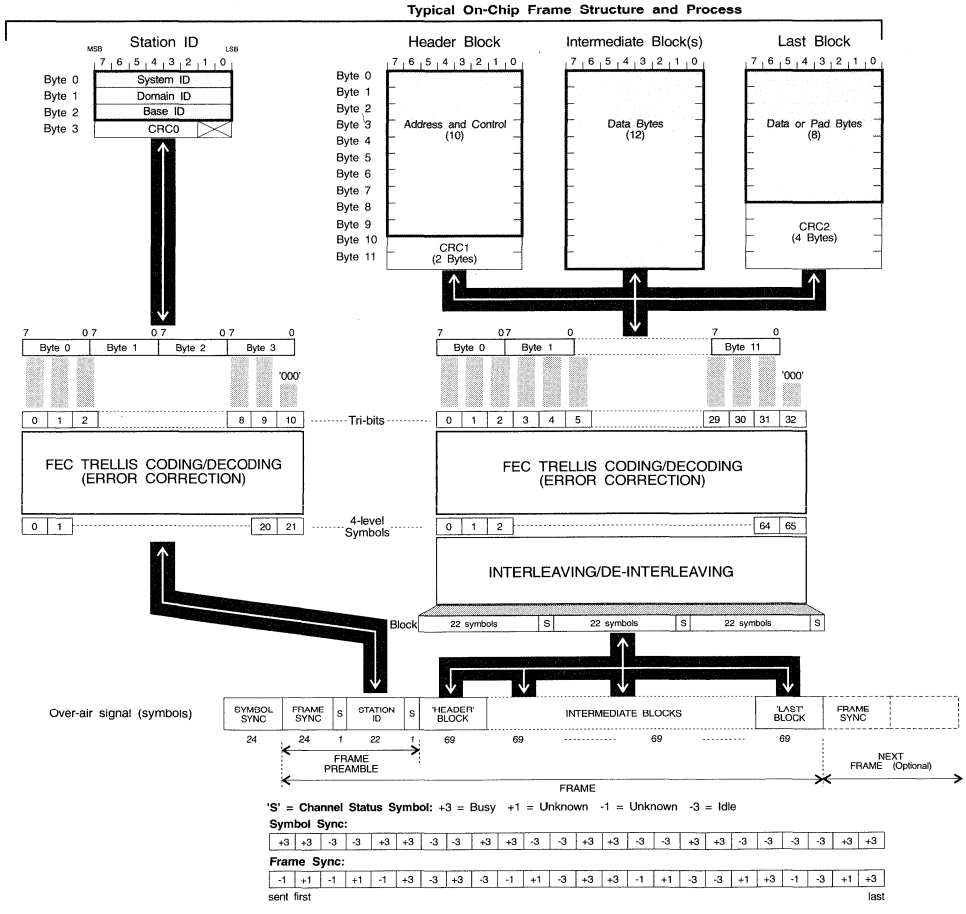


Fig.13 FX929 System Data Format

Programming Information .....

Modem/μController Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronisation pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (cyclic redundancy checksum) generation, Forward Error Correction coding and Interleaving. Details of the message format handled by this modem are shown in Figure 13.

To reduce the processing load on the associated μController, the FX929 has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting and de-formatting and - when in receive mode - in searching for and synchronising onto the Frame Preamble. In normal operation the modem will only require servicing by the μController once per received or transmitted block.

Thus, to transmit a block, the controlling μController has only to load the unformatted -'raw'- binary data into the modem's Data Block Buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result as 4-level symbols (with Forward Error Correction coding) and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary -using the FEC coding to correct as many errors as possible- and check the resulting CRC before placing the received binary data into the Data Block Buffer for the μController to read.

The FX929 can also handle the transmission and reception of unformatted data -to allow for example the transmission of Symbol and Frame Synchronisation sequences or special test patterns.

The Programmer's View

Register Selection

The FX929 modem appears to the programmer as 4 write-only 8-bit registers shadowed by 3 read-only registers. Individual registers are selected by the A_1 and A_0 inputs.

Table 1 Register Selection

A_1	A_0	Write to Modem	Read from Modem
0	0	Data Block Buffer	Data Block Buffer
0	1	Command Register	Status Register
1	0	Control Register	D Q Register
1	1	Mode Register	not used

Note that there is a minimum allowable time between accesses of the modem's registers. See Read and Write cycle timing diagrams.

Data Block Buffer

A 12-byte read/write buffer which is used to transfer data (as opposed to Command, Status, Mode, Data-Quality and Control information) between the modem and the controlling μController.

The Data Block Buffer appears to the μController as a single 8-bit register; the modem ensures that sequential μController 'read' or 'write' actions to the buffer are routed to the correct locations within this buffer.

When the modem is in the Tx mode, any attempt by the μController to 'read' from this buffer will have no effect. Similarly, any attempt to 'write' to this buffer will have no effect when the modem is in the Rx mode.

Note that when in Rx mode the modem will function correctly even if the received data is not read from the Data Block Buffer by the μController. The μController should only access this buffer when the Status Register BFREE (Buffer Free) is '1'.

Command Register

Writing to this register instructs the modem to perform a specific action or actions, depending upon the setting of the TASK, AQLEV, and AQSC bits.

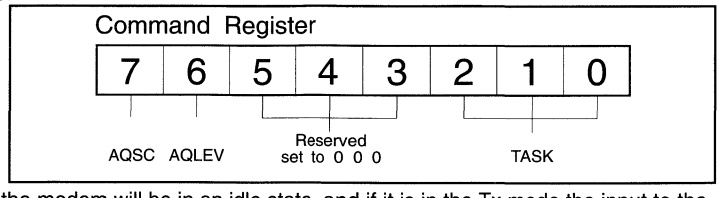


Fig.14 The Command Register

When it has no action to perform, the modem will be in an idle state, and if it is in the Tx mode the input to the Tx Filter will be connected to a voltage mid-way between the '+1' and '-1' symbol voltages.

In the Rx mode the modem will continue to measure the received data quality and extract symbols from the received signal, feeding them into the De-Interleave Buffer, but will otherwise ignore the received data.

Command Register

B7 AQSC

Acquire Symbol Clock: This bit has no effect in the Tx mode.

In the Rx mode, whenever a byte with the AQSC bit set to logic '1' is written to the Command Register, it initiates an automatic sequence designed to achieve timing synchronisation with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received symbol-timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronisation is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to logic '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be restarted every time that a byte written to the Command Register has the AQSC bit set to logic '1'. The AQSC bit will normally be set at the same time as a SFS (Search for Frame Sync) or SFP (Search for Frame Preamble) task, however it may also be used independently to re-establish clock synchronisation quickly after a long fade. Alternatively, an SFS or SFP task may be written to the Command Register with the AQSC bit at logic '0' if it is known that clock synchronisation does not need to be re-established.

B6 AQLEV

Acquire Receive Signal Levels: This bit has no effect in the Tx mode.

In receive mode, whenever a byte with the AQLEV bit set to a logic '1' is written to the Command Register, it initiates an automatic sequence designed to measure the amplitude and dc offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time -hence improving the measurement accuracy- until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to a logic '0' (or changing it from '1' to '0') has no effect; note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQLEV bit set to a logic '1'.

The AQLEV bit will normally be set at the same time as an SFS (Search for Frame Sync) or SFP (Search for Frame Preamble) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, a SFS or SFP task may be written to the Command Register with the AQLEV bit at logic '0' if it is known that there is no need to re-establish the received signal levels.

B5
B4
B3

These bits should each be set to a logic '0'.

B2
B1
B0
TASK

Task: Operations such as transmitting a data block are treated by the modem as 'Tasks'. Information on Task functions is given on the following pages.

A task is initiated when the µController writes a byte to the Command Register with the Task bits set to anything other than the 'NULL' code.

The µController should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is a logic '0'.

Different tasks apply in receive and transmit modes.

Tx Mode: All tasks other than NULL, RESET instruct the modem to transmit data from the Data Block Buffer, formatting it as required. For these tasks the µController should wait until the BFREE (Buffer Free) bit of the Status Register is a logic '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number '0' of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will: Set the BFREE (Buffer Free) bit of the Status Register to a logic '0', take the data from the Data Buffer as quickly as it can -transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Programming Information .....

Command Register

B2 **B1** **B0** **TASK**	**Task: .....** Once all of the data has been transferred from the Data Block Buffer the modem will set the BFREE and IRQ bits of the Status Register to a logic '1', (causing the interrupt output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the µController that it may write new data and the next task to the modem. In this way the µController can write a task -and the associated data- to the modem while the modem is still transmitting the data from the previous task. **Rx Mode:** The µController should wait until the BFREE bit of the Status Register is a logic '1', then write the desired task to the Command Register. Once the byte containing the desired task has been written to the Command Register, the modem will: Set the BFREE bit of the Status Register to a logic '0'. Wait until enough received bits are in the De-Interleave Buffer. Decode them as needed, and transfer any resulting data to the Data Block Buffer. Then the modem will set the BFREE and IRQ bits of the Status Register to logic '1', (causing the interrupt output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the µController that it may read from the Data Buffer and write the next task to the modem. In this way the µController can read data and write a new task to the modem while the received symbols needed for this new task are being stored in the De-Interleave Buffer.

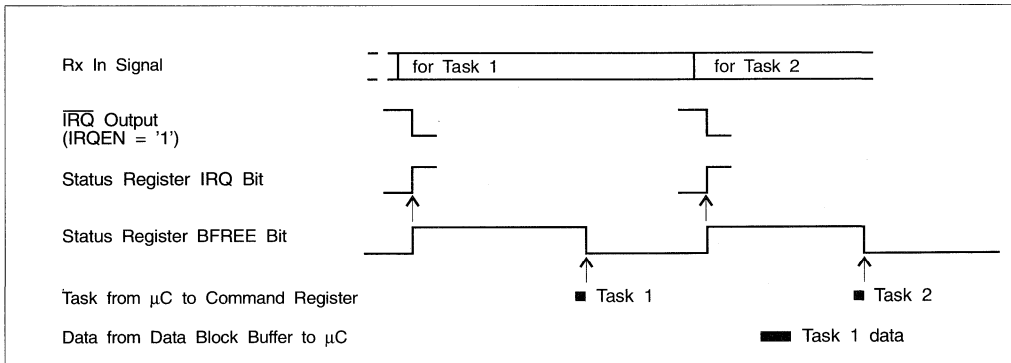


Fig.15 The Receive Process

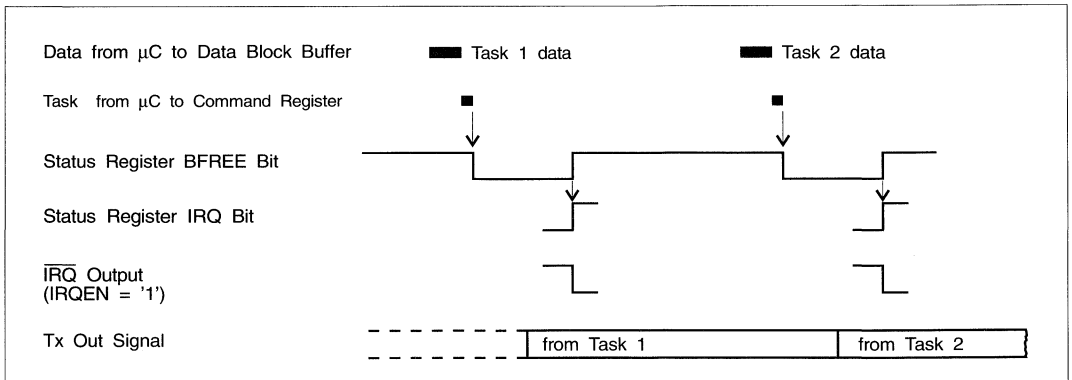


Fig.16 The Transmit Process

Modem Tasks in Detail

The following describes the setting and format of the Command Register 'task' bits (bits 2, 1 and 0). Note that before a task is programmed the Tx/Rx bit in the Mode Register must be placed in the relevant position.

Command Bits 2	1	0		Receive Mode		Transmit Mode
0	0	0	NULL	.. ..	NULL	.. ..
0	0	1	SFP	Search for Frame Preamble	T24S	Transmit 24 Symbols
0	1	0	RHB	Read Header Block	THB	Transmit Header Block
0	1	1	RILB	Read Intermediate or Last Block	TIB	Transmit Intermediate Block
1	0	0	SFS	Search for Frame Sync	TLB	Transmit Last Block
1	0	1	R4S	Read 4 Symbols	T4S	Transmit 4 Symbols
1	1	0	RSID	Read Station ID	TSID	Transmit Station ID
1	1	1	RESET	Cancel any Current Action	RESET	Cancel any Current Action

Table 2 Modem Task Details

Modem Tasks

NULL

No Effect. This task is provided so that an AQSC or AQLEV (Command Register) command can be initiated without loading a new task.

SFP

Search for Frame Preamble. Causes the modem to search the received signal for a valid RD-LAP Frame Preamble, consisting of a 24-symbol Frame Sync sequence followed by Station ID data which has a correct CRC0 checksum. This task continues until a valid Frame Preamble has been found. The search consists of four stages:

1. The modem will attempt to match the incoming symbols against the RD-LAP Frame Synchronisation pattern to within the tolerance defined by the Frame Sync Tolerance (FSTOL) bits of the Control Register.
2. Once a match has been found, the modem will read-in the following 'S' symbol then update the SVAL bits of the Status Register and set the SRDY bit to a logic '1'. (The IRQ bit of the Status Register will also be set to a logic '1' at this time if the SSIEN bit of the Mode Register is a logic '1').
3. The modem will then read the next 22 symbols as Station ID data. The 22 Station ID symbols will be decoded and the CRC0 checked. If this is incorrect, the modem will resume the search, looking for a fresh Frame Sync pattern.
4. If the received CRC is correct, the following 'S' symbol will be read in, the SVAL bits of the Status Register updated and the SRDY, BFREE and IRQ bits set to a logic '1', the CRCERR bit cleared to a logic '0', and the three decoded Station ID bytes placed into the Data Block Buffer.

On detecting the BFREE bit of the Status Register has gone to a logic '1', the µController should read the 3 Station ID bytes from the Data Block Buffer and then write the next task to the modem's Command Register.

RHB

Read Header Block. Causes the FX929 to read the next 69 symbols as a 'Header' block. It will strip out the 'S' symbols then de-interleave and decode the remaining 66 symbols, placing the resulting 10 data bytes and the 2 received CRC bytes into the Data Block Buffer, and setting the BFREE and IRQ bits of the Status Register to a logic '1' when the task is complete to indicate that the µController may read the data from the Data Block Buffer and write the next task to the modem's Command Register. The CRCERR bit of the Status Register will be set to a logic '1' or '0' depending on the validity of the received CRC1 checksum bytes.
As each of the 3 'S' symbols of a block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to a logic '1'. (If the SSIEN bit of the Mode Register is a logic '1', then the Status Register IRQ bit will also be set to a logic '1'). Note that when the third 'S' symbol is received, the SRDY bit will be set to a logic '1' coincidentally with the BFREE bit also being set to a logic '1'.

Modem Tasks .....

RILB	**Read 'Intermediate' or 'Last' Block.** Causes the modem to read the next 69 symbols as an 'Intermediate' or 'Last' block (the µController can tell from the received 'Header' block how many blocks are in the frame, and hence when to expect the 'Last' block). In each case, it will strip out the 3 'S' symbols, de-interleave and decode the remaining 66 symbols and place the resulting 12 bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register to a logic '1' when the task is complete to indicate that the µController may read the data from the Data Block Buffer and write the next task to the modem's Command Register. If an 'Intermediate' block is received then the µController should read out all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µController need only read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum. Note that in the Rx mode the CRC2 checksum circuits are initialised on completion of any task other than NULL or RILB. As each of the 3 'S' symbols of a block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to a logic '1'. (If the SSIEN bit of the Mode Register is a logic '1', then the Status Register IRQ bit will also be set to a logic '1'). Note that when the third 'S' symbol is received, the SRDY bit will be set to a logic '1' coincidentally with the BFREE bit also being set to a logic '1'.
SFS	**Search for Frame Sync.** This task, which is intended for special test and channel monitoring purposes, performs the first two parts only of a Search for Frame Preamble (SFP) task. It causes the modem to search the received signal for a 24-symbol sequence which matches the RD-LAP Frame Synchronisation pattern to within the tolerance defined by the FSTOL bits of the Mode Register. When a match is found the modem will read in the following 'S' symbol, then set the BFREE, IRQ and SRDY bits of the Status Register to a logic '1' and update the SVAL bits. The µController may then write the next task to the Command Register.
R4S	**Read 4 Symbols.** This task is intended for special tests and channel monitoring -perhaps preceded by an SFS task. Causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set high to a logic '1' to indicate that the µController may read the data byte from the Data Block Buffer and write the next task to the Command Register.
RSID	**Read Station ID.** Causes the modem to read in and decode the following 23-symbols as Station ID data followed by an 'S' symbol. It is similar to the last two parts of a SFP task except that it will not re-start if the received CRC0 is incorrect. It would normally follow an SFS task. The decoded System, Domain and Base ID bytes will be placed into the Data Block Buffer, and the CRCERR bit of the Status Register set to a logic '1' if the received CRC0 was incorrect, otherwise it will be cleared to a logic '0'. The SVAL bits of the Status Register will be updated and the BFREE, SRDY and IRQ bits set to a logic '1' to indicate that the µController may read the 3 Station ID bytes from the Data Block Buffer and write the next task to the modem's Command Register.
T24S	**Transmit 24 Symbols.** This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC, FEC, Interleaving or adding any 'S' symbols. Byte '0' of the Data Block Buffer is sent first, byte '5' last. Once the modem has read all the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

The tables prepared on the following page show what data has to be written to the Data Block Buffer to transmit the RD-LAP Symbol and Frame Sync Sequences: .....

Modem Tasks .....

T24S ..... **Transmit 24 Symbols .....** These tables show what data has to be written to the Data Block Buffer to transmit the RD-LAP Symbol and Frame Sync Sequences: .....

'Symbol Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
+3	+3	-3	-3	Byte 0 :	1 1 1 1 0 1 0 1	F5
+3	+3	-3	-3	Byte 1 :	1 1 1 1 0 1 0 1	F5
+3	+3	-3	-3	Byte 2 :	1 1 1 1 0 1 0 1	F5
+3	+3	-3	-3	Byte 3 :	1 1 1 1 0 1 0 1	F5
+3	+3	-3	-3	Byte 4 :	1 1 1 1 0 1 0 1	F5
-3	-3	+3	+3	Byte 5 :	0 1 0 1 1 1 1 1	5F

'Frame Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
-1	+1	-1	+1	Byte 0 :	0 0 1 0 0 0 1 0	22
-1	+3	-3	+3	Byte 1 :	0 0 1 1 0 1 1 1	37
-3	-1	+1	-3	Byte 2 :	0 1 0 0 1 0 0 1	49
+3	+3	-1	+1	Byte 3 :	1 1 1 1 0 0 1 0	F2
-3	-3	+1	+3	Byte 4 :	0 1 0 1 1 0 1 1	5B
-1	-3	+1	+3	Byte 5 :	0 0 0 1 1 0 1 1	1B

THB **Transmit Header Block.** Takes 10 bytes of data (Address & Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols and transmits the result as an RD-LAP formatted 'Header' Block inserting 'S' symbols at 22-symbol intervals.
Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

TIB **Transmit Intermediate Block.** Takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as an RD-LAP formatted 'Intermediate' Block inserting 'S' symbols at 22-symbol intervals. Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the µController that it may write the next task and its data to the modem.
Note that in Tx mode the CRC2 checksum circuits are initialised on completion of any task other than NULL, TIB or TLB.

TLB **Transmit 'Last' Block.** Takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12-bytes to 4-level symbols with (FEC), interleaves the symbols and transmits the result as an RD-LAP formatted 'Last' Block, inserting 'S' symbols at 22-symbol intervals.
Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the µController that it may write the next task and its data to the modem.

T4S **Transmit 4 Symbols.** This task is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

Programming Information .....

Modem Tasks	
TSID	**Transmit Station ID.** Takes 3 Station ID bytes from the Data Block Buffer, calculates and appends the 6-bit CRC0 checksum, translates the result to 4-level symbols (with FEC) and transmits the resulting 22 symbols preceded and followed by 'S' symbols. Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the µController that it may write the next task and its data to the modem.
RESET	**RESET.** Stop any current action. This 'task' takes effect immediately, and terminates any current action (task , AQSC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to a logic '1', without setting the IRQ bit. RESET should be used to set the modem into a known state when V_{DD} is applied. *Note that due to delays in the transmit filter, it will take several symbol-times for any change to become apparent at the Tx Out pin.*

RRC Filter Delay

The Task Timing figures detailed in Table 3 are based upon: the signal at the input to the RRC Filter in the transmit mode, or the signal at the input to the de-interleave circuits in the receive mode. As can be seen from the diagram in Figure 17, there is an additional delay of approximately 8 (eight) symbol-times in both Tx and Rx modes due to the (Tx/Rx) RRC Filter.

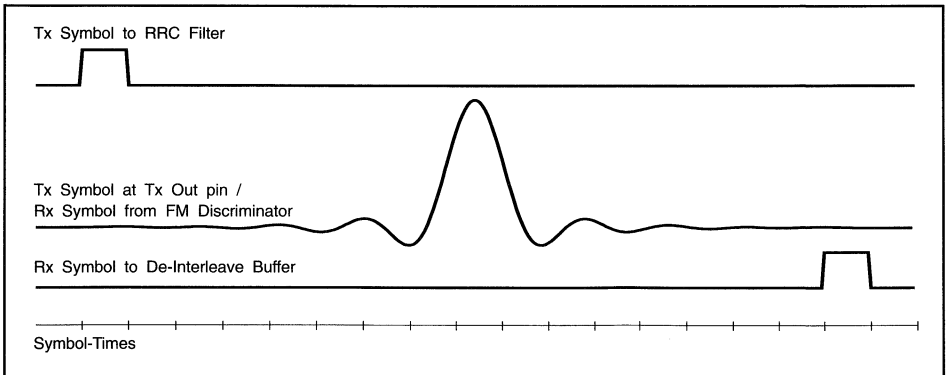


Fig.17 Examples of Filter Delay Times

Transmit and Receive Task Timing

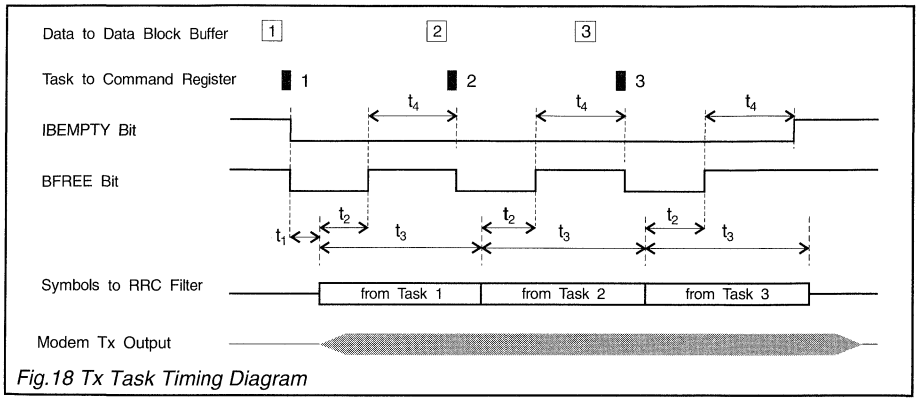


Fig.18 Tx Task Timing Diagram

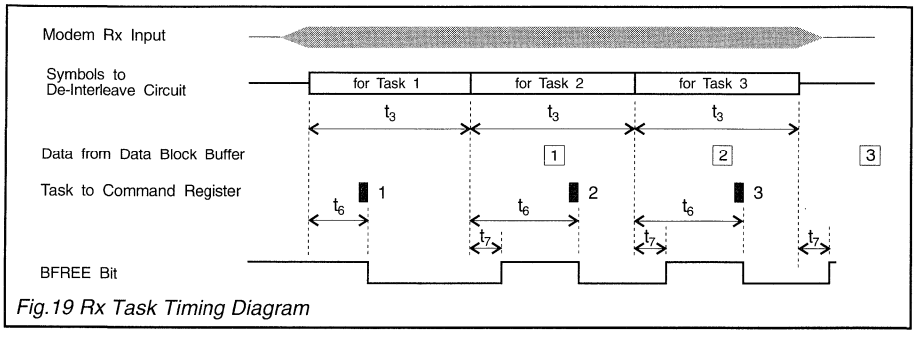


Fig.19 Rx Task Timing Diagram

Timing	Notes	Task	Time (symbol times)
t_1	Modem in idle state. Time from writing first task to the application of the first Tx symbol to the RRC Filter.	Any	1 to 2
t_2	Time from the application of the first symbol of the task to the RRC Filter until BFREE goes to a logic '1' (high).	T24S TSID THB/TIB/TLB T4S	5 6 16 0
t_3	Time to transmit all symbols of the task. or Time to receive all symbols of the task	T24S/TSID THB/TIB/TLB RHB/RILB T4S SFS SFP R4S RSID	24 69 69 4 25 (Min.) 48 (Min.) 4 23
t_4	Maximum time allowed from BFREE going to a logic '1' for the next task (and data) to be written to the modem.	T24S TSID THB/TIB/TLB T4S	18 17 52 3
t_6	Maximum time between the first symbol of the task entering the de-interleave circuit and the task being written to the modem.	SFP/SFS RHB/RILB RSID R4S	21 51 15 3
t_7	Time from last symbol of task entering the de-interleave circuit to BFREE going to a logic '1'.	Any	1

Table 3 Typical Rx/Tx Task Load Timings

Programming Information .....

Control Register

This 8-bit write-only register controls the modem's symbol-rate, the response times of the receive clock extraction and signal level measurement circuits and the Frame Sync pattern recognition tolerance.

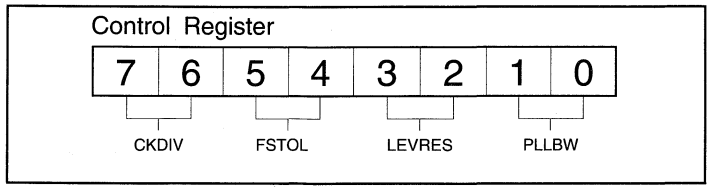


Fig.20 The Control Register

Control Register

Table 4 shows how bit-rates of 2,400/4,800/9,600 symbols per second may be obtained from common Xtal/clock frequencies.

B7, B6 CKDIV

Clock Division Ratio: These bits control a frequency divider driven from the clock signal present at the Xtal pin; this ratio and Xtal input will determine the nominal symbol-rate.

		Division Ratio Xtal Freq. / Symbol Rate	Xtal Frequency (MHz)		
			2.4576	4.9152	9.8304
B7	B6		Symbol Rate (symbols/sec.)		
0	0	512	4,800	9,600	
0	1	1024	2,400	4,800	9,600
1	0	2048		2,400	4,800
1	1	4096			2,400

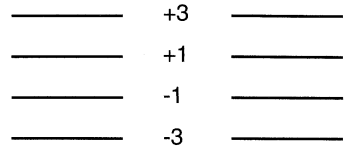
Table 4 Clock/Data Rates ***Note*** *that device operation is not guaranteed or specified above 9,600symbols/s or below 2,400symbols/s*

B5, B4 FSTOL

Frame Sync Tolerance: For use in the Rx mode only; these bits have no effect in the Tx mode. These bits define the maximum number of mismatches which will be allowed during a search for the Frame Sync pattern:

B5	B4	Mismatches Allowed
0	0	0
0	1	2
1	0	4
1	1	6

Note that a single 'mismatch' is defined as the difference between two adjacent symbol levels; if the symbol '+1' were expected, then the received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2.



Symbol Levels

Control Register .....

B3, B2
LEVRES

Level Measurement Modes: These bits are only used in the Rx mode and have no effect in the Tx mode; they set the 'normal' operating mode of the Rx signal amplitude and dc offset measuring circuits. This setting will be temporarily overridden by the automatic sequencing of an AQLEV command.

For most applications these two bits should be set to 'Slow Peak Detect' mode, in which the peak positive and peak negative excursions of the received signal (after filtering) are measured to establish the amplitude and dc offset of the signal. The decay time-constant of the peak rectifier circuits used in this mode is approximately 1000 symbol-times.

The 'Hold' setting freezes the stored values of the current amplitude and offset measurements and may therefore be used to improve performance during short fades or for while the radio is switched from Rx mode for the transmission of a short acknowledgement. It should be noted, however, that the measured amplitude and offset values are stored on the external "Doc" capacitors and will decay gradually when the 'Hold' setting is chosen, the discharge-time constant being approximately 1000 symbol-times.

The 'Lossy Peak Detect' setting is similar to 'Slow Peak Detect' except that the decay time-constants of the peak detectors are reduced to approximately 75 symbol-times to give a faster response to signal changes at the expense of BER performance. This mode is used by the automatic level measurement acquisition sequence but may also be useful in non-standard systems.

The 'Clamp' setting is primarily intended for use by the automatic level measurement acquisition sequence, but may also be useful in non-standard systems. In this mode the Doc 1 and Doc 2 pins are connected directly to the output of the circuit that normally drives the peak detectors.

Table 5 details bit-setting application.

B3	B2	Setting
0	0	Hold
0	1	Slow Peak Detect
1	0	Lossy Peak Detect
1	1	Clamp

Table 5

B1, B0
PLLBW

PLL Bandwidth: For use in the Rx mode only (no effect in Tx).
In the receive mode these two bits set the 'normal' bandwidth of the Rx Clock Extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the automatic sequence of an AQSC (Command Register Bit 7) command.

B1	B0	PLL Mode	Working Bandwidth (± ppm)
0	0	Hold	0
0	1	Narrow Bandwidth	20
1	0	Medium Bandwidth	100
1	1	Wide Bandwidth	650

Note: 'Working Bandwidths' are the maximum difference between the actual received symbol rate and the nominal rate determined by the tolerance of the modem's Xtal frequency, to give minimal degradation of a reasonably random received signal.

Table 6

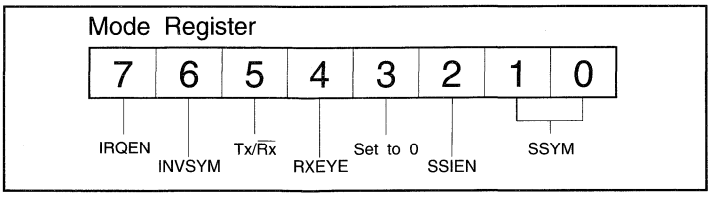
The minimum bandwidth consistent with the transmit and receive modem symbol rate tolerances should be chosen, i.e. if the Xtals used with both modems have accuracies of within ±50ppm, then the PLLBW bits should be set to '1' '0' (Medium Bandwidth).
The 'Wide Bandwidth' setting is intended for message acquisition in systems where the µController cannot detect the start of the received message, as it allows the modem to respond rapidly to fresh messages and recover rapidly after a fade without µController intervention - although at the cost of reduced Bit Error Rate vs Signal to Noise performance.
The 'Hold' setting disables the PLL feedback loop, and may be used during signal fades.
The Narrow' setting should preferably not be applied until about 200 symbols after an AQSC, to allow time for the PLL to settle.

Programming Information .....

Mode Register

This 8-bit write-only register controls the basic operating modes of the modem.

Fig.21 The Mode Register



Mode Register

B7 IRQEN

IRQ Output Enable. When set to a logic '1' the Interrupt Request output is pulled low (to V_{SS}) whenever the IRQ bit (BIT 7) of the Status Register is set by the modem to a logic '1'.
When set to a logic '0' the Interrupt Request output will not function and will remain in its high-impedance state (see Pin Functions and Figure 12 - µController Interface).

B6 INVSYM

Invert Symbols. Controls the polarity (sense) inversion of transmitted and received symbol voltages.

B6	Symbol	Signal at Tx Out	Signal at Rx Fb
'0'	'+3'	above V_{BIAS}	below V_{BIAS}
'0'	'-3'	below V_{BIAS}	above V_{BIAS}
'1'	'+3'	below V_{BIAS}	above V_{BIAS}
'1'	'-3'	above V_{BIAS}	below V_{BIAS}

B5 Tx/Rx

Tx/$\overline{Rx}$ Mode. When set to a logic '1' places the modem in the Transmit mode; when set to a logic '0' places the modem in the Receive mode.
Note that changing between Transmit and Receive modes will cancel any current task.

B4 RxEYE

Show Rx Eye. This bit should be set to a logic '0' for normal Rx operation and always for Tx operation.
Setting this bit to a logic '1' in the receive mode configures the modem into a special test mode, in which the input to the Tx Output Buffer is connected to the Rx Symbol/Clock Extraction circuit at a point which carries the equalised receive signal. This may be monitored with an oscilloscope (at the Tx Out pin *before* the external RC filter), to assess the quality of the complete radio channel including the Tx and Rx modem filters, the Tx modulator and the Rx IF filters and FM demodulator. The resulting 'eye' diagram (for reasonably random data) should ideally be as shown in Figure 8, with 4 'crisp' and equally spaced crossings.

B3

This bit should always be set to a logic '0'.

B2 SSIEN

'S' Symbol IRQ Enable. In Transmit Mode, setting this bit to a logic '1' causes the IRQ bit of the Status Register to be set to a logic '1' whenever a new 'S' symbol has been transmitted. (The SRDY bit of the Status Register will also be set to a logic '1' at the same time.)
In Receive Mode, setting this bit to a logic '1' causes the IRQ bit of the Status Register to be set to a logic '1' whenever a new 'S' symbol has been received. (The SRDY bit of the Status Register will also be set to a logic '1' at the same time.)

B1, B0 SSYM

'S' Symbol to be Transmitted.
Transmit Mode Only. These two bits define the next "'S' Symbol" to be transmitted.

B1	B0	'S' Symbol	Meaning
0	0	-1	Unknown
0	1	-3	Idle
1	0	+1	Unknown
1	1	+3	Busy

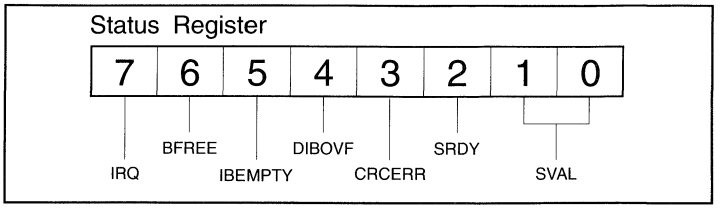
These two bits have no effect in the Receive Mode.

Programming Information .....

Status Register

This register may be read by the µController to determine the current state of the modem.

Fig.22 The Status Register



Status Register

B7 IRQ

Interrupt Request. This bit is set to a logic '1' by:

The Status Register BFREE bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's Tx/Rx bit.

or

The Status Register IBEMPTY bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's Tx/Rx bit.

or

The Status Register DIBOVF bit going from a logic '0' to '1'.

or

The Status Register SRDY bit being set to a logic '1' (due to an 'S' symbol being received or transmitted) if the Mode Register SSIEN bit is a logic '1'.

This (IRQ) bit is cleared to a logic '0' immediately after a read of the Status Register.
If the IRQEN bit of the Mode Register is a logic '1', the FX929 $\overline{IRQ}$ output pin will be pulled low (to V_{SS}) whenever the Status Register IRQ bit is a logic '1'.

B6 BFREE

Data Block Buffer Free. BFREE reflects the availability of the Data Block Buffer; BFREE is cleared to a logic '0' *(Buffer NOT Free)* whenever a task other than NULL or RESET is written to the Command Register.
In Transmit Mode, the BFREE bit will be set to a logic '1' (also setting the Status Register IRQ bit to a logic '1) when the modem is ready for the µController to write new data to the Data Block Buffer and the next task to the Command Register.
In Receive Mode, the BFREE bit is set to a logic '1' (also setting the Status Register IRQ bit to a logic '1) by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The µController may then read that data and write the next task to the Command Register.
The BFREE bit is also set to a logic '1' -but without setting the IRQ bit- by a RESET task or when the Mode Register's Tx/Rx bit is changed.

B5 IBEMPTY

Interleave Buffer Empty. In Transmit mode, IBEMPTY is set to a logic '1' (also setting the IRQ bit) when less than two symbols remain in the Interleave Buffer or the Interleave Buffer is empty. Any transmit task written to the modem after IBEMPTY goes to a logic '1' will be too late to avoid a gap in the transmit output signal (see Figure 18 and Table 3, Tx Task Timing)
IBEMPTY is also set to a logic '1' by a RESET task and by a change of the Mode Register's Tx/Rx bit, but in this case the IRQ bit will not be set.
IBEMPTY is cleared to a logic '0' within 1-symbol time after a task other than NULL or RESET is written to the Command Register.
Note that when the modem is in the transmit mode and the Interleave Buffer is empty, a mid-level (half-way between '+1' and '-1') will be fed to the RRC Filter.
In Receive mode this bit is a logic '0'.

Status Register .....

B4 DIBOVF	**De-Interleave Buffer Overflow. In Receive Mode** DIBOVF is set to a logic '1' (also setting the IRQ bit) when an RHB, RILB, RSID or R4S task is written to the Command Register too late to allow continuous reception (see Figure 19 and Table 3 Rx Task Timing). DIBVOF is cleared to a logic '0' by reading the Status Register, by writing a RESET task to the Command Register or by changing the Tx/Rx bit of the Mode Register. **In Transmit mode** this bit is a logic '0'.
B3 CRCERR	**CRC Checksum Error. In Receive Mode** CRCFEC will be updated at the end of an SFP, RSID, RHB, or RILB task to reflect the result of the receive CRC check. A logic '0' indicates that the CRC was received correctly. A logic '1' indicates that an error is present. Note that this bit should be ignored when an 'Intermediate' Block (which does not have an integral CRC) is received. CRCERR is cleared to a logic '0' by a RESET task, or by changing the Tx/Rx bit of the Mode Register. **In Transmit mode** this bit is a logic '0'.
B2 SRDY	**'S' Symbol Ready. In Receive Mode** this bit is set to a logic '1 whenever an 'S' symbol has been received. The µController may then read the value of the symbol from the SVAL field of the Status Register. **In Transmit mode** this bit is set to a logic '1' whenever an 'S' symbol has been transmitted. This bit is cleared to a logic '0' immediately after a read of the Status Register, by a RESET task or by changing the TX/Rx bit of the Mode Register.
B1, B0 SVAL	**Received 'S' Symbol Value. In Receive Mode** these two bits reflect the value of the latest received 'S' symbol. **In Transmit mode** these two bits will be logic '0's'.

The Data Quality Register

In Receive Mode, the modem continuously measures the quality of the received signal by comparing the actual received waveform over the previous 64 symbol times against an internally generated "ideal". The result is placed into bits 3 to 7 of the Data Quality Register for the µController to read at any time, bits 0 to 2 being always set to '0'. Figure 23 shows how the value (0 to 255) read from the Data Quality Register varies with the received signal-to-noise ratio.

In Transmit mode, and for 64 symbol-times after enabling Receive mode, the value will be invalid.

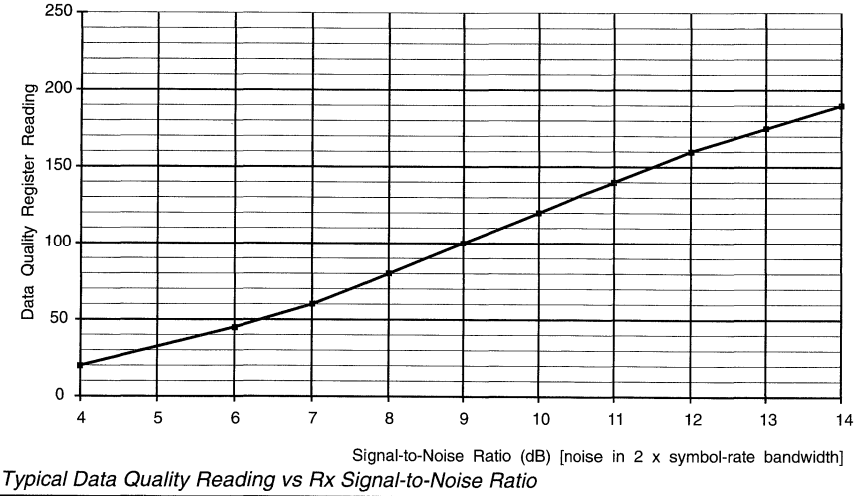


Fig.23 Typical Data Quality Reading vs Rx Signal-to-Noise Ratio

Programming Information .....

Registers

This diagram may provide a useful quick-reference to FX929 register allocations.

Register Selection

Write to Modem	A_1	A_0	Read from Modem
Data Block Buffer	0	0	Data Block Buffer
Command Register	0	1	Status Register
Control Register	1	0	DQ Register
Mode Register	1	1	not used

Command Register

7	6	5	4	3	2	1	0

AQSC AQLEV set to '0' '0' '0' (Reserved) TASK

AQSC - Acquire Symbol Clock
AQLEV - Acquire Receive Signal Levels
TASK:

B2	B1	B0	Rx Mode	
0	0	0	NULL	
0	0	1	SFP	Search For Frame Preamble
0	1	0	RHB	Read Header Block
0	1	1	RILB	Read Intermediate or Last Block
1	0	0	SFS	Search For Frame Sync
1	0	1	R4S	Read 4 Symbols
1	1	0	RSID	Read Station ID
1	1	1	RESET	Cancel any Current Action

B2	B1	B0	Tx Mode	
0	0	0	NULL	
0	0	1	T24S	Transmit 24 Symbols
0	1	0	THB	Transmit Header Block
0	1	1	TIB	Transmit Intermediate Block
1	0	0	TLB	Transmit Last Block
1	0	1	T4S	Transmit 4 Symbols
1	1	0	TSID	Transmit Station ID
1	1	1	RESET	Cancel any Current Action

Control Register

7	6	5	4	3	2	1	0

CKDIV FSTOL LEVRES PLLBW

CKDIV - Clock Division Ratio
FSTOL - Frame Sync Tolerance
LEVRES - Level Measurement Response Time

B3	B2	
0	0	Hold
0	1	Slow Peak Detect
1	0	Lossy Peak Detect
1	1	Clamp

PLLBW - PLL Bandwidth

B1	B0	Mode	+/-ppm
0	0	Hold	0
0	1	Narrow	20
1	0	Medium	100
1	1	Wide	650

Mode Register

7	6	5	4	3	2	1	0

IRQEN INVSYM Tx/$\overline{Rx}$ RxEYE (Reserved set to '0') SSIEN SSYN

IRQEN - IRQ Output Enable
INVSYM - Invert Symbol
Tx/Rx - Transmit or Receive Mode
RxEYE - Show Rx Eye
SSIEN - 'S' Symbol IRQ Enable
SSYM - 'S' Symbol to be Transmitted

Status Register

7	6	5	4	3	2	1	0

IRQ BFREE IBEMPTY DIBOVF CRCERR SRDY SVAL

IRQ - Interrupt Request
BFREE - Data Block Buffer Free
IBEMPTY - Interleave Buffer Empty
DIBOVF - De-Interleave Buffer Overflow
CRCERR - CRC Checksum Error
SRDY - 'S' Symbol Ready
SVAL - Received 'S' Symbol Value

Fig.24 Ready-Use Guide to Register Functions

Operational Information

"Transmit Frame" Example

The operations needed to transmit a single Frame consisting of Symbol and Frame Sync sequences and one each Station ID, Header, Intermediate and Last blocks are shown below.

Sequence Explanation

Prerequisites:

Ensure that the Control Register has been loaded with a suitable CKDIV value, and that the IRQEN and Tx/Rx bits of the Mode Register are '1', the RxEYE and SSIEN bits are '0' and the INVSYM bit is set appropriately-

Steps

1	Read Status Register to ensure BFREE = '1'	BFREE = '1'
2	Write 6 Symbol Sync bytes to the Data Block Buffer - and a Transmit 24 Symbols task to the Command Register -	Write to Data Block Buffer T24S
3	Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ BFREE = '1' IRQ = '1'
4	Write 6 Frame Sync bytes to the Data Block Buffer - and a Transmit 24 Symbols task to the Command Register -	Write to Data Block Buffer T24S
5	Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ BFREE = '1' IRQ = '1'
6	Write 3 Station ID bytes to the Data Block Buffer - and a Transmit Station ID task to the Command Register -	Write to Data Block Buffer TSID
7	Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ BFREE = '1' IRQ = '1
8	Write 10 Header Block bytes to the Data Block Buffer - and Transmit Header Block task to the Command Register -	Write to Data Block Buffer THB
9	Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ BFREE = '1' IRQ = '1'
10	Write 12 Intermediate Block bytes to the Data Block Buffer - and a Transmit Intermediate Block task to the Command Register -	Write to Data Block Buffer TIB
11	Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ BFREE = '1' IRQ = '1'
12	Write 8 Last Block bytes to the Data Block Buffer - and a Transmit Last Block task to the Command Register -	Write to Data Block Buffer TLB
13	Wait for Interrupt - Read Status Register, check that the IRQ and BFREE bits are '1' -	IRQ BFREE = '1' IRQ = '1'
14	Wait for another Interrupt - Read Status Register, check that the IRQ and BFREE and IBEMPTY bits are '1' -	IRQ BFREE = '1' IRQ = '1' IBEMPTY = '1"

Note that the final symbol of the frame will start to appear at the Tx Out pin approximately 2 symbol-times after the Status Register IBEMPTY bit goes to a '1'; a further 16 symbol-times should be allowed for the symbol to pass completely through the RRC Filter.The SSYM bits of the Mode Register may be altered at any time to change the transmitted 'S' symbols. If a timing reference is required, then setting the SSIEN bit to '1' will cause a µC interrupt after every 'S' symbol transmitted -in which case the µC will have to distinguish between interrupts caused by the BFREE bit going to '1', and those caused by the SRDY bit going to '1'.

Note that this example uses only the minimum 24-symbol "Symbol Synchronisation" pattern. Overall performance may be improved by increasing the length of the Symbol Synchronisation Sequence.

"Receive Frame" Example

The operations needed to receive a single frame consisting of Symbol and Frame Sync sequences and one each Station ID, Header, Intermediate and Last blocks are shown below.

Sequence Explanation	
Prerequisites: Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values, that the Mode Register IRQEN bit is '1' and the RxEYE, SSIEN and Tx/Rx bits are '0', and that the INVSYM bit is set appropriately. Wait until the received carrier has been present for at least 8 symbol-times.	
Steps	
1 Read Status Register and check that the IRQ and BFREE bits are '1' -	IRQ = '1' BFREE = '1'
2 Write a byte containing a Search for Frame Preamble task and with the AQSC and AQLEV bits set to '1' -	SFP (AQSC/AQLEV) = '1'
3 Wait for Interrupt - Read Status Register and check that the IRQ and BFREE bits are '1' -	IRQ IRQ = '1' BFREE = '1'
4 Check that the Status Register CRCERR bit was '0', then read 3 Station ID bytes from the Data Block Buffer -	CRCERR '0' Read from Data Block Buffer
5 Write a Read Header Block task to the Data Block Buffer -	RHB
6 Wait for Interrupt - Read Status Register and check that the IRQ and BFREE bits are '1' -	IRQ IRQ = '1' BFREE = '1'
7 Check the CRCERR bit was '0', then read 10 Header Block bytes from the Data Block Buffer -	CRCERR '0' Read from Data Block Buffer
8 Write a Read Intermediate or Last Block task to the Command Register -	RILB
9 Wait for Interrupt - Read Status Register and check that the IRQ and BFREE bits are '1'. (The state of the Status Register CRCERR bit should be ignored as this is an Intermediate Block) -	IRQ IRQ = '1' BFREE = '1'
10 Read 12 Intermediate Block bytes from the Data Block Buffer -	Read from Data Block Buffer
11 Write a Read Intermediate or Last Block task to the Command Register -	RILB
12 Wait for Interrupt - Read Status Register and check that the IRQ and BFREE bits are '1' -	IRQ IRQ = '1' BFREE = '1'
13 Check the CRCERR bit of the Status Register as '0' - and read the 8 Last Block bytes from the Data Block Buffer -	CRCERR = '0' Read from Data Block Buffer
Note: The value of the latest 'S' symbol received will be contained in the SVAL bits each time that the Status Register is read. If desired, the Mode Register SSIEN bit may be set to '1', which will cause a µC interrupt after every 'S' symbol is received -in which case the µC will have to distinguish between interrupts caused by the BFREE bit going to a '1', and those caused by the SRDY bit going to a '1'.	

Operational Information .....

Operation Details

Cyclic Redundancy Codes

CRC0

This is a six-bit CRC check code used in the Station ID Block. It is calculated by the modem from the first 24-bits of the block (bytes 0, 1 and 2) as follows:

The 24 bits are considered as the coefficients of a polynomial M(x) of degree 23, such that the MSB (bit 7) of byte 0 is the coefficient of x^{23}, and bit 0 of byte 2 is the coefficient of x^0.

The polynomial F(x) of degree 5 is calculated as being the remainder of the division

$$x^6 M(x)/(x^6 + x^4 + x^3 + 1)$$

where division is performed modulo-2.

The polynomial $x^5 + x^4 + x^3 + x^2 + x^1 + x^0$ is added (modulo-2) to F(x).

The coefficients of F(x) are placed in the 6-bit CRC0 field, such that the coefficient of x^5 corresponds to the MSB of CRC0.

CRC1

This is a sixteen-bit cyclic redundancy checksum which uses the generator polynomial: $X^{16} + X^{12} + X^5 + 1$

CRC2

This is a 32-bit cyclic redundancy checksum which uses the generator polynomial:

$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$

Interleaving

The 66 symbols of a 'Header', 'Intermediate' or 'Last' block are interleaved by the modem before transmission to give protection against noise bursts and short fades (the 22 symbols of a Station ID block are not interleaved).

In the receive mode, the modem de-interleaves the received symbols prior to decoding.

Forward Error Correction

Transmit Mode, the FX929 uses a Trellis Encoder to translate the 96 bits (12 bytes) of a Header, Intermediate or Last Block or the 30 bits of a Station ID Block into a 22 or 66-symbol sequence which includes FEC information.

Receive Mode, the FX929 decodes the received 22 or 66-symbol block into 30 or 96 bits of binary data using a Viterbi algorithm to take advantage of the encoded FEC information

Level Measurement and Clock Extraction

The FX929 is intended for use in systems where the Symbol Sync pattern is transmitted immediately on startup of the transmitter.

When the carrier is detected by the receiver or when the receiver is switched to another channel, the controlling µController should wait approximately 8 symbol-times for the received signal to propagate through the modem's RRC filter then issue a SFS or SFP task with the AQSC and AQLEV bits set to '1'.

The 8-symbol delay can usefully be included in the carrier detect circuitry.

Setting the AQSC and AQLEV bits to '1' triggers the modem's automatic Symbol Clock Extraction and Level Measurement acquisition sequences, which are designed to measure the received symbol timing, amplitude and dc offset as quickly as possible during the Symbol Sync period before switching to more accurate - but slower - measurement modes for the remainder of the received message. Note that if the acquisition sequences are triggered after the Symbol Sync period - as can happen when the receiver is switched to another channel- they will still function correctly, but will take longer to acquire accurate level and timing information.

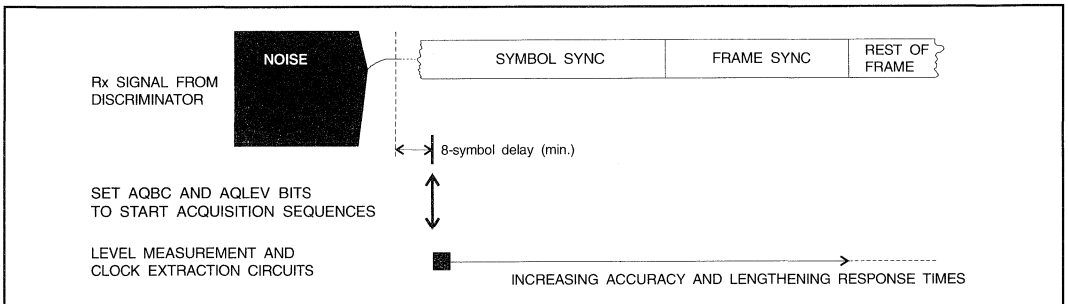


Fig.25 Symbol-Clock and Level Acquisition Example

The operation of the Level Acquisition Sequence depends on the settings of the Control Register LEVRES bits:

LEVRES Setting ---	B3	B2	Details of Level Acquisition Sequence
'Hold'	0	0	1 symbol-time of 'Clamp' mode then 15 symbol-times of 'Lossy Peak Detect' mode before reverting to 'Hold' mode
'Slow Peak Detect'	0	1	1 symbol-time of 'Clamp' mode then 15 symbol-times of 'Lossy Peak Detect' mode before reverting to 'Slow Peak Detect' mode
'Lossy Peak Detect'	1	0	1 symbol-time of 'Clamp' mode before reverting to 'Lossy Peak Detect' mode
'Clamp'	1	1	Remain in 'Clamp' mode

The 1-symbol 'Clamp' time at the start of these sequences is used to make an initial measurement of the dc offset present on the received signal, after which the 'Lossy Peak Detect' period is used to estimate the signal amplitude.

The operation of the Symbol Clock Acquisition Sequence depends on the settings of the Control Register PLLBW bits:

PLLBW Setting ---	B1	B0	Details of Symbol Clock Acquisition Sequence
'Hold'	0	0	16 symbol-times of 'Extra-wide BW mode' followed by 30 symbol-times of 'Wide BW' mode before reverting to 'Hold' mode
'Narrow Bandwidth'	0	1	16 symbol-times of 'Extra-wide BW mode' followed by 30 symbol-times of 'Wide BW' mode before reverting to 'Narrow BW' mode
'Medium Bandwidth'	1	0	16 symbol-times of 'Extra-wide BW mode' followed by 30 symbol-times of 'Wide BW' mode before reverting to 'Medium BW' mode
'Wide Bandwidth'	1	1	16 symbol-times of 'Extra-wide BW mode' before reverting to 'Wide BW' mode

The 'Extra-wide BW' PLL mode is designed to synchronise rapidly to the '+3 +3 -3 -3 ...' Symbol Sync pattern and is available only as part of an automatic acquisition sequence. Although not recommended, it is possible to use the FX929 in a non-standard system where there is an indeterminate delay between the transmitter startup and the Symbol Sync pattern, or where an Rx carrier detect signal is not available to the controlling µC. In these cases the Symbol Sync pattern should be extended to about 100 symbols, the Control Register LEVRES bits set to 'Lossy Peak Detect' and the PLLBW bits to 'Wide BW' before initating an 'SFS + AQSC + AQLEV' task. Once the Frame Sync pattern has been detected, the Control Register settings may be changed to 'Slow Peak Detect' and 'Medium' or 'Narrow' PLL BW for the remainder of the received message.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref. V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating temperature range: **FX929J4/L2**	-40°C to +85°C
Storage temperature range: **FX929J4/L2**	-40°C to +85°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Remarks	Min.	Max.	Unit
Supply Voltage (V_{DD})		4.5	5.5	V
Operating Temperature (T_{OP})		-40.0	+85.0	°C
Symbol Rate		2400	9600	symbols/sec
Xtal/Clock Frequency		1.0	10.0	MHz

Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 4.5 to 5.5V, T_{OP} = -40°C to +85°C. Xtal/Clock Frequency = 4.9152MHz.
Symbol Rate = 4800 symbols/sec.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
I_{DD}	1	-	5.0	-	mA
Tx Output					
Impedance	2	-	1.0	2.5	kΩ
Signal Level	3	0.8	1.0	1.2	Vp-p
Output DC Offset (wrt V_{DD}/2)	9	-0.25	-	0.25	V
Rx Input					
Impedance (Rx In pin)		-	10.0	-	MΩ
Rx Input Amp Voltage Gain		-	300	-	V/V
Input Signal Level	4	0.7	1.0	1.3	Vp-p
Input dc Offset (wrt V_{DD}/2)	4	-0.5	-	0.5	V
Xtal/Clock Input					
'High' pulse width	5	40.0	-	-	ns
'Low' pulse width	5	40.0	-	-	ns
Input Impedance		10.0	-	-	MΩ
Inverter Gain (I/P = 1mV rms @ 1kHz)		20.0	-	-	dB
µController Interface					
Input logic '1' level	6, 7	V_{DD} -1.5	-	-	V
Input Logic '0' level	6, 7	-	-	1.5	V
Input Leakage Current (V_{IN} = 0V to V_{DD})	6, 7	-5.0		+5.0	µA
Input Capacitance	6, 7	-	10.0	-	pF
Output Logic '1' Level (IOH = 120µA	7	V_{DD} -0.4			V
Output Logic '0' Level (IOL = 360µA)	7, 8	-	-	0.4	V
'Off' State Leakage Current (V = V_{DD})	8	-	-	10	µA

Specification .....

µController Interface Timings

Conditions: V_{DD} = 4.5 to 5.5V; T_{OP} = -40°C to +85°C; with a maximum load of 30pF to V_{SS} on pins D_0 to D7.

Description		Note	Min.	Typ.	Max.	Unit
t_{ACSL}	"Address Valid" to "CS Low" time		0	-	-	ns
t_{AH}	"Address Hold" time		0	-	-	ns
t_{CSH}	"CS Hold" time		0	-	-	ns
t_{CSHI}	"CS High" time		6.0	-	-	Xtal/Clock Cycles
t_{CSRWL}	"CS" to "WR" or "RD" Low time		0	-	-	ns
t_{DHR}	"Read-Data Hold" time		0	-	-	ns
t_{DHW}	Write-Data Hold time		0	-	-	ns
t_{DSW}	Write-Data Set-Up" time		90.0	-	-	ns
t_{RHCSL}	"RD High" to "CS Low" time (write cycle)		0	-	-	ns
t_{RACL}	"Read Access" time from "CS Low"		-	-	175	ns
t_{RARL}	"Read Access" time from "RD Low"		-	-	145	ns
t_{RL}	"RD" Low time		200	-	-	ns
t_{RX}	"RD High" to "D_0-D_7 3-State" time		-	-	50.0	ns
t_{WHCSL}	"WR High" to "CS Low" time (read cycle)		0	-	-	ns
t_{WL}	"WR" Low time		200	-	-	ns

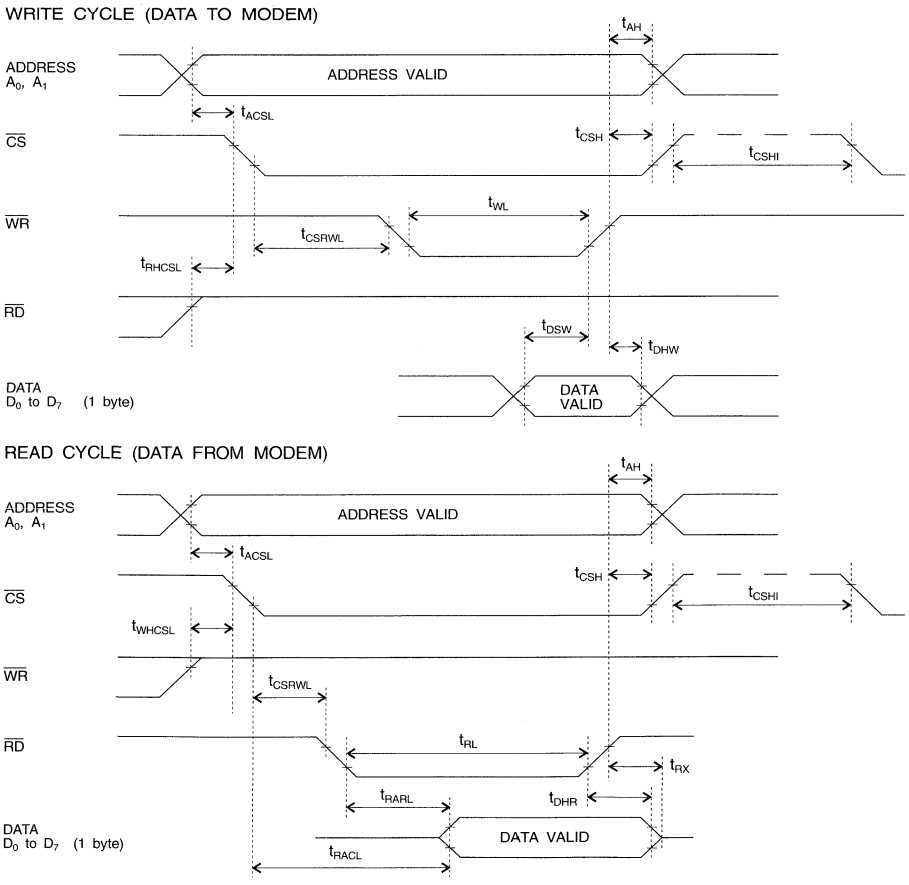


Fig.26 FX929 - µProcessor Interface Read/Write Timing

Notes Overleaf .....

Specification .....

Notes:

1. V_{DD} = 5.0V, T_{OP} = 25°C; not including any current drawn from the modem pins by external circuitry.
2. Small signal impedance at 1kHz.
3. Measured after the external CR filter, for a '+3 +3 -3 -3 +3 +3 -3 -3 ... symbol sequence; at V_{DD} = 5.0V (output level is proportional to V_{DD}).
4. For optimum performance, measured at the Rx Feedback pin, for a '+3 +3 -3 -3 +3 +3 -3 -3 ... symbol sequence.
5. Timing for an external input to the Xtal/Clock pin.
6. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A_0 and A_1 pins.
7. D_0 - D_7 pins.
8. $\overline{IRQ}$ pin.
9. Measured at the Tx Out pin with the modem in the Tx (idle) mode.

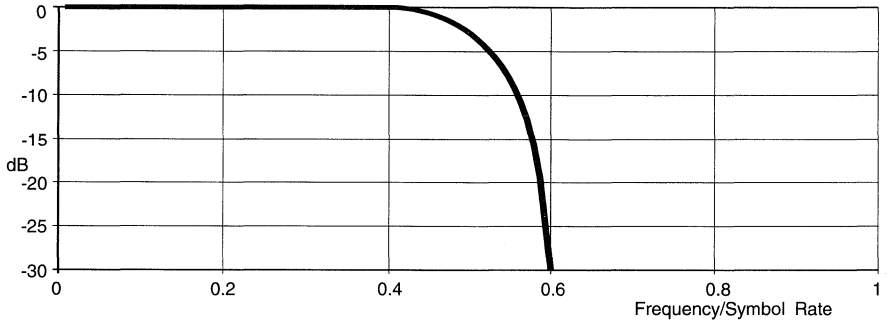


Fig.27 Frequency Response of RRC Tx Filter

Signal-to-Noise Performance

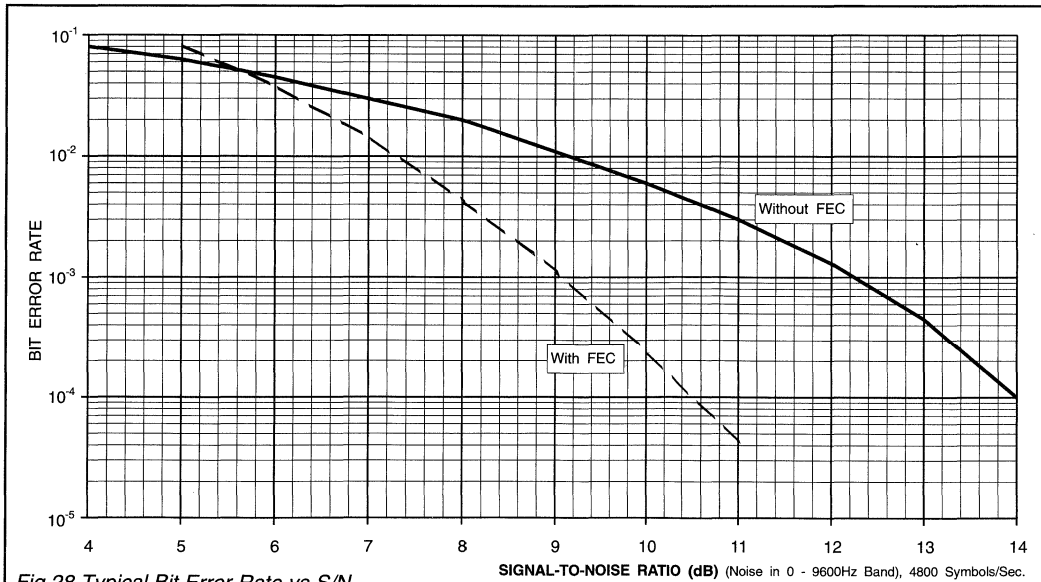


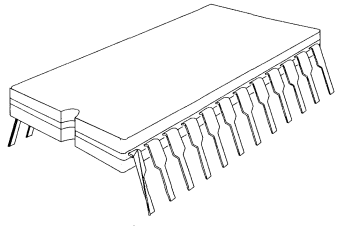
Fig.28 Typical Bit Error Rate vs S/N

Package Outlines

The FX929 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX929J4 24-pin cerdip DIL **(J)**

NOT TO SCALE



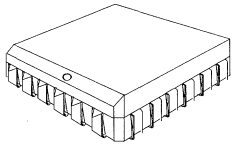
Max. Body Length 32.03mm
Max. Body Width 14.81mm

Handling Precautions

The FX929 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX929L2 24-lead plastic leaded chip carrier **(LS)**

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX929J4 28-pin cerdip DIL **(J)**

FX929L2 24-lead plastic leaded chip carrier **(LS)**

Integrated Circuits Data Book

Section 9

Voice Security/ Voice Coding

CML Semiconductor Products

PRODUCT INFORMATION

FX214 FX224

VSB* Audio Scrambler

Publication D/214/3 July 1994

Features/Applications

- *Variable Split-Band Frequency Inversion Voice Scrambler
- 32 Programmable Split Frequencies
- CTCSS HP Filter
- High Recovered Audio Quality
- Low-Power 5 Volt CMOS
- Half-Duplex Switching
- Powersave Facility
- Mobile or Cellular Radio Applications
- Fixed or Rolling Code Applications
- Serial/Parallel Load Options: FX214 (Serial), FX224 (Parallel),
- DIL and SMD Package Options

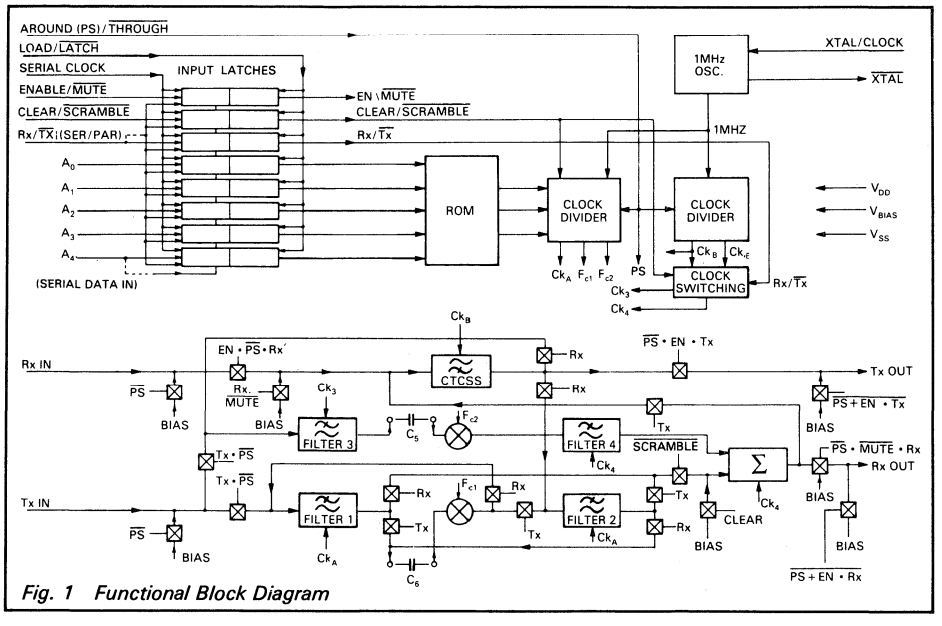


Fig. 1 Functional Block Diagram

Brief Description

The FX214 and 224 are low-power CMOS LSI devices designed as Variable Split-Band (VSB) voice scramblers.

The device uses separate Rx and Tx paths which are switched for half-duplex operation. To prevent interference from sub-audio products, an on-chip Continuous Tone Controlled Squelch System (CTCSS) highpass filter is automatically switched to the input in Rx and to the output in Tx.

Scrambling is achieved by splitting the input voice frequencies into upper and lower frequency bands using switched capacitor filters, modulating each band with selected carrier frequencies to "frequency invert" the bands and then summing the output.

A total of 32 different split-point and carrier frequency combinations are externally programmable using a 5-bit code; this code can be either fixed or varying (rolling), for greater security.

'Sync/Speech Mute', 'Powersave', 'Clear' and 'Audio-Bypass' facilities are controlled via external commands.

Timing and filter clocks are derived internally from an on-chip oscillator requiring only an external 1MHz Xtal or clock pulse input.

This device demonstrates high baseband and carrier frequency rejection with good 'recovered audio' quality. Serial or parallel command loading functions are available in both DIL and SMD Packages

Pin Functions

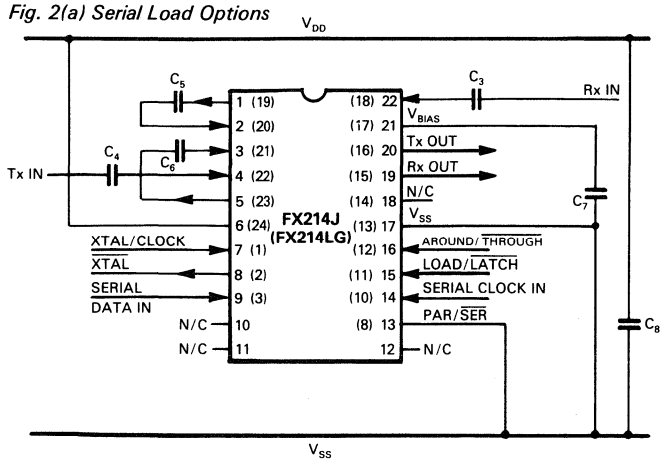
FX 214J	FX 214LG 214L2	FX 224J	FX 224LG 224LS	
7	1	1	1	**Xtal/Clock:** Input to the clock oscillator inverter. A 1MHz Xtal input or externally derived 1MHz clock is injected here. See Figure 2.
8	2	2	2	**$\overline{\text{Xtal}}$:** Output of the clock oscillator inverter.
9	3			**Serial Data Input:** This pin is used, on devices wired in the serial loading mode, to input an 8- bit word representing the digital control functions. This word is loaded using the serial data clock and is input in the following sequence: ENABLE; CLEAR; Rx/Tx; A_0; A_1; A_2; A_3; A_4, with the Load/Latch being operated on completion. See Timing Diagram Figure 7.
		3	3	**A_4:** **Programming Inputs:** In parallel mode, these are the 5 digital inputs
		4	4	**A_3:** whose code defines the split point frequency and the High and Low band
		5	5	**A_2:** carrier frquencies. Each of the 5 input pins have a 1MΩ internal pullup
		6	6	**A_1:** resistor. Table 2 contains programming information .
		7	7	**A_0:**
		8	8	**Rx/$\overline{\text{Tx}}$:** This digital input selects the Receive or Transmit paths and configures Upperband and Lowerband filter bandwidths whilst setting the CTCSS High Pass Filter position in the signal path. See Table 1 and Figures 5 and 6. 1MΩ internal pullup resistor [Rx].
13	8			**Parallel/$\overline{\text{Serial}}$:** This pin defines the loading mode of the digital function inputs. In the parallel load devices this pin has no external connections. For serial load devices this pin must be externally conected to V_{SS}. This pin on all devices has an 1MΩ internal pullup resistor.
		9	9	**Clear/$\overline{\text{Scramble}}$:** This digital input puts the device 'Clear' or 'Frequency Inversion' mode by controlling the application of carrier frequency to the upper and lower band balanced modulators. In 'Scramble' the balanced modulator carrier frequency values are selected by the split point address A_0 - A_4 [Table 2]. In 'Clear' carriers are turned off and the balanced modulators are bypassed internally, the lower band is not added to the output signal. 1MΩ internal resistor [Clear].
		10	10	**Enable/$\overline{\text{Mute}}$:** This digital function is used to disable receive or transmit signal paths for rolling code synchronization whilst maintaining bias conditions. To allow synchronizing information to be transmitted, or receiver audio output to be removed during sync periods, a logic '1' will enable' a logic '0' will disable the selected [Rx/Tx] audio path. See Table 1. 1MΩ internal pullup resistor.
14	10			**Serial Clock Input:** The externally applied data clock frequency used to shift input data along on devices wired in the Serial loading mode. One full data clock cycle is required to shift one data bit completely into the register. See Timing Diagram Figure 7. This pin has a 1MΩ internal pullup resistor.
15	11	11	11	**Load/$\overline{\text{Latch}}$:** Controls the loading of the 8 digital function inputs: ENABLE; CLEAR; Rx/Tx; A_0-A_4 into the internal register. When this pin is '1' all 8 inputs are transparent and new data acts directly. For controlled changing of parameters in the parallel mode Load/Latch must be kept at logic '0' whilst a new function is loaded, then Load/Latch strobed 0-1-0 to latch the inputs in. For serial loading the data should be loaded with Load/Latch at logic '0' and then Load/Latch strobed 0-1-0 on completion of data loading. 1MΩ internal pullup resistor. See Figure 7. NOTE: Serial and/or parallel loading functions are dependant upon device type.

Pin Functions

FX 214J	FX 214LG 214L2	FX 224J	FX 224LG 224LS	
16	12	12	12	**Around [Powersave]/Through:** This digital input is used, when logic '1' to put the device into a powersave condition where all parts of the device except the 1MHz oscillator circuits are shut down, and signal input and output lines made open-circuit, free of all bias. This allows signal paths to be routed externally around the device. whilst reducing current consumption. A logic '0' enables the device to work normally as shown in Table 1. 1MΩ internal pullup resistor.
17	13	13	13	**V_{SS}:** Negative Supply [GND].
18	14	14	14	Internally connected , leave open circuit .
19	15	15	15	**Rx Output:** The processed audio signal output. This pin is held at dc 'bias' voltage for all functions except Powersave. This buffered output is driven by the Summer circuit in the Rx mode. Signal paths and bias levels are detailed in the Table 1 and Figure 6.
20	16	16	16	**Tx Output:** The processed audio output for the transmission channel. This pin is held at a dc 'bias' for all functions except Powersave. This summed and buffered signal is passed through the CTCSS High Pass Filter to the output pin in the Tx mode. Signal paths and bias levels are detailed in Table 1 and Figure 5.
21	17	17	17	**V_{BIAS}:** Normally at $V_{DD}/2$ this pin requires an external decoupling capacitor to V_{SS}.
22	18	18	18	**Rx Input:** The analogue received audio signal input. This pin is held at a dc 'bias' voltage by a 300kΩ on-chip bias resistor which is selected for all functions except Powersave, and therefore requires to be connected to external circuitry by a capacitor, C_3. See Figure 2. This input is routed through the CTCSS High Pass Filter in Rx mode to remove sub-audio frequencies from the voiceband. Signal paths and bias levels are detailed in Table 1 and Figure 6.
1	19	19	19	**Highband Filter Output:** The output of the Input Filter of the Upperband arm. The Rx/Tx function sets the lowpass filter at 3400Hz or 2700Hz respectively. This output must be connected to the Highband Balanced Modulator input via capacitor C_5. See Figure 2.
2	20	20	20	**Highband Balanced Modulator Input:** The input to the Balanced Modulator of the Upperband arm. This input must be connected to the Highband Filter Output via capacitor C_5.
3	21	21	21	**Lowband Balanced Modulator Input:** The input to the Balanced Modulator of the Lowerband arm. This input must be connected to the Lowerband Filter Output with capacitor C_6.
4	22	22	22	**Tx Input:** This is the analogue 'Clear' audio input for the VSB scrambler. This pin is held at a dc 'bias' voltage by a 300KΩ on-chip bias resistor which is selected for all functions except Powersave, and therefore requires to be connected to external circuitry by C_4. This input, in the Tx mode, is connected to Upper and Lowerband input filters, signal paths and bias levels are detailed in Table 1 and Figure 5.
5	23	23	23	**Lowband Filter Output:** The output of the Input Filter of the Lowerband arm, the Rx/Tx function determines which filter is used [Filter 1 or 2]. Figures 5 and 6. This output must be connected to the Lowerband Balanced Modulator Input via C_6.
6	24	24	24	**V_{DD}:** A single + 5V supply is required.

Component Connections

Fig. 2(a) Serial Load Options

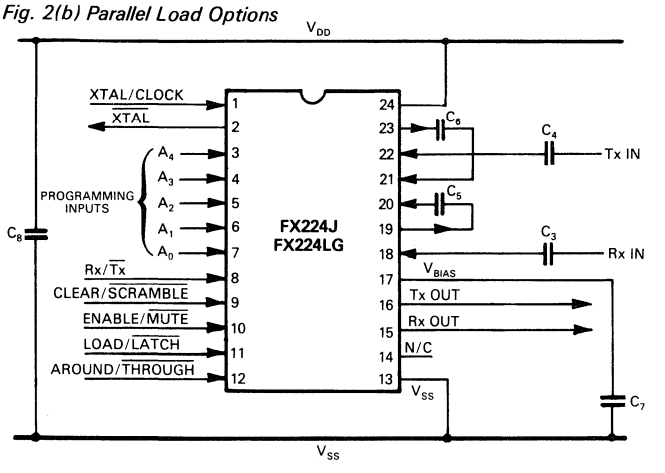


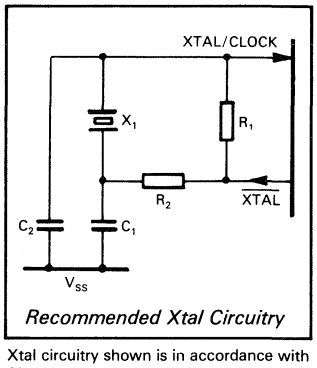
Not Connected

FX214J	10, 11, 12, 18*
FX214LG	4, 5, 6, 7, 9, 14*
FX224J	14*
FX224LG	14*

*Internally connected, do not connect to.

Fig. 2(b) Parallel Load Options





Recommended Xtal Circuitry

Xtal circuitry shown is in accordance with CML Application Note D/XT/1 April '86.

Component References	
Component	**Unit Value**
R_1	1M
R_2	Selectable
C_1	33p
C_2	68p
C_3	15n
C_4	15n
C_5	1.0μ
C_6	1.0μ
C_7	1.0μ
C_8	1.0μ
X_1	1MHz

Tolerance Resistors ± 10%
Capacitors ± 20%

C_5 and C_6 are coupling capacitors between filter outputs and balanced modulator inputs.

Fig. 2 External Component Connections

Application Information

This device can be used in 'Scramble' (frequency inversion) or 'Clear' speech modes. The inversion frequencies, when selected are controlled by the ROM address code (table 2). Keeping the code in one state (fixed) is the simplest form of operation. A more secure method is to continually change the ROM address code (rolling code) therefore changing split-point and carrier frequencies. This method requires some external form of code change generation with synchronization between transmit and receive stations. Many variations of code sequence are possible.

The recommended external component connections are shown in figure 2. In the Scramble mode, Split-point and Low and High band carrier frequencies (F_c1, F_c2) are selected and set in accordance with the ROM address code present at the inputs A_0 to A_4, *See Table 2.*

During the Clear speech function both Lower and Upperband filter arms are selected (figures 5 or 6), the carrier frequencies are turned off and the balanced modulators are bypassed internally. The Low band audio is removed from the output signal prior to summation.

Enable/$\overline{\text{Mute}}$

To enable code synchronization to be transmitted the speech output can be interrupted with the Enable/$\overline{\text{Mute}}$ function. A logic '0' will isolate the whole device whilst leaving the audio input and output pins at bias level. *See Table 1.*

Powersave

When the Around/$\overline{\text{Through}}$ function is at a logic '1' the device is in the powersave condition. Audio signals may be hardwired around the device normally as the input and output pins are open circuit. *See Table 1.*

Effect of Chosen Function on Inputs and Outputs		CHOSEN FUNCTION			
		Rx = '1'	$\overline{\text{Tx}}$ = '0'	$\overline{\text{Mute}}$ = '0'	Around (Powersave) = '1'
Rx Input	Path	Enabled	Disconnect	Disconnect	High Impedance
	Level	Bias	Bias	Bias	
Rx Output	Path	Enabled	Disconnected	Disconnect	High Impedance
	Level	Bias	Bias	Bias	
Tx Input	Path	Disconnected	Enabled	Enabled	High Impedance
	Level	Bias	Bias	Bias	
Tx Output	Path	Disconnected	Enabled	Disconnected	High Impedance
	Level	Bias	Bias	Bias	

Table 1 Functions Influencing Signal Paths

ROM Address A_4-A_0	Split Point Hz	Low Band Carrier, Hz f_{c1}	High Band Carrier, Hz f_{c2}
0 0 0 0 0	2800	3105	6172
0 0 0 0 1	2625	2923	6024
0 0 0 1 0	2470	2777	5813
0 0 0 1 1	2333	2631	5681
0 0 1 0 0	2210	2512	5555
0 0 1 0 1	2100	2403	5494
0 0 1 1 0	2000	2304	5376
0 0 1 1 1	1909	2212	5263
0 1 0 0 0	1826	2127	5208
0 1 0 0 1	1750	2049	5102
0 1 0 1 0	1680	1984	5050
0 1 0 1 1	1555	1858	4950
0 1 1 0 0	1448	1748	4807
0 1 1 0 1	1354	1655	4716
0 1 1 1 0	1272	1572	4629
0 1 1 1 1	1200	1501	4587

ROM Address A_4-A_0	Split Point Hz	Low Band Carrier, Hz f_{c1}	High Band Carrier, Hz f_{c2}
1 0 0 0 0	1135	1436	4504
1 0 0 0 1	1050	1351	4424
1 0 0 1 0	976	1278	4347
1 0 0 1 1	913	1213	4310
1 0 1 0 0	857	1157	4273
1 0 1 0 1	792	1094	4166
1 0 1 1 0	736	1037	4132
1 0 1 1 1	688	988	4065
1 1 0 0 0	636	936	4032
1 1 0 0 1	591	891	3968
1 1 0 1 0	552	853	3937
1 1 0 1 1	512	813	3906
1 1 1 0 0	471	772	3846
1 1 1 0 1	428	728	3816
1 1 1 1 0	388	688	3787
1 1 1 1 1	350	650	3731

Table 2 ROM Address Programming Table

Application Information

For the following descriptions, the term 'FX214' can be taken to mean FX214 or FX224.

Audio Quality

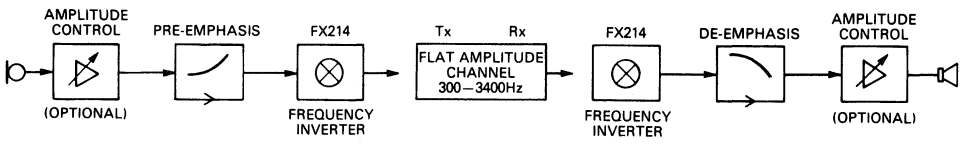


Fig. 3 · Recommended Basic Communication Audio System Layout

Figure 3 shows the recommended basic audio system layout using added pre- and de-emphasis circuitry to maintain good recovered speech quality. In the Transmit mode *Do Not* pre-emphasise the audio output of the FX214. In the Receive mode de-emphasis should be used after the FX214.

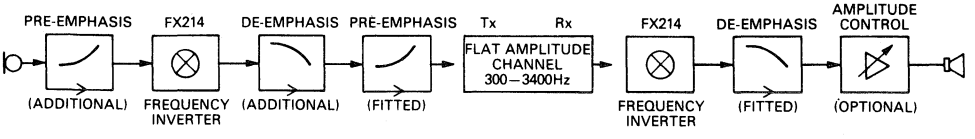


Fig. 4 Recommended Basic Radio Communication Audio System Layout

Figure 4 shows the recommended basic audio system layout if it is necessary to install the FX214 within a radio having pre- and de-emphasis circuitry as a standard. This is where post-emphasis access is not possible in the transmitter.

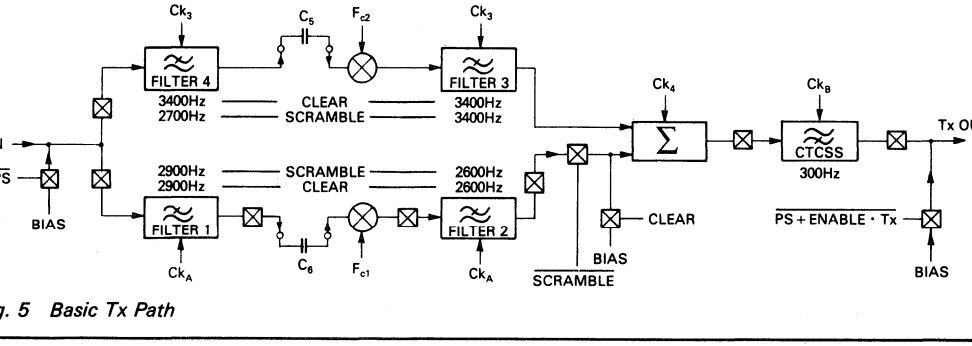


Fig. 5 Basic Tx Path

During the Transmit function the Low Pass and CTCSS filters are configured automatically as shown in Figure 5, with cut-off frequencies (-3dB) indicated.

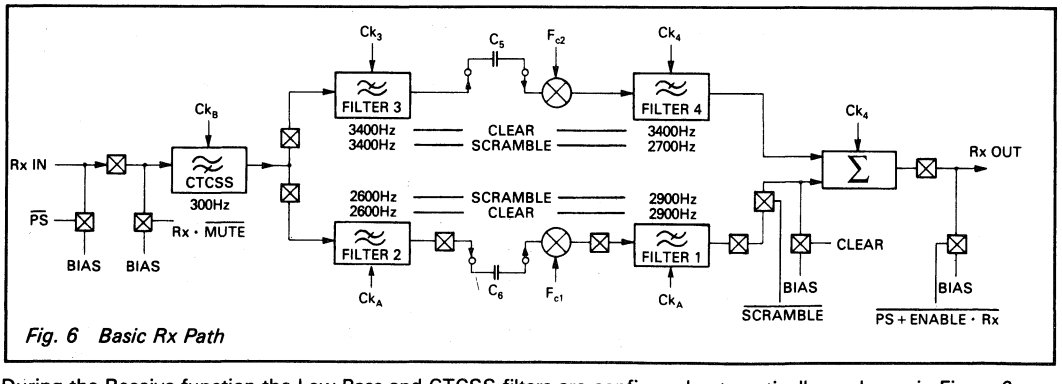


Fig. 6 Basic Rx Path

During the Receive function the Low Pass and CTCSS filters are configured automatically as shown in Figure 6, with cut-off frequencies (-3dB) indicated.

Electrical Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Sink/source current (supply pins)		± 30mA
(other pins)		± 20mA
Total device dissipation @ 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	FX214J/224J	−30°C to +85°C (Ceramic)
	FX214LG/224LG	−30°C to +70°C (Plastic)
Storage temperature range:	FX214J/224J	−55°C to +125°C (Ceramic)
	FX214LG/224LG	−40°C to +85°C (Plastic)

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5.0V, T_{amb} = 25°C, F_{clk} = 1.0MHz, Audio Level Ref: 0dB = 775mVrms.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply voltage		4.5	5	5.5	V
Supply current (Enabled)		—	8	—	mA
Supply current (Powersave)		—	1.2	—	mA
Analogue Input Impedances					
Tx/Rx Input (Enabled)		—	100	—	kΩ
Tx/Rx Input (Powersave)		1	—	—	MΩ
Balanced Modulator		—	40	—	kΩ
Analogue Output Impedances					
Rx Output (Tx Mode)		—	100	—	kΩ
Rx Output (Rx Mode)		—	—	2	kΩ
Rx Output (Powersave)		1	—	—	MΩ
Tx Output (Tx Mode)		—	—	2	kΩ
Tx Output (Rx Mode)		—	100	—	kΩ
Tx Output (Powersave)		1	—	—	MΩ
Input LPF		—	—	1	kΩ
Digital Values					
Digital Input Impedance		100	—	—	kΩ
Dynamic Values					
Input Logic '1'		3.5	—	—	V
Input Logic '0'		—	—	1.5	V
Xtal/Clock Frequency		—	1	—	MHz
Analogue Input Level		−18	—	+6	dB
Carrier Breakthrough	1	—	−55	—	dB
Baseband Breakthrough	1, 2 or 3	—	−33	—	dB
Filter Clock Breakthrough	1, 2 or 3	—	−50	—	dB
Output Noise	1, 4	—	−45	—	dB
Passband Characteristics					
Clear Mode	7				
Passband Gain		—	0	—	dB
Output Lower 3dB Point (Rx or Tx)		—	300	—	Hz
Output Upper 3dB Point (Rx or Tx)		—	3400	—	Hz
Scramble-Descramble	5				
Received Signal Passband Gain	6	—	0	—	dB
Received Signal Lower 3dB Point		—	400	—	Hz
Received Signal Upper 3dB Point		—	2700	—	Hz
Transmitted Signal Lower 3dB Point		—	300	—	Hz
Transmitted Signal Upper 3dB Point		—	3400	—	Hz
CTCSS (Highpass Filter)					
−3dB Point		—	300	—	Hz
Passband Gain		—	0	—	dB
Stopband Attenuation at f>250 Hz		—	40	—	dB

Electrical Specifications...

Characteristics	See Note	Min.	Typ.	Max.	Unit
Timing *(Figure 7)*					
Serial Mode Enable Set Up (t_{SMS})		250	—	—	ns
Serial Clock 'High' Pulse Width (t_{PWH})		250	—	—	ns
Serial Clock 'Low' Pulse Width (t_{PWL})		250	—	—	ns
Data Set Up Time (t_{DS})		150	—	—	ns
Data Hold Time (t_{DHS})		50	—	—	ns
Load/$\overline{\text{Latch}}$ Set Up Time (t_{LL})		250	—	—	ns
Load/$\overline{\text{Latch}}$ Pulse Width (t_{LLW})		150	—	—	ns
Data Set Up Time (t_{DSP})		150	—	—	ns
Data Hold Time (t_{DHP})		20	—	—	ns

Notes:
1. *Measured at the output of a single device.*
2. *Tx Mode.*
3. *Rx Mode.*
4. *With input A.C. short-circuited to V_{SS}.*
5. *Measured at the output of a receiving device in a scrambler-descrambler system with a transmission channel having a flat amplitude response and a bandwidth of 300Hz to 3400Hz and measured relative to the input signal at the transmitting device.*
6. *Excluding split point ± 150Hz.*
7. *Measured at the Rx or Tx output pin of a single device.*

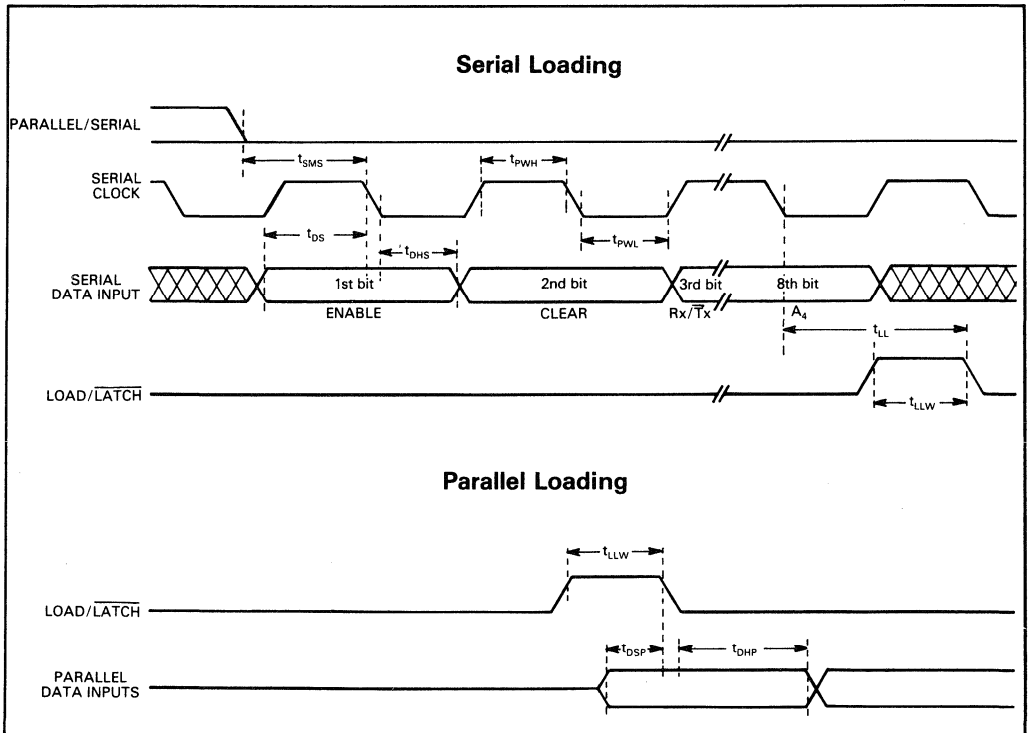


Fig. 7 Loading Timing Diagram

Package Outlines

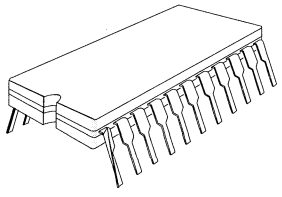
The FX214 and FX224 are available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX214 and FX224 are CMOS LSI circuits which include input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX214J 22-pin cerdip DIL (J3)

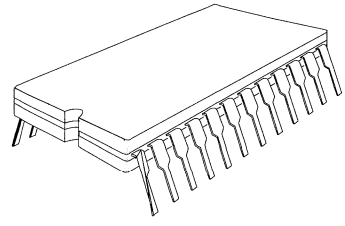
NOT TO SCALE



Max. Body Length 27.38mm
Max. Body Width 9.75mm

FX224J 24-pin cerdip DIL (J4)

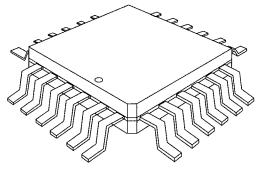
NOT TO SCALE



Max. Body Length 32.03mm
Max. Body Width 14.81mm

FX214LG/224LG 24-pin quad plastic encapsulated bent and cropped (L1)

NOT TO SCALE

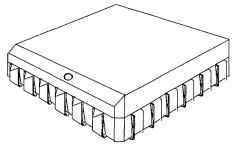


Max. Body Length 10.25mm
Max. Body Width 10.25mm

Package Outlines .....

FX214L2/224LS 24-lead plastic leaded chip carrier

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX214J	22-pin cerdip DIL	(J3)
FX214LG	24-pin quad plastic encapsulated bent and croppped	(L1)
FX214L2	24-lead plastic leaded chip carrier	
FX224J	24-pin cerdip DIL	(J4)
FX224LG	24-pin quad plastic encapsulated bent and croppped	(L1)
FX224LS	24-lead plastic leaded chip carrier	(L2)

CML Semiconductor Products

APPLICATION INFORMATION

Rolling Code Scrambling Using the FX224 VSB* Audio Scrambler

Publication AP/224 - Sc/1 April 1989

Features/Applications

- * Variable Split-Band
- High Quality Received Audio
- 6 Code "Hop Rates"
- 32 Different Split-Point/Carrier (Code) Combinations
- Half-Duplex System
- Pseudo-Random Codes

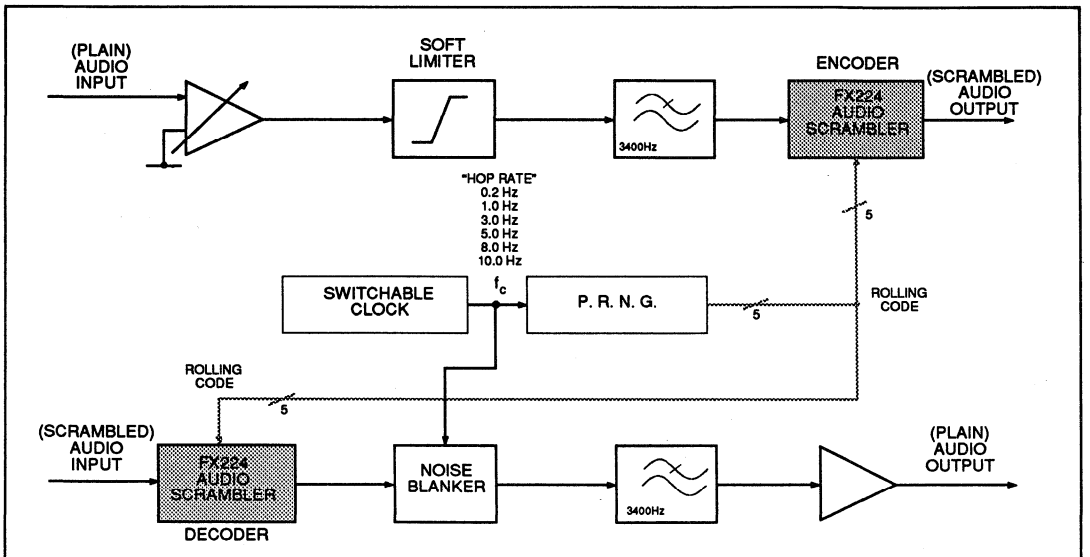


Fig.1 System Block Diagram

Introduction

The principle application of the FX224 *Variable Split-Band Audio Scrambler is that of a frequency domain speech-band inverter.

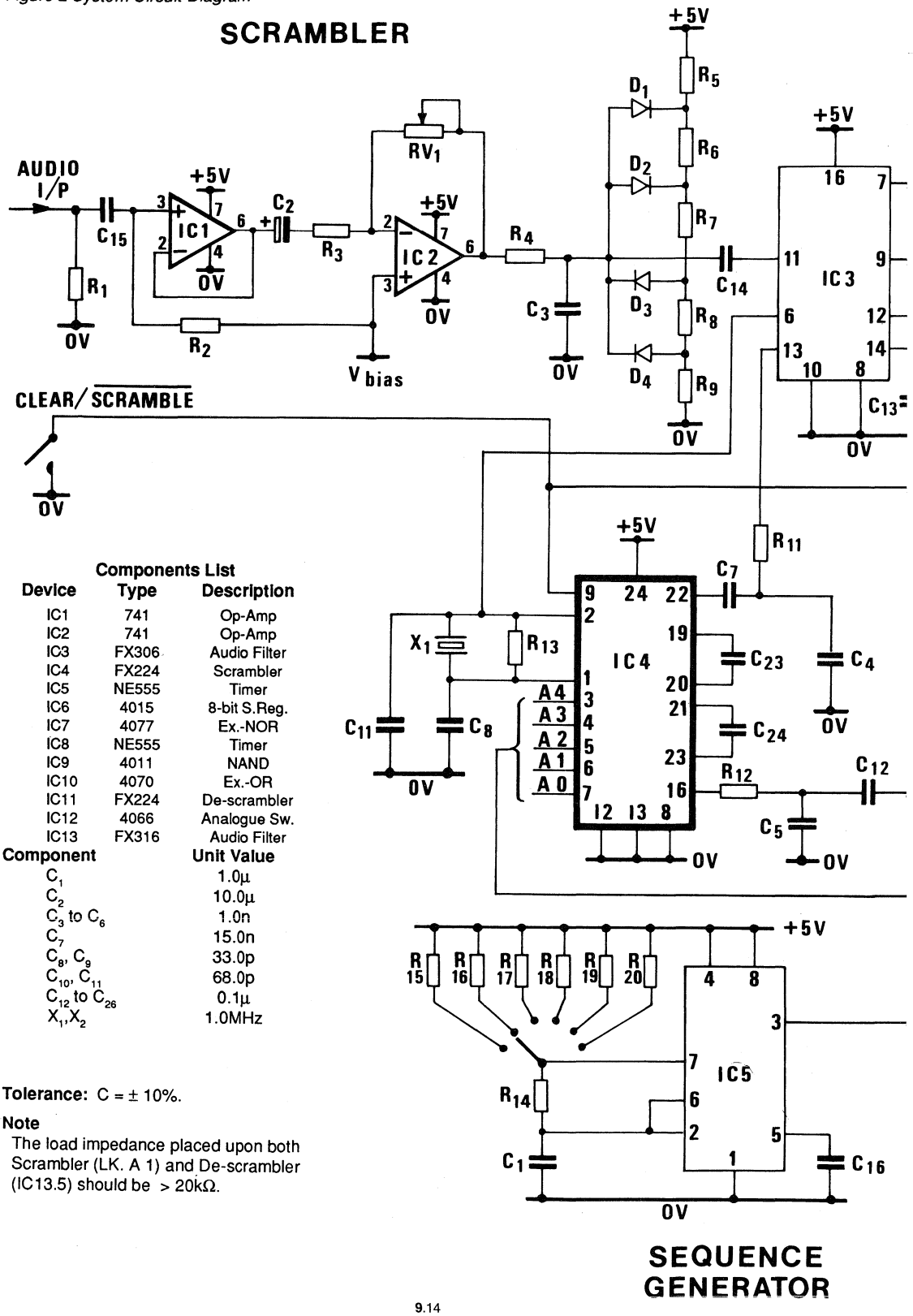
Scrambling is achieved by splitting the input voice frequencies into upper and lower frequency bands using switched capacitor filters, modulating each band with a separate carrier frequency to "frequency invert" the bands, then summing the output.
De-scrambling is carried out using the same method ensuring that the carrier frequencies are the same as those used to scramble the original audio.
Using the FX224 a total of 32 different split-point and carrier frequency combinations are externally programmable using a 5-bit code which can be fixed or varying (Rolling), for greater security.

This application note, used with a current FX224 Data Sheet, is intended to assist in integrating the device into audio circuitry by giving details of:

(a) The transmission (scramble) circuit.
(b) The reception (de-scramble) circuit.
(c) A Pseudo-Random Code Generator with switchable clock circuitry controlling the 'rolling' (change) rate of the 5-bit pseudo-random code at the rates of : 0.2Hz, 1.0Hz, 3.0Hz, 5.0Hz, 8.0Hz and 10.0Hz.

Synchronization of the scrambling and de-scrambling devices is important and can be accomplished by using either FSK data bursts or continuous outband tone signals.
The power requirement of this particular application is between 50 and 60 mA at 5 volts, per Tx/Rx pair, ie. one circuit.

Figure 2 System Circuit Diagram



Components List

Device	Type	Description
IC1	741	Op-Amp
IC2	741	Op-Amp
IC3	FX306	Audio Filter
IC4	FX224	Scrambler
IC5	NE555	Timer
IC6	4015	8-bit S.Reg.
IC7	4077	Ex.-NOR
IC8	NE555	Timer
IC9	4011	NAND
IC10	4070	Ex.-OR
IC11	FX224	De-scrambler
IC12	4066	Analogue Sw.
IC13	FX316	Audio Filter

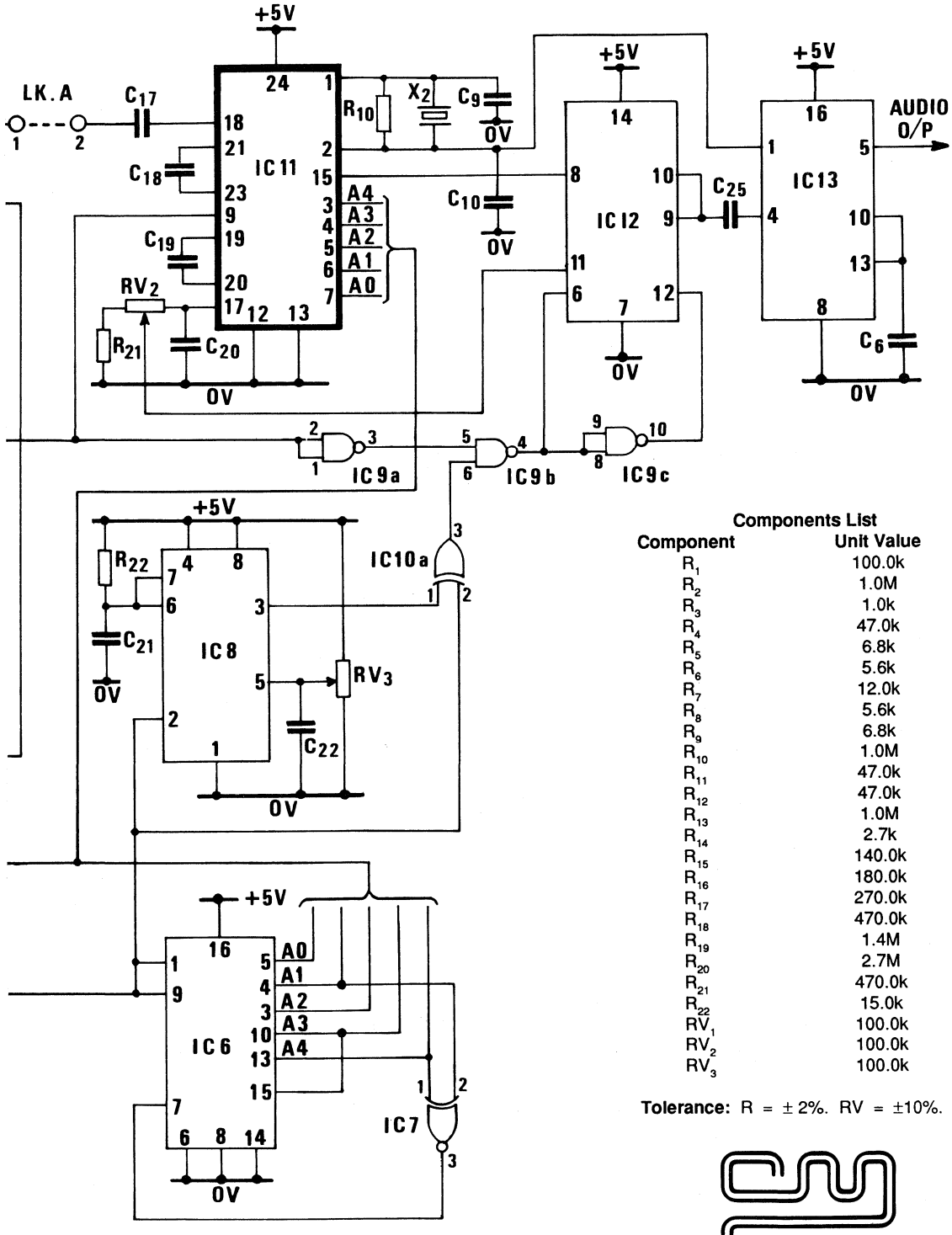
Component	Unit Value
C_1	1.0µ
C_2	10.0µ
C_3 to C_6	1.0n
C_7	15.0n
C_8, C_9	33.0p
C_{10}, C_{11}	68.0p
C_{12} to C_{26}	0.1µ
X_1,X_2	1.0MHz

Tolerance: C = ± 10%.

Note

The load impedance placed upon both Scrambler (LK. A 1) and De-scrambler (IC13.5) should be > 20kΩ.

DE-SCRAMBLER



Components List

Component	Unit Value
R_1	100.0k
R_2	1.0M
R_3	1.0k
R_4	47.0k
R_5	6.8k
R_6	5.6k
R_7	12.0k
R_8	5.6k
R_9	6.8k
R_{10}	1.0M
R_{11}	47.0k
R_{12}	47.0k
R_{13}	1.0M
R_{14}	2.7k
R_{15}	140.0k
R_{16}	180.0k
R_{17}	270.0k
R_{18}	470.0k
R_{19}	1.4M
R_{20}	2.7M
R_{21}	470.0k
R_{22}	15.0k
RV_1	100.0k
RV_2	100.0k
RV_3	100.0k

Tolerance: R = ±2%. RV = ±10%.

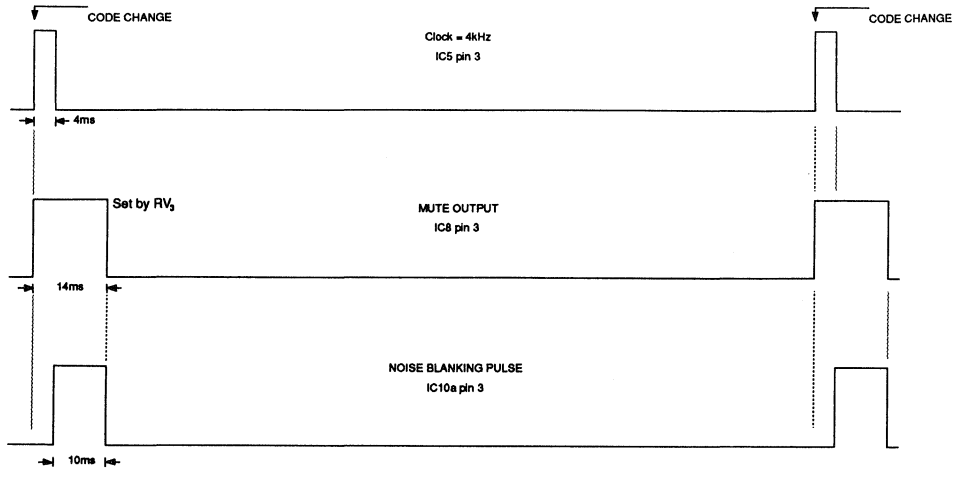


Fig.3 Receiver Timing

Timing

Figure 3 (above) shows the noise blanking pulse generation and its position relative to the code change. The blanking pulse width is variable using RV_2 (Figure 2).

The Circuit Diagram – *Figure 2* – is laid out as a Scramble/De-scramble evaluation circuit with the Scrambled (unintelligable) audio available at LK.A 1. The pseudo-random code is common to both functions.

The Scrambler Circuit

The incoming, plain, audio signal is buffered by IC1 and amplified by IC2. RV_1 sets a level of 300mV rms (this is found to be the optimum level to the FX224 in this application). Prior to the split-band frequency inversion process the signal is 'soft' limited to remove any high frequency spikes, then filtered to 3.4kHz by IC3 to simulate a radio channel voice bandwidth.
Using the 5-bit pseudo-random code generated by ICs 5, 6, & 7, the signal is frequency inverted by the FX224 (IC4). The inverted output of Variable Split-Band Scrambler is once again filtered (300Hz -3400Hz) by IC3, making the resulting scrambled audio compatible with a radio transmission channel. Scrambled (unintelligable) audio is available at LK.A 1.

The De-scrambler Circuit

Frequency inverted audio (LK.A 2) is recovered using the identical pseudo-random code to that used in the scrambling process.
As is the problem with most rolling code frequency inversion systems, unwanted transients are produced in the device, at the code change. In this application, a noise blanking circuit (ICs 8, 9, 10 & 12) is utilized to remove these transients by switching the output of the analogue switch (IC12) between the de-scrambling FX224 (IC11) and a d.c. level, at the code change, for a period determined by RV_3. The d.c. level is approximately 60mV below the FX224 V_{bias} line and is set by RV_2. Whilst the circuit is in the "Clear" mode, the noise blanking is disabled as it is not required.
IC13 completes the audio recovery by removing high frequency noise from the plain audio output.

The Pseudo-Random Code Generator

Produces a random 31-step-sequence 5-bit logic code capable of change rates between 0.2Hz and10Hz. The sequence generator consists of a variable frequency oscillator (IC5) clocking a dual 4-stage shift register (IC6). By selecting a suitable Exclusive-NOR feedback arrangement using IC7, the random sequence length can be extended or modified.
NOTE – The code used at both Scrambler and De-scrambler must be in synchronization.

Power Requirements

This Rolling Code Scrambler operates on a single 5v, 60mA supply.

THIS APPLICATION NOTE MUST BE READ WITH A CURRENT FX224 DATA SHEET

Consumer Microcircuits Limited

PRODUCT INFORMATION

FX609 Continuously Variable Slope Delta Modulation (CVSD) Codec

Publication D/609/4 July 1994

Features/Applications

- Full Duplex CVSD Codec
- On-Chip Input and Output Filters
- Selectable 3 or 4-Bit Compand Algorithm
- Programmable Sampling Clocks
- Forced Idle Facility
- Powersave Facility
- Low Power 5V CMOS
- Digital Speech Communications
- Time Domain Scramblers
- Digital Cordless Telephone
- Voice Storage
- Digital Delay Lines
- Speech Analysis
- Multiplexers
- General Purpose

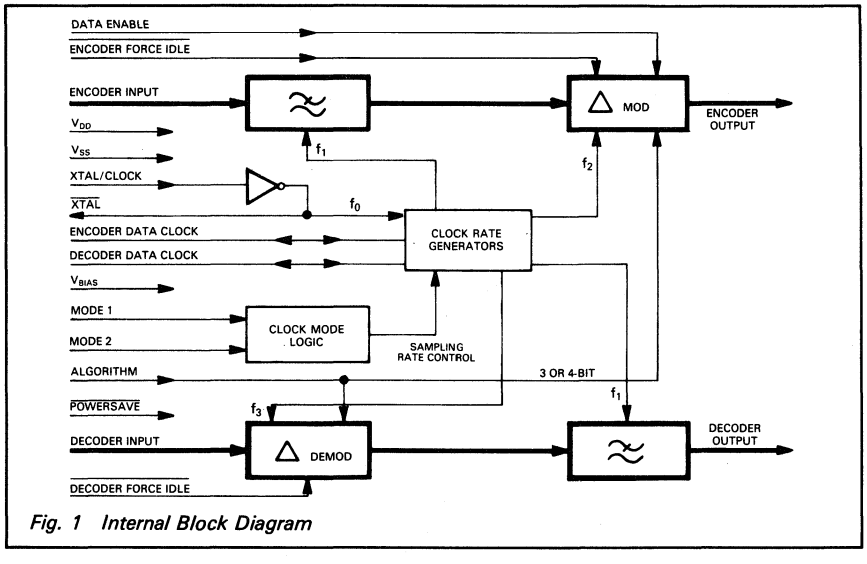


Fig. 1 Internal Block Diagram

FX609

Brief Description

The FX609 is an LSI circuit designed as a Continuously Variable Slope Delta Modulation (CVSD) Codec and is intended for use in voice storage, time domain speech scramblers and digital speech communications equipment. Encode input and decoder output analogue filters are incorporated on-chip and use switched capacitor technology. Sampling clock rates can be programmed to 16, 32 or 64k bits/second from an internal clock generator or may be externally applied in the range 8 to 64k bits/second. Sampling clock frequencies are output for the synchronisation of external circuits. The internal clocks are derived from an on-chip reference oscillator using an externally connected crystal. The encoder has an enable function for use in multiplexer applications. When not enabled, the encoder output is high impedance (three-state). Forced idle facilities in the encoder cause a perfect 1010....output pattern and in the decoder an output voltage of $V_{DD}/2$. The companding circuits may be operated with a 3 or 4-bit algorithm which is externally selected. The device may be put into standby mode by selection of the powersave facility. The FX609 is a low power, 5 volt CMOS device and is available in 22- pin DIL, 24-pin plastic quad packages.

Pin Number			Function
DIL FX609J	Quad Plastic FX609LG	Quad Plastic FX609L2	
1	1	1	**Xtal/Clock:** Input to the clock oscillator inverter. A nominal 1.024MHz xtal input or externally derived clock is injected here. See Fig. 2.
	2	2	**No connection.**
2	3	3	**$\overline{\text{Xtal}}$:** Output of clock oscillator inverter.
3	4	4	**No Connection.**
4	5	5	**Encoder Data Clock:** A Logic I/O port. External encode clock input or internal data clock output. Clock frequency dependent upon clock mode 1, 2 inputs and xtal frequency (see **Clock Mode** pins).
5	6	6	**Encoder Output:** The encoder digital output, this is a three state output:
6	7	7	**No Connection.** **$\overline{\text{Encoder Force Idle}}$:** When this pin is at logical '0' the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical '1' the encoder encodes as normal. Internal 1MΩ Pullup.
7	8	8	**Data Enable:** Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1MΩ Pullup.
8	9	9	**No Connection.**
9	10	10	**Bias:** Normally at $V_{DD}/2$ bias, this pin requires to be externally decoupled by a capacitor, C_2. Internally pulled to V_{SS} when "$\overline{\text{Powersave}}$" is logical '0'.
10	11	11	**Encoder Input:** The analogue signal input. Internally biased at $V_{DD}/2$, an external 1μF input coupling capacitor, C_1, is required on this input. See Fig. 2 Note 3 for source impedance details.
11	12	12	**V_{SS}:** Negative Supply (GND).
12	13	13	**No connection.**
13	14	14	**Decoder Output:** The recovered analogue signal is output at this pin, it is the buffered output of a low pass filter. During "$\overline{\text{Powersave}}$" this output is o/c.
14	15	15	**No Connection.**
15	16	16	**$\overline{\text{Powersave}}$:** A logical '0' at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical '1' the codec operates normally. Internal 1MΩ Pullup.
	17	17	**No Connection.**
16	18	18	**$\overline{\text{Decoder Force Idle}}$:** A logical '0' at this pin gates a 0101...pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$. When this pin is at a logical '1' the decoder operates as normal. Internal 1MΩ Pullup.
17	19	19	**Decoder Input:** Received digital signal input. Internal 1MΩ Pullup.
18	20	20	**Decoder Data Clock:** A Logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1, 2 inputs, see **Clock Mode** pins.
19	21	21	**Algorithm:** A logical '1' at this pin sets this device for a 3-bit companding algorithm. A logical '0' sets a 4-bit companding algorithm. Internal 1MΩ Pullup.
20	22	22	**Clock Mode 2:** These inputs select encoder and decoder data clock modes.
21	23	23	**Clock Mode 1:**
22	24	24	**V_{DD}: Positive Supply:** A single +5 volt power supply is required.

Data Enable	$\overline{\text{Powersave}}$	Encoder Output
1	1	Enabled
0	1	High Z (o/c)
1	0	V_{SS}

Internal 1MΩ pull-ups.

Clock 1	Mode 2	
0	0	External Clocks
0	1	Internal, 64kb/s = f ÷ 16
1	0	Internal, 32kb/s = f ÷ 32
1	1	Internal, 16kb/s = f ÷ 64

Clock rates refer to f = 1.024MHz Xtal/Clock input.
During Internal Data Clock operation the data clock frequencies are available at the ports for external circuit synchronisation. Independent or Common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode.

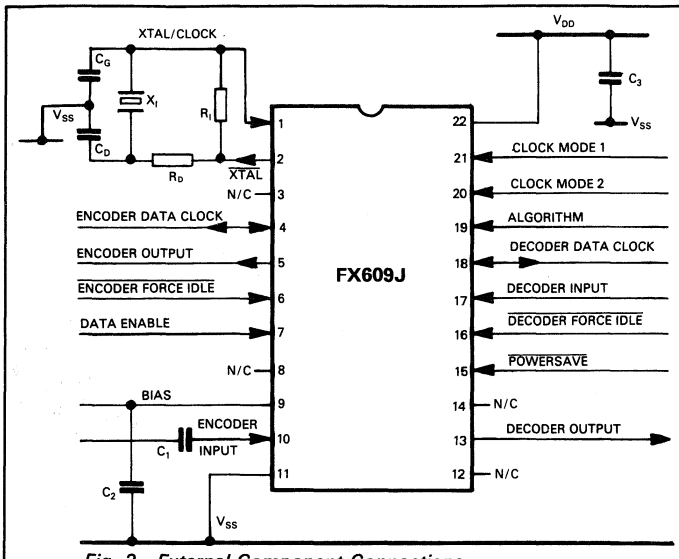


Fig. 2 External Component Connections

Component References		
Component	**Unit Value**	**Note**
R_1	Typ. 1 M	1
R_D	Selectable	1
C_1	1.0μ	
C_2	1.0μ	
C_3	1.0μ	
C_D	Typ. 33p	1
C_G	Typ. 68p	1
X_1	1.024 MHz	1, 2

Tolerance

Resistors $\pm 10\%$
Capacitors $\pm 20\%$

NOTES

1. *Xtal circuitry shown is in accordance with CML application note D/XT/1 April '86.*
2. *A 1.024 MHz clock/xtal input will yield exactly 16/32/64 kb/s data clock rates.*
3. *To prevent unwanted internal oscillations at the encoder input pin, the source impedance to this input must be less than 100Ω. Output noise levels will improve with even lower source impedances.*

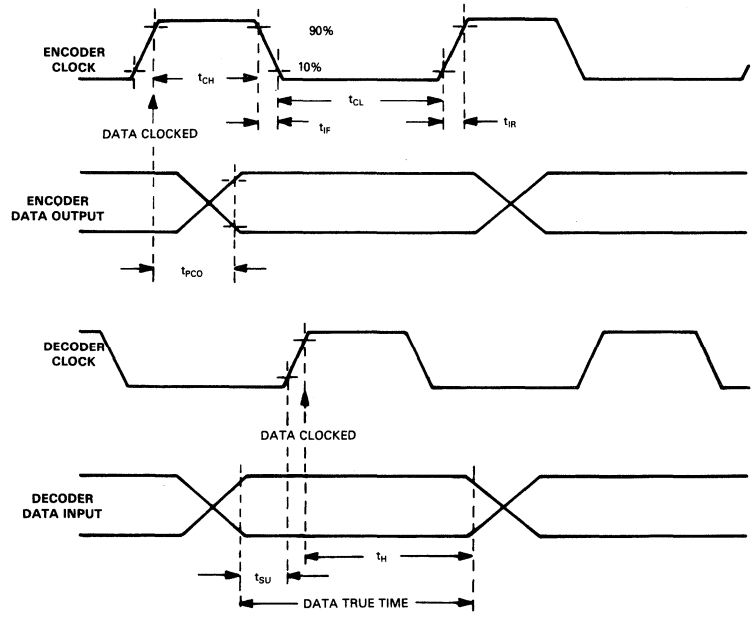


Fig. 3 Codec Timing Diagrams

TIMING

t_{CH} *Clock '1' Pulse Widths 1µs Min.*

t_{CL} *Clock '0' Pulse Widths 1µs Min.*

t_{IR} *Clock Rise Time 100ns Typ.*

t_{IF} *Clock Fall Time 100ns Typ.*

t_{SU} *Data Set-up Time 450ns Max.*

t_H *Data Hold Time 600ns Min.*

$t_{SU} + t_H$ *Data True Time*

t_{PCO} *Clock to Output Delay Time = 750ns Max.*
Xtal input 1.024 MHz.

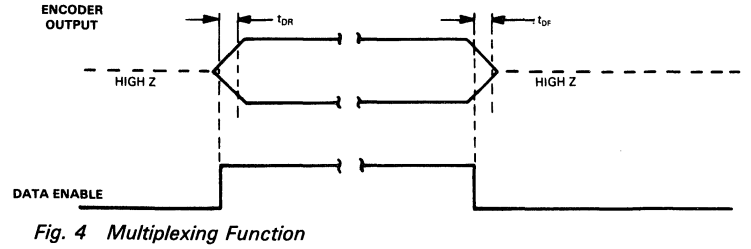


Fig. 4 Multiplexing Function

TIMING

t_{DR} *Data Rise Time 100ns Typ.*

t_{DF} *Data Fall Time 100ns Typ.*

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3 to (V_{DD} + 0.3V)
Output sink/source current (supply pins)		±30mA
(other pins)		±20mA
Total device dissipation @ 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX609J**	-30°C to +85°C (Ceramic)
	FX609LG/L2	-40°C to +85°C (Plastic)
Storage temperature range:	**FX609J**	-55°C to +125°C (Ceramic)
	FX609LG/L2	-40°C to +85°C. (Plastic)

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:

V_{DD} = 5V, T_{amb} = 25°C, Xtal/Clock (f) = 1.024 MHz, Sample Rate 32kb/s.
[Standard Test Signal 820Hz, ref. 0dB = 489mV (rms)]

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)		—	3.5	—	mA
Supply Current (Powersave)		—	500	—	µA
Inputs Logic '1'		3.5	—	—	V
Inputs Logic '0'		—	—	1.5	V
Outputs Logic '1'		4.0	—	—	V
Outputs Logic '0'		—	—	1.0	V
Digital Input Impedance (logic I/O pins)		—	10	—	MΩ
Digital Input Impedance (logic input pins, pullup resistor)	2	300	—	—	kΩ
Digital Output Impedance		—	4	—	kΩ
Analogue Input Impedance		—	100	—	kΩ
Analogue Output Impedance		—	800	—	Ω
Three State Output leakage Current (output disabled)		—	±4	—	µA
Insertion Loss		—	0	—	dB
Dynamic Values	1				
Encoder:					
Analogue Signal Input levels	5	−30	—	+8	dB
Principal Integrator Frequency		—	275	—	Hz
Encoder Passband			3400		Hz
Compand Time Constant		—	4	—	ms
Decoder:					
Analogue Signal Output levels	5	−30	—	+8	dB
Decoder Passband		300	—	3400	Hz
Encoder Decoder (Full codec):					
Passband		300	—	3400	Hz
Stopband		6	—	10	kHz
Stopband Attenuation		—	60	—	dB
Passband Gain		—	0	—	dB
Passband Ripple		−3	—	+3	dB
Output Noise (Input short circuit)		—	−60	—	dB
Perfect Idle Channel Noise (Encode Forced)		—	−63	—	dB
Group Delay Distortion	3				
1000 − 2600Hz		—	—	450	µs
600 − 2800Hz		—	—	750	µs
500 − 3000Hz		—	—	1.5	ms
Xtal/Clock Frequency		500	1024	1500	kHz

Notes:
1. *Dynamic characteristics specified at 5V only.*
2. *All logic Inputs except, Encoder and Decoder Data Clocks.*
3. *Group delay distortion for full codec relative to the delay at 820Hz, −20dB at the encoder input.*
4. *Relative timings are shown on Figures 3 and 4.*
5. *Recommended values—see graph Fig. 7.*

Codec Performance

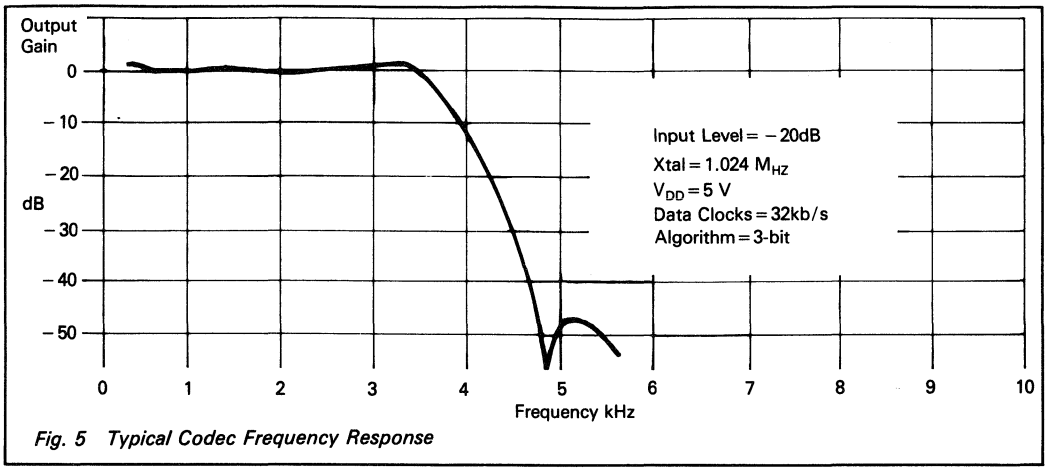


Fig. 5 Typical Codec Frequency Response

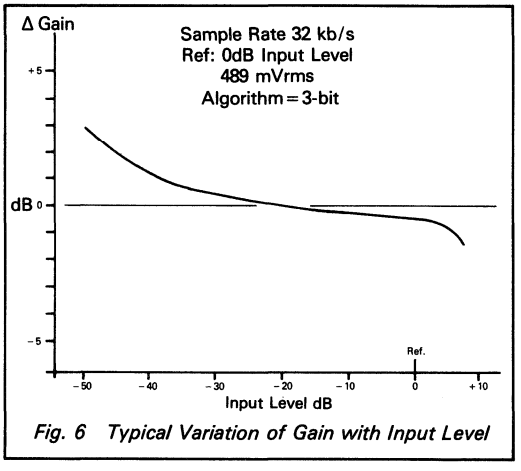


Fig. 6 Typical Variation of Gain with Input Level

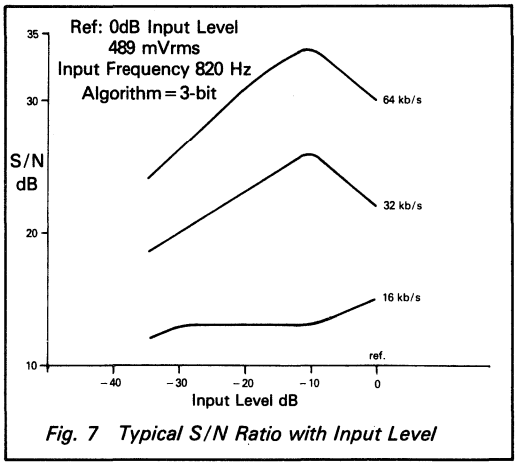


Fig. 7 Typical S/N Ratio with Input Level

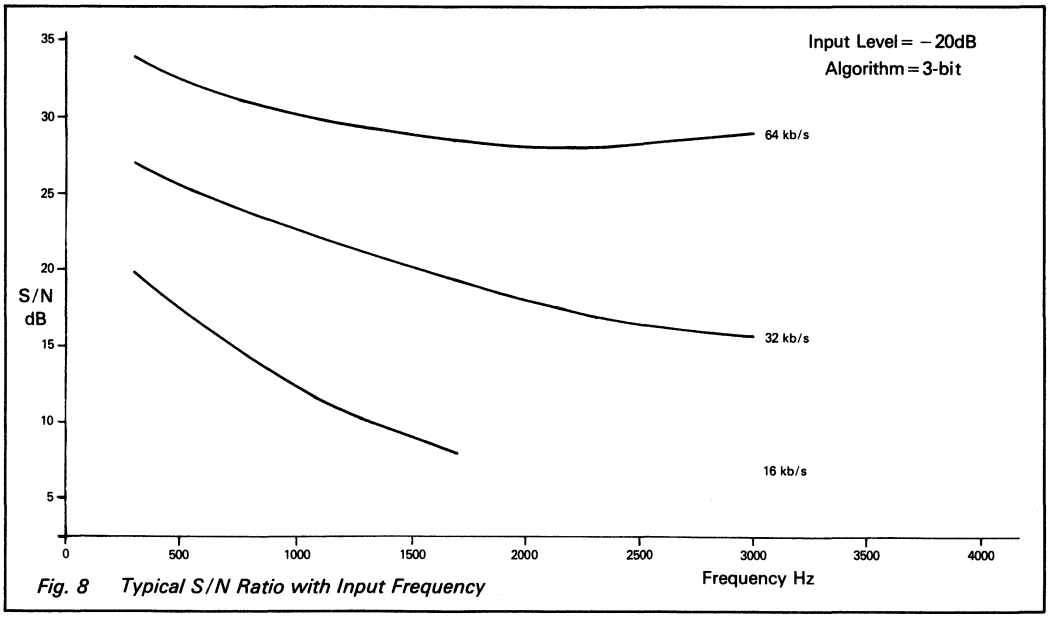


Fig. 8 Typical S/N Ratio with Input Frequency

Package Outlines

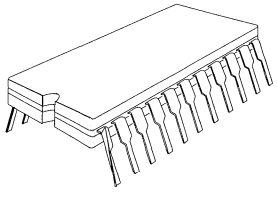
The FX609 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX609 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX609J 22-pin cerdip DIL (J3)

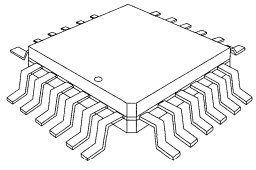
NOT TO SCALE



Max. Body Length 27.38mm
Max. Body Width 9.75mm

FX609LG 24-pin quad plastic encapsulated bent and cropped (L1)

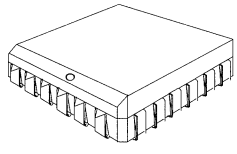
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX609L2 24-lead plastic leaded chip carrier (LS)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX609J	22-pin cerdip DIL	(J3)
FX609LG	24-pin quad plastic encapsulated bent and cropped	(L1)
FX609L2	24-lead plastic leaded chip carrier	(LS)

Consumer Microcircuits Limited

PRODUCT INFORMATION

FX709 Voice Store Retrieve CVSD Codec

Publication D/709/6 July 1994

Features/Applications

- CVSD Encode + Decode
- Programmable Clock Rates
- Programmable Voice Filters
- Voice Power Output
- Voice Spectrum Monitor
- 8-bit Memory/Instruction I/O
- Processor Interface
- Voice Message Mailbox
- Status Annunciators
- Re-try Message Forward
- Voice Security Scrambling
- Voice Data Communications
- Time/Frequency Companding
- Audio Delay Functions

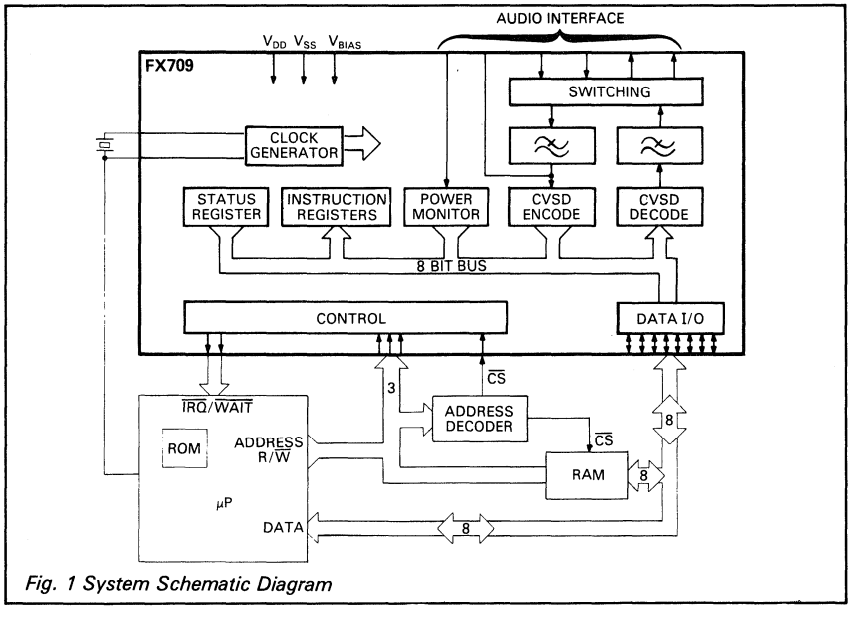


Fig. 1 System Schematic Diagram

FX709

Brief Description

The FX709 is an audio-digital interface codec for microprocessor controlled Voice Store and Retrieve applications.

In encode, audio input signals are band-limited by a lowpass filter and digitised by a CVSD 1-bit serial encoder. After conversion to 8-bit parallel format, encoded data is read to the I/O bus for storage in memory.

In decode, memory contents written into the I/O port are converted back to 1-bit serial form and decoded by a CVSD decoder. The decoder output is lowpass filtered and output as retrieved audio.

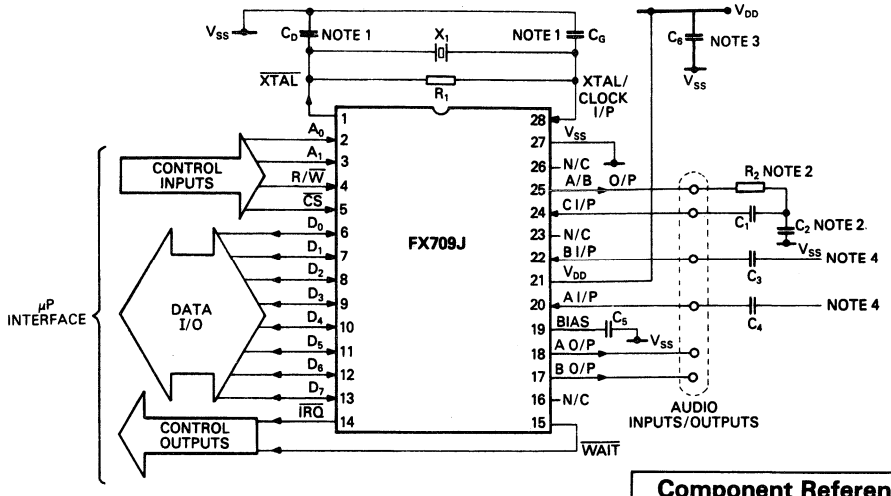
The audio encode/decode functions are independently controlled, permitting concurrent or asynchronous VSR operations to be performed. Time and frequency companding is available via independently programmable encode/decode data rates and filter cut-offs.

Support for VOX functions and 'Pause' memory management is provided by the power assessment register.

This contains two 4-bit numbers representing the average signal levels into the data encoder and a replica encoder over a programmable averaging period.

The device instruction set includes input/output signal switching and a standby powerdown function. The FX709 is a lowpower CMOS circuit and uses a single 5 volt supply.

Pin Number FX709J/LH	Function
1	**$\overline{\text{Xtal}}$:** Output of clock oscillator inverter.
2 3 4	**A_0:** **A_1:** These pins determine which register may be addressed via the I/0 port. **R/$\overline{W}$:** A_0 A_1 R/$\overline{W}$ **Register** 0 0 0 'A' instruction 1 0 0 'B' instruction 0 1 0 Decoder 1 1 0 No Register 0 0 1 Status 1 0 1 Power 0 1 1 Encoder 1 1 1 No Register
5	**$\overline{\text{CS}}$:** Chip Select input, this input has a 1 MΩ pullup to V_{DD}.
6 7 8 9 10 11 12 13	**D_0:** **D_1:** **D_2:** **D_3:** **I/0 Port** **D_4:** **D_5:** **D_6:** **D_7:**
14	**$\overline{\text{IRQ}}$:** Interrupt Request Output, this pin is the output of the interrupt request generator. This device can be "wire OR'd" with other active-low components. See section on Interrupt Requests. (100kΩ internal pullup to V_{DD}).
15	**$\overline{\text{WAIT}}$ Output:** The circuit requires a minimum Chip Select time of t_{ACS}. If the host µP has a CS time of less than this the WAIT output must be used to delay the µP when accessing the FX709. (See Figure 7). (100kΩ internal pullup to V_{DD}). *NOTE:* If the WAIT output is to be used, then to prevent spurious operation of this function during Power-Up, it is recommended that: a: Power-Up of the FX709 is delayed until µP Power-Up is complete, or, b: The Chip Select input is held open-circuit during the FX709 Power-Up sequence.
16	No connection.
17	**Analogue Output B:** (See Figure 4).
18	**Analogue Output A:** (See Figure 4).
19	**V_{BIAS}:** The bias or analogue ground pin and is internally set to $V_{DD}/2$. It should be decoupled to V_{SS} with a capacitor of 1.0µF (min.).
20	**Analogue Input A:** (See Figure 2, Note 4 and Figure 4).
21	**V_{DD}:** Positive Supply.
22	**Analogue Input B:** (See Figure 2, Note 4 and Figure 4).
23	No connection.
24	**Analogue Input C:** This is the analogue input to the power encoder.
25	**Analogue Output A/B:** (See Figure 4).
26	No connection.
27	**V_{SS}:** Negative supply.
28	**Xtal/Clock Input:** This is the input to the clock oscillator inverter. A 1.0 MHz Xtal input or externally derived clock is injected at this pin.



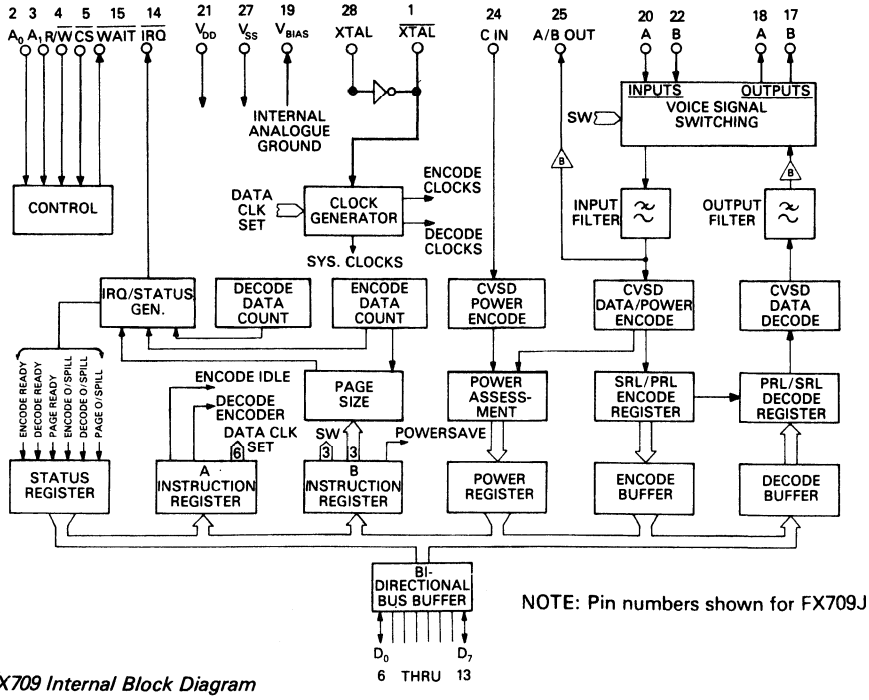
NOTES:

1. *C_G used to reduce voltage overshoot. Refer to CML Crystal application Applications Note D/XT/1 April 86.*
2. *R_2, C_2 forms a lowpass filter input to 'C' input power assessment circuit. The values shown represent a 820Hz lowpass although other cutoff frequencies may be selected depending on the application — see page 9.*
3. *Additional decoupling may be necessary for noisy supplies.*
4. *To prevent unwanted internal oscillations at the Encoder input pins, the source impedance to these inputs must be less than 100Ω. Output idle channel noise levels will improve with even lower source impedances.*

Component References

Component	Unit Value	Tolerance
R_1	>1M	±10%
R_2	5.6k	±10%
C_G	68p	Note 1
C_D	33p	Note 1
C_1	0.1μ	±20%
C_2	33n	±20%
C_3	0.1μ	±20%
C_4	0.1μ	±20%
C_5	1.0μ min	±20%
C_6	0.1μ	±20%

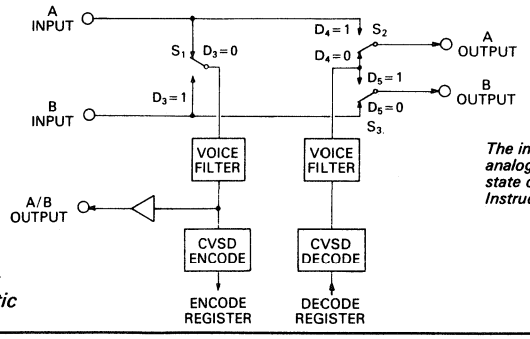
Fig. 2 External Component Connections



NOTE: Pin numbers shown for FX709J

Fig. 3 FX709 Internal Block Diagram

Analogue Switching



The input and output switching of analogue signals is controlled by the state of bit no's D_3, D_4 and D_5 in Instruction Register B.

Fig. 4 Audio Switching — Simplified Block Schematic

Frequency and Data Rate Control

Six bits of Instruction Register A (D_2 — D_7) control the data rates of the encoder and decoder and the bandwidths of the filters for the encoder and decoder. The configuration of the frequency dividers is as shown in the diagrams below and obtainable combinations of frequencies with various input clocks are listed.

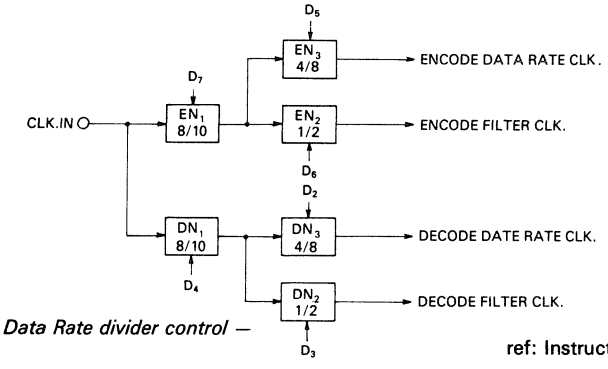


Fig. 5 Filter Clock and Data Rate divider control — Block diagram

ref: Instruction Register 'A'

CLOCK INPUT	N1	N2	FILTER CLOCK (Hz)	LOWPASS FILTER BW PB. ± 1dB	N3	DATA CLOCK (kbs)
2MHz	8	2	125k	3320	4	62.5
,,	8	2	125k	3320	8	31.25
,,	10	2	100k	2656	4	50.0
,,	10	2	100k	2656	8	25.0
1MHz	8	1	125k	3320	4	31.25
,,	8	1	125k	3320	8	15.625
,,	8	2	62.5k	1660	4	31.25*
,,	8	2	62.5k	1660	8	15.625*
,,	10	1	100k	2656	4	25.0
,,	10	1	100k	2656	8	12.5
,,	10	2	50k	1328	4	25.0*
,,	10	2	50k	1328	8	12.5*
2.048MHz	8	2	128k	3400	4	64.0
,,	8	2	128k	3400	8	32.0
,,	10	2	102.4k	2720	4	51.2
,,	10	2	102.4k	2720	8	25.6
1.024MHz	8	1	128k	3400	4	32.0
,,	8	1	128k	3400	8	16.0
,,	8	2	64k	1700	4	32.0*
,,	8	2	64k	1700	8	16.0*
,,	10	1	102.4k	2720	4	25.6
,,	10	1	102.4k	2720	8	12.6
,,	10	2	51.2k	1360	4	25.6*
,,	10	2	51.2k	1360	8	12.6*
614.4kHz	8	1	76.8k	2040	8	9.6*
768.0kHz	10	1	76.8k	2040	8	9.6*

***Caution:** Although possible, the Codec insertion loss is not according to the specification at these settings. (see Page 10).

Table 1 Possible combinations of clock input frequency, filter cutoff (Hz) and Data Clock (kbs)

Register Truth Tables

The following tables describe the function of each bit within each register. 'Address Input' logic states are shown in the top right hand corner of each table. The following registers are described below:

IRA	INSTRUCTION REGISTER 'A'			A_0 = 0 A_1 = 0 R/$\overline{W}$ = 0
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_0	Encoder Idle		SRD_3	D_0 sets the encoder idle/normal mode of operation.
		1		**FORCED:** Forces the encode register to fill with a 1010101... idle pattern. *Note: incoming encoded data is still available for the power assessment circuits.*
		0		**NORMAL:** Allows the encode register to fill with encoded data. Data is transferred to the encode buffer during the last bit of the encode byte.
D_1	Decoder Data Source In Overspill		SRD_4	D_1 determines the source of data for the decoder.
		1		**ENCODER:** Internally connects the output of the encode register to the input of the decode register. This condition effectively connects the audio straight through. The encoded data may still be accessed via the encode buffer, and I/O port.
		0		Fills the decode register with idle pattern. In either case data may be loaded into the decode register via the I/O port. This automatically overwrites the current contents of the decode register.
D_2	Decode Data Rate Clock Divider		Fig. 5 Table 1	D_2 sets the Decode data rate divider.
		1		÷ 8
		0		÷ 4
D_3	Decode Filter Clock Divider		Fig. 5 Table 1	D_3 sets the Decode Filter Clock Divider and hence the Filter Cut-off Frequency.
		1		÷ 2
		0		÷ 1
D_4	Decode Master Clock Divider		Fig. 5 Table 1	D_4 sets the Decode Master clock divider.
		1		÷ 10
		0		÷ 8

IRA	INSTRUCTION REGISTER 'A'			A_0 = 0 A_1 = 0 R/$\overline{W}$ = 0
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_5	Encode Data Rate Divider	1 0	Fig. 5 Table 1	D_5 sets the Encode Data Rate Divider. ÷ 8 ÷ 4
D_6	Encode Filter Clock Divider	1 0	Fig. 5 Table 1	D_6 sets the Encode Filter Clock Divider and hence the filter cut-off frequency. ÷ 2 ÷ 1
D_7	Encode Master Clock Divider	1 0	Fig. 5 Table 1	D_7 sets the Encode Master Clock Divider. ÷ 10 ÷ 8

IRB	INSTRUCTION REGISTER 'B'			A_0 = 1 A_1 = 0 R/$\overline{W}$ = 0
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_0 D_1 D_2	Page Size Set	See Notes		$D_0 - D_2$ set the "page size" in Encode Data bytes. (one byte = 8 serial data bits) in accordance with the table below: Page Period (secs) = 8 x Page Bytes/Data Rate (b/s)
D_3	"A/B" Encode	0 1	Fig. 4	D_3 defines which audio input A or B is connected to the encoder via the encode filter. (See fig. 4). **AUDIO INPUT "A":** Internally connects the "A" audio input to the encode filter input. The "A/B OUT" pin outputs filtered audio "A". Audio input "B" set to $V_{DD}/2$. **AUDIO INPUT "B":** Internally connects the "B" audio input to the encode filter input. The "A/B OUT" pin outputs filtered audio "B". Audio input "A" set to $V_{DD}/2$.

D_2	D_1	D_0	:	PAGE BYTES	Page Period @32kbs
0	0	0	:	32	8ms
0	0	1	:	64	16ms
0	1	0	:	96	24ms
0	1	1	:	128	32ms
1	0	0	:	160	40ms
1	0	1	:	192	48ms
1	1	0	:	224	56ms
1	1	1	:	256	64ms

IRB	INSTRUCTION REGISTER 'B'			A_0 = 1 A_1 = 0 R/$\overline{W}$ = 0
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_4	Switch Audio Output "A"	 1 0	Fig. 4	D_4 controls the Output Audio Switch to determine which source audio is connected to Audio Output "A" pin. Input "A" to Output "A" (direct). Decoder to Output "A".
D_5	Switch Audio Output "B"	 1 0	Fig. 4	D_5 controls the Output Audio Switch to determine which source audio is connected to Audio Output "B" pin. Decoder to Output "B" Input "B" to Output "B" (direct).
D_6	Powersave	 1 0		D_6 controls the enablement and disablement of all analogue circuit elements. **POWERSAVE MODE:** Disables the circuit elements, thereby effectively reducing current consumption. **OPERATING MODE:** All circuit elements enabled. **NOTE:** During POWERSAVE, inputs are biased $V_{DD}/2$. Outputs are biased $V_{DD}/2$ if IRB D_4/D_5 are set to "direct".
D_7	Power Sensitivity	 1 0		D_7 determines the sensitivity range of the power measuring circuits. **HIGH:** Low power input, assessment circuits have +12dB gain over LOW Setting. **LOW:** Normal power assessment sensitivity range. **NOTE:** High input levels in the HIGH condition may lead to overflow, producing an ambiguous reading.

SR	STATUS REGISTER			A_0 = 0 A_1 = 0 R/$\overline{W}$ = 1
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_0	Encode Data Ready	1		D_0 indicates that a byte of data has been encoded and can be read from the encode buffer. **READ BYTE:** Set high during the last bit of the byte shifted into the encode register. This condition causes an interrupt request.
		0		**NOT READY/OVERSPILL:** This condition occurs when: 1. The last data byte in the encode data register has been read. 2. Encode data overspill bit = 1 ie. $SRD_3 = 1$.
D_1	Decode Data Ready	1	SRD_4	D_1 indicates that a byte of data has been decoded and a new byte should be written to the decode buffer. **WRITE BYTE:** This condition occurs when the decode register has been loaded from its buffer, i.e. after the last bit of the previous byte has been clocked out of the register.
		0		**NOT READY/OVERSPILL:** This condition occurs when data has been written into the decode buffer or the decode data overspill condition is valid ($SRD_4 = 1$).
D_2	Page Ready	1		This bit indicates that a page of bytes has been encoded. **READ PAGE:** This condition occurs when the page counter has completed the last byte of a page. This is after power measurements have been written into PRD_0 to PRD_7 inclusive.
		0	SRD_5	**NOT READY/OVERSPILL:** This condition occurs when Power Register "PR" has been read or the page overspill condition is valid.
D_3	Encode Overspill	1		**OVERSPILL:** Indicates that the encode data was not read between two consecutive "encode data ready" flags. Encoded data bytes have been lost, and no further bytes will be transferred to the encode buffer.
		0		**NORMAL:** This condition occurs when data has been read from the encode buffer, following a data ready flag, $SRD_0 = 1$, or by writing to the decode buffer if both encode and decode overspill bits are set. (See 'Interrupts' page 9).
D_4	Decode Overspill	1		**OVERSPILL:** When this bit is set data transfer from the decode buffer to the decode register is inhibited. If the "DECODER/ENCODER BUS" ($IRAD_1$) is not set then the decode register will fill with idle pattern.
		0		**NORMAL:** This condition occurs when data has been written to the decode buffer following a data ready flag, $SRD_1 = 1$ or by reading the contents of the encode buffer if both encode and decode overspill bits are set. (See 'Interrupts' page 9).

SR	STATUS REGISTER			$A_0 = 0$ $A_1 = 0$ $R/\overline{W} = 1$
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_5	Page Overspill	1		**OVERSPILL:** This state indicates that the power register was not read before the next page was completed.
		0		**NORMAL:** Power register "read" or IRB written.

PR	POWER REGISTER		$A_0 = 1$ $A_1 = 0$ $R/\overline{W} = 1$
Bit	**Function Name**	**Logic State**	**NOTES**
D_0 D_1 D_2 D_3	"A/B" Power LSB "A/B" Power MSB		$D_0 - D_3$ represent the average signal level of the last page of data in the range from +6dBm to −24dBm (at 1kHz) for the A or B input. The relationship between binary value and signal level is frequency dependant and exhibits pre-emphasis characteristics. (see fig. 9).
D_4 D_5 D_6 D_7	"C" Power LSB "C" Power MSB		$D_4 - D_7$ represent the average signal level of the last page of data in the range from +6dBm to −24dBm (at 1kHz) for the C input.

Interrupts

Three conditions can cause interrupt requests to the host microprocessor.

(i) The encode buffer contains an unread byte of data which is the most recent byte encoded.

(ii) The decode buffer is ready to receive the next consecutive byte for decoding.

(iii) The power register contains a power assessment for the most recent whole page encoded.

The status register indicates which of the above conditions are true.

If an interrupt condition remains unserviced and the condition becomes irrecoverably untrue, the status bit is cleared, the corresponding overspill bit is set and further interrupts are automatically inhibited. Also the encode and decode data buffers retain the data present when the data bit was set, i.e. register-buffer update is inhibited. The power register is updated at all times.

Condition (i) is serviced by a valid address to the encode buffer. Condition (ii) is serviced by a valid address to the decode buffer. If conditions (i) and (ii) have both become UNTRUE, servicing either buffer resets both to a cleared start position. Condition (iii) is serviced by reading the Power Register.

The C Input

By careful selection of the audio frequency filtering to the C input the A/B and C power words can be used in the processor to provide frequency as well as power information. This facility could be used for word, pause or voice recognition.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref. V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	FX709J	−30°C to + 85°C
	FX709LH	−30°C to + 70°C
Storage temperature range:	FX709J	−55°C to +125°C
	FX709LH	−40°C to + 85°C

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5V, T_{amb} = 25°C, Ø = f_{in} = 1kHz.

Characteristics	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply voltage		4.5	5.0	5.5	V
Supply Current		—	6	—	mA
Supply Current (Power Save)		—	1	—	mA
Supply Ripple		—	50	—	mV
Input Impedance (Audio)		100	—	—	kΩ
Output Impedance (Audio)		—	—	6	kΩ
Input Logic '1'		3.5	—	—	V
Input Logic '0'		—	—	1.5	V
Output Logic '1'	1	3.5	—	—	V
Output Logic '0'	1	—	—	1.5	V
Input Current (Logic I/P's)		—	—	1.0	μA
Input Capacitance (Logic I/P's)		—	—	7.5	pF
Output Logic '1' Source current	2	—	—	120	μA
Output Logic '0' Sink current	3	—	—	360	μA
Three State output leakage current		—	—	4	μA
Dynamic Characteristics					
Audio Input Level		—	500	—	mV (rms)
Insertion Loss, (direct)	4, 7	−1.5	—	+1.5	dB
Attenuation distortion *(See Fig. 6)*					
Clock bit Rate	5	8	—	64	k bits/s
Idle Channel Noise	4, 6	—	2.5	—	mV (rms)
Signal/Noise Ratio *(See Fig. 8)*					

Notes

1. *Load 50pF, 200kΩ.*
2. *V_{out} = 4.6V, not pins 14 ($\overline{IRQ}$) and 15 ($\overline{WAIT}$), these wire OR 'able pins have 100kΩ pullups .*
3. *V_{out} = 0.4V.*
4. *Measured from Codec audio input to audio output.*
5. *2.048MHz master clock ÷ 32.*
6. *32kHz clock.*
7. *For a load of > 100kΩ, (serial switch impedance is 3kΩ/switch, see Fig. 4.*

Typical Performance

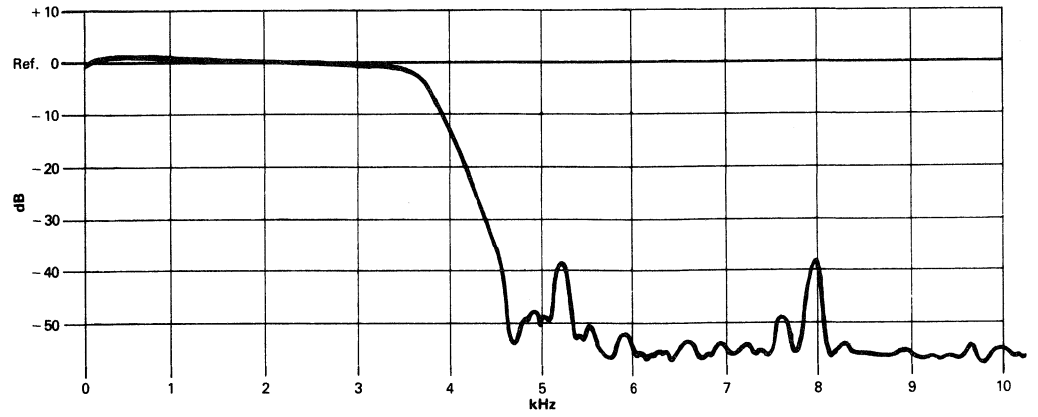
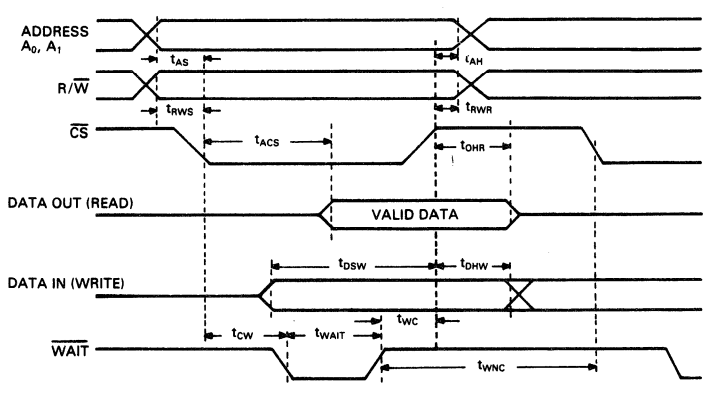


Fig. 6 Typical FX709 System Response measured at: filter 3320 Hz, V_{IN} −24 dBm, 32 kb/s



t=	Min.	Typ.	Max.	Units
t_{AS}	50	—	—	ns
t_{RWS}	50	—	—	ns
t_{AH}	0	—	—	ns
t_{RWR}	0	—	—	ns
t_{ACS}	—	—	250	ns
t_{OHR}	0	—	100	ns
t_{DSW}	150	—	—	ns
t_{DHW}	150	—	—	ns
t_{CW}	—	—	100	ns
t_{WAIT}	2	—	3	Xtal Cycle
t_{WC}	0	—	—	ns
t_{WNC}	2	—	—	Xtal Cycle

KEY

t_{AS} – Address Set Up Time
t_{RWS} – Read/Write Set Up Time
t_{AH} – Address Hold Time
t_{RWR} – Read/Write Recovery Time
t_{ACS} – Chip Select Access Time
t_{OHR} – Output Hold Time (Read)
t_{DSW} – Data Set Up Time (Write)
t_{DHW} – Data Hold Time (Write)
t_{CW} – Chip Select to WAIT Output
t_{WAIT} – WAIT Time
t_{WC} – WAIT High to Chip Select High
t_{WNC} – End of Wait to Next Chip Select

Fig. 7 Timing Diagram

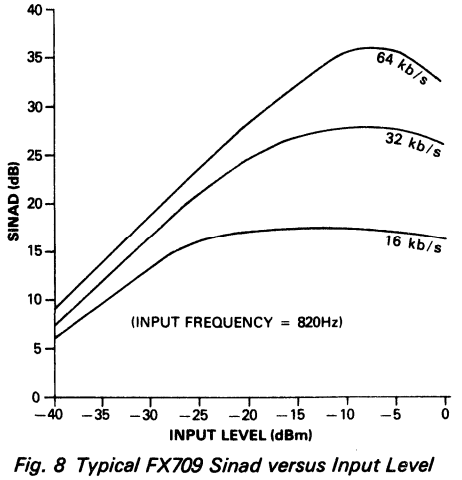


Fig. 8 Typical FX709 Sinad versus Input Level

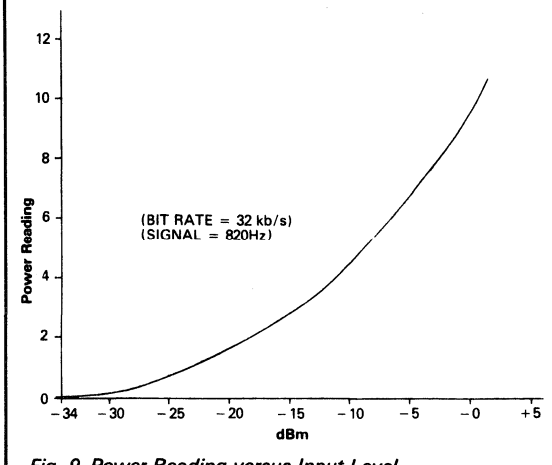


Fig. 9 Power Reading versus Input Level

Package Outlines

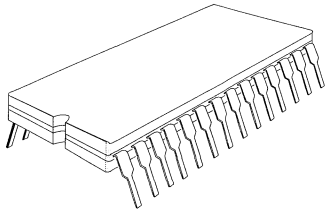
The FX709 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX709 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX709J 28-pin cerdip DIL (J5)

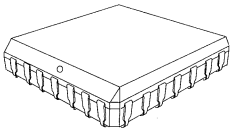
NOT TO SCALE



Max. Body Length 37.05mm
Max. Body Width 13.36mm

FX709LH 28-lead plastic leaded chip carrier (L3)

NOT TO SCALE



Max. Body Length 11.58mm
Max. Body Width 11.58mm

Ordering Information

FX709J 28-pin cerdip DIL (J5)

FX709LH 28-lead plastic leaded chip carrier (L3)

Integrated Circuits Data Book

Section 10

Package Information

CML Microcircuit Package Information

Package Suffixes

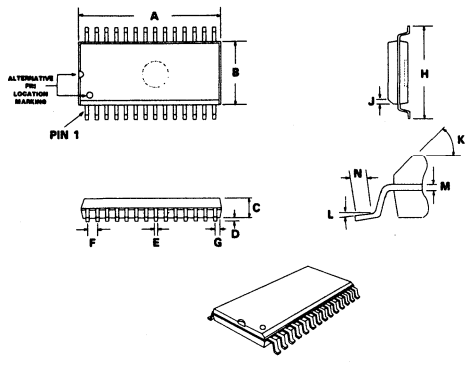
CML package styles are currently identified with the following suffixes: J, LG, LH, LS and P.
To make this system more explanatory, new identifier suffixes are being introduced to all NEW CML products.
For an undetermined period both current and new identifiers will be used in publications where relevant.
The table below explains the old and new nomenclature:

Package Information	PLCC - Plastic Leaded Chip Carrier. TQFP - Thin Quad Plastic Flatpack. SOIC - Small Outline Integrated Circuit. PDIP - Plastic Dual In Line.						
Number of Pins	**Material**	**Package Type**	**Package Style**	**Lead Style**	**Current Product Suffix**	**New Product Suffix**	**Page**
24	Plastic	PLCC	Quad	Gull	LG	L1	10.6
24	Plastic	PLCC	Quad	Hook	LS	L2	10.5
28	Plastic	PLCC	Quad	Hook	LH	L3	10.5
48	Plastic	TQFP	Quad	Gull		L4	10.5
28	Ceramic	CLCC	Quad	Hook	M1		10.7
28	Plastic	SOIC	DIL	Gull	DW	D1	10.3
24	Plastic	SOIC	DIL	Gull	DW	D2	10.3
20	Plastic	SOIC	DIL	Gull	DW	D3	10.3
16	Plastic	SOIC	DIL	Gull	DW	D4	10.3
14	Plastic	PDIP	DIL	Thro' Hole	P	P2	10.6
16	Plastic	PDIP	DIL	Thro' Hole	P	P3	10.6
24	Plastic	PDIP	DIL	Thro' Hole	P	P4	10.6
14	Ceramic	Cerdip	DIL	Thro' Hole	J	J1	10.5
16	Ceramic	Cerdip	DIL	Thro' Hole	J	J2	10.4
22	Ceramic	Cerdip	DIL	Thro' Hole	J	J3	10.4
24	Ceramic	Cerdip	DIL	Thro' Hole	J	J4	10.4
28	Ceramic	Cerdip	DIL	Thro' Hole	J	J5	10.4

CML microcircuit package working diagrams with dimensions are detailed on the following pages; basic form illustrations of the relevant packages are provided on the back page of each individual data sheet.

CML Microcircuit Package Information .....

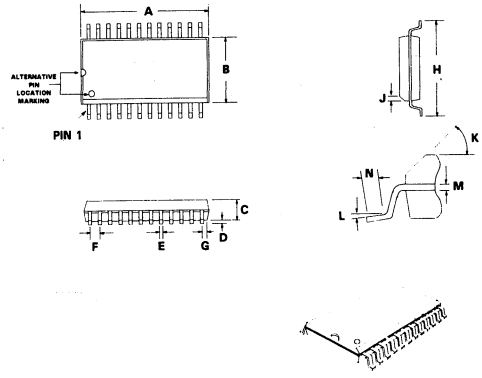
28-Pin Plastic S.O.I.C., DW (D1)



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	18.05		17.70
B	7.65		7.39
C	2.67		2.21
D		0.20	
E		0.40	
F		1.27	
G		0.66	
H	10.51		10.11
J		0.63	
K		45°	
L		5°	
M		0.25	
N		0.76	

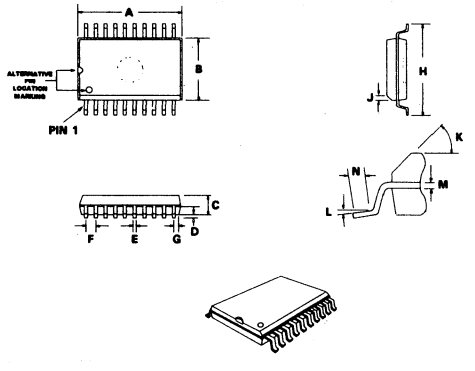
24-Pin Plastic S.O.I.C., DW (D2)



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	15.70		15.16
B	7.65		7.39
C	2.67		2.21
D		0.20	
E		0.40	
F		1.27	
G		0.66	
H	10.51		10.11
J		0.63	
K		45°	
L		5°	
M		0.25	
N		0.76	

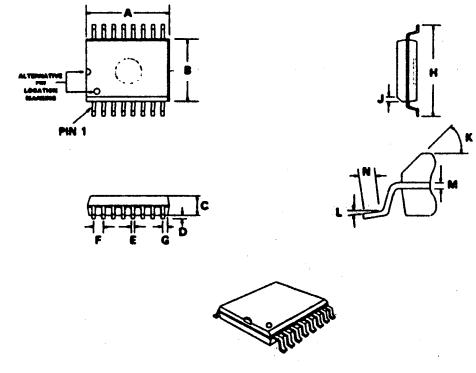
20-Pin Plastic S.O.I.C., DW (D3)



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	12.85		12.62
B	7.59		7.39
C	2.67		2.21
D		0.20	
E		0.40	
F		1.27	
G		0.66	
H	10.51		10.11
J		0.63	
K		45°	
L		5°	
M		0.25	
N		0.76	

16-Pin Plastic S.O.I.C., DW (D4)

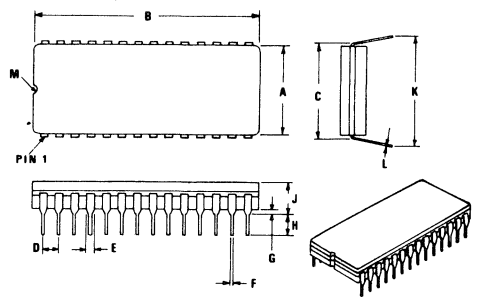


All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	10.31		10.03
B	7.59		7.39
C	2.67		2.21
D		0.20	
E		0.40	
F		1.27	
G		0.66	
H	10.51		10.11
J		0.63	
K		45°	
L		5°	
M		0.25	
N		0.76	

CML Microcircuit Package Information .....

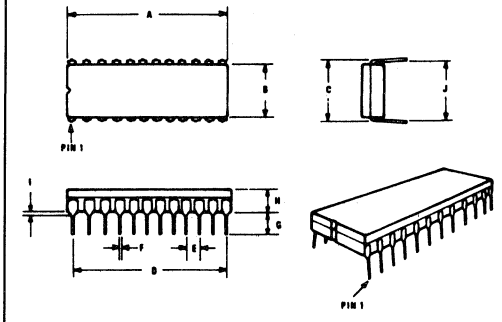
28-Pin Cerdip DIL; J (J5)



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	13.36		13.06
B	37.05		36.58
C	15.70		15.50
D		2.54	
E		1.39	
F		0.45	
G		1.40	
H	4.30		4.10
J	5.57		4.49
K		17.00	
L		0.25	
M		0.64 R	

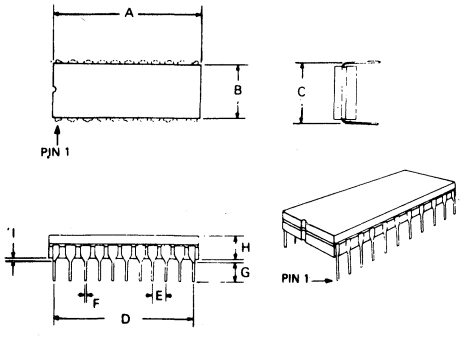
24-Pin Cerdip DIL; J (J4)



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	32.03		31.50
B	14.81		13.06
C	15.61		15.14
D	28.04		27.84
E		2.54	
F		0.46	
G	4.30		4.10
H	4.35		3.99
I		1.40	
J	18.20		16.54

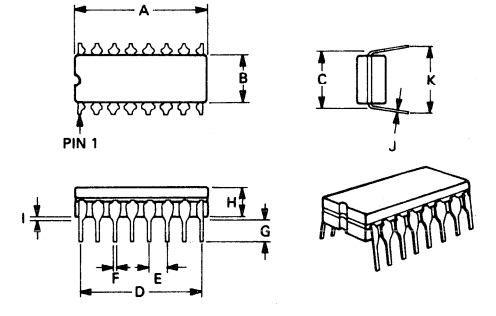
22-Pin Cerdip DIL; J (J3)



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	27.38		26.98
B	9.75		9.55
C	10.60		10.40
D	25.50		25.30
E		2.54	
F		0.46	
G	4.30		4.10
H	4.27		3.99
I		1.40	

16-Pin Cerdip DIL; J (J2)

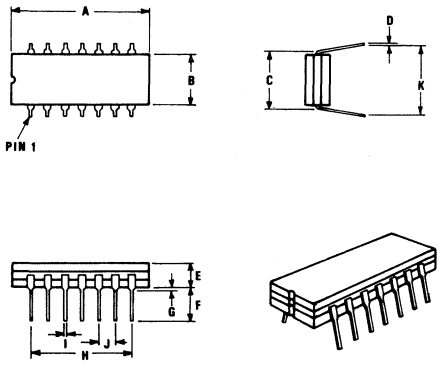


All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	19.48		19.12
B	7.40		7.24
C	8.00		7.80
D		17.78	
E		2.54	
F		0.46	
G	4.30		4.10
H		4.27	
I		1.40	
J		0.25	
K	9.45		8.45

CML Microcircuit Package Information .....

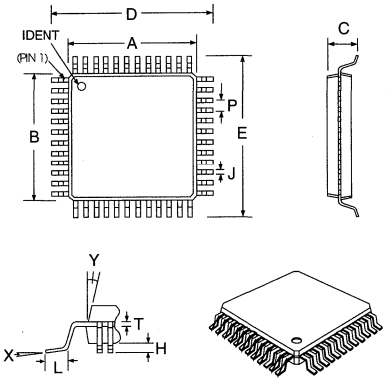
14-Pin Cerdip DIL; J (J1)



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	19.45		19.15
B	6.38		6.22
C	8.00		7.75
D		0.25	
E		4.10	
F	4.30		4.10
G		1.40	
H		15.24	
I		0.46	
J		2.54	
k	10.67		9.65

48-Pin Thin Quad Flat Pack (L4)

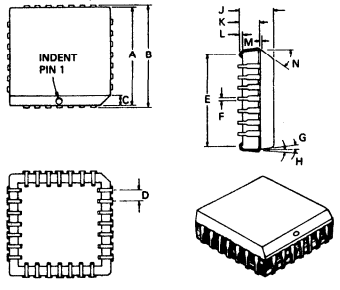


All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	7.10		6.90
B	7.10		6.90
C	1.60		
D	9.25		8.75
E	9.25		8.75
H	0.15		0.05
J	0.27		0.11
L	0.66		0.35
P		0.50	
T		0.13	
X	7°		0°
Y	13°		11°

Lead coplanarity to be 0.08 Max.

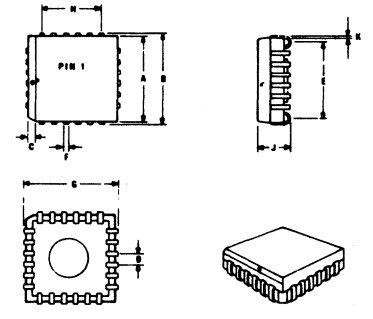
28-Lead PLCC; LH (L3)



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	11.58		11.43
B	12.57		12.32
C		1.14 x 45°	
D		1.27	
E	10.82		10.03
F		0.46	
G	7°		3°
H	7°		3°
J	4.49		4.24
K		2.50	
L	1.10		0.50
M		0.59	
N		45°	

24-Lead PLCC; LS (L2)

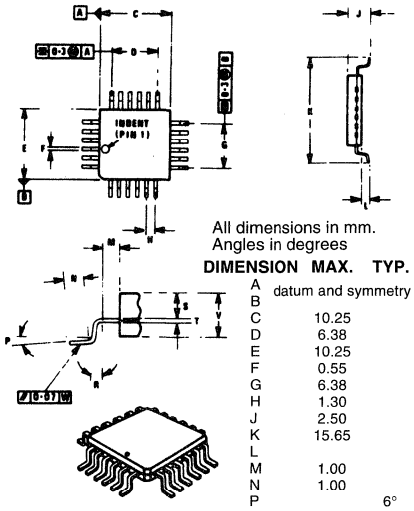


All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	10.40		9.70
B	11.05		10.60
C		1.15 x 45°	
D		1.27	
E		9.30	
F	0.55		0.45
G	11.05		10.60
H		6.35	
J	3.70		3.25
K	0.27		0.17

CML Microcircuit Package Information .....

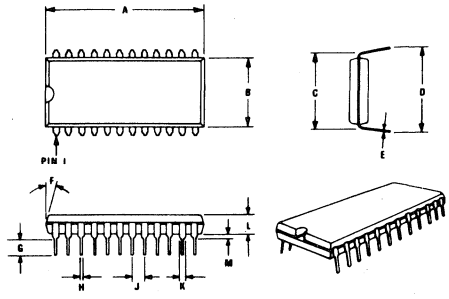
24-Pin PLCC; LG (L1)



All dimensions in mm.
Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	datum and symmetry		
B			
C	10.25		10.00
D	6.38		6.32
E	10.25		10.00
F	0.55		0.47
G	6.38		6.32
H	1.30		1.24
J	2.50		
K	15.65		
L			0.10
M	1.00		0.85
N	1.00		0.80
P		6°	
R		6°	
S	1.40		1.14
T	0.22		0.16
V		2.30	
W//	0.07		

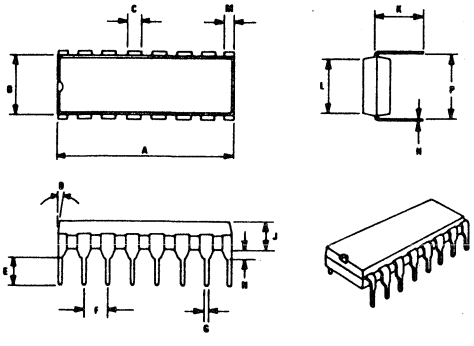
24-Pin Plastic DIL; P (P4)



All dimensions in mm.
Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	31.85		31.65
B	13.82		13.61
C	15.75		15.11
D	17.02		15.75
E		0.254	
F		7°	
G	3.43		2.92
H		0.46	
J		2.54	
K		1.52	
L	3.91		3.71
M		0.75	

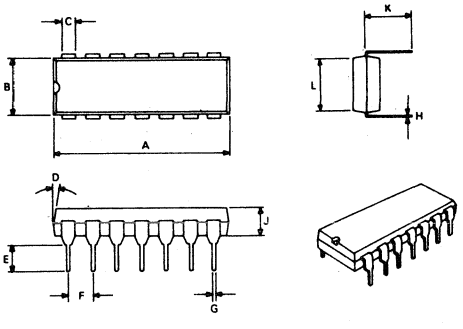
16-Pin Plastic DIL; P (P3)



All dimensions in mm.
Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	19.24		18.86
B	6.41		6.29
C	1.54		1.51
D	7°,30'		6°,30
E	3.20		3.15
F		2.54	
G		0.46	
H		0.25	
J	3.33		3.27
K	5.77		5.65
L	5.90		5.78
M	1.00		0.98
N	1.78		0.51
P	9.40		8.38

14-Pin Plastic DIL; P (P2)

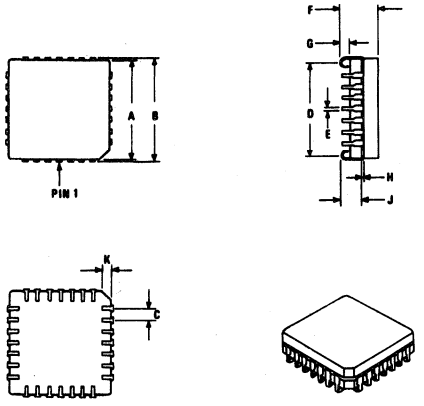


All dimensions in mm.
Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	19.24		18.86
B	6.41		6.29
C	1.54		1.51
D	7°,30'		6°,30
E	3.20		3.15
F		2.54	
G		0.46	
H		0.25	
J	3.33		3.27
K	5.77		5.65
L	5.90		5.78

CML Microcircuit Package Information .....

28-Lead Ceramic CLCC; M1



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.
A	11.50		11.35
B	12.15		12.05
C		1.27	
D	10.82		10.03
E		0.46	
F	4.30		4.20
G	1.15		1.05
H		0.59	
J	2.75		2.60
K		45°	

CML Packaging for Despatch

For ease and convenience CML products are packaged for despatch in industry standard bulk or individual packaging as described below.

- Trays (17cm x 10.5cm) and cardboard boxes with conductive foam.
- 50-pocket conductive trays for surface-mount microcircuits.
- Anti-static coated tubes, of various sizes, with thumbplugs.
- 13-inch reel Tape-and-Reel packaging which fully conforms to the latest EIC specification. The conductive embossed tape provides a secure cavity sealed with a peel-back cover tape. 500/1,000 units/reel (see Tape and Reel, Section 6.6) – no partial reel counts are available.

CML Tape and Reel Specification

1. Scope

The specification relates to the tape packaging of integrated circuits suitable for use in "surface mount" assembly. It includes only those dimensions which are essential for the purchaser to use the product.

2. Dimensions (Refer to Figure 1)

2.1 Tape Width (W)

LG, LH, LS, DW-20/24/28	W = 24.0 ± 0.3mm
DW-16	W = 16.0 ± 0.3mm

2.2 Carrier Tape Thickness (t)

t = 0.3 ± 0.05mm

2.3 Pitch of Sprocket Holes (Po)

Po = 4.0 ± 0.1mm

2.4 Diameter of Sprocket Holes (D)

D = 1.5 + 0.1mm

2.5 Distance (E)

E = 1.75 ± 0.1mm

2.6 Distance (F)

LG, LH, LS, DW-20/24/28	F = 11.5 ± 0.1mm
DW-16	F = 7.5 ± 0.1mm

2.7 Dimension (P2)

P2 = 2.0 ± 0.05mm

2.8 Embossed Pocket Dimension (Ao and Bo)

NOTE: These dimensions are measured at 0.3mm above the base of the pocket.

LG	Ao = 15.8 ± 0.1mm
	Bo = 15.8 ± 0.1mm
LH	Ao = 13.1 ± 0.1mm
	Bo = 13.1 ± 0.1mm
LS	Ao = 11.5 + 0.1mm
	Bo = 11.5 + 0.1mm
DW-16	Ao = 10.9 ± 0.1mm
	Bo = 10.7 ± 0.1mm
DW-20	Ao = 10.9 ± 0.1mm
	Bo = 13.2 ± 0.1mm
DW-24	Ao = 10.9 ± 0.1mm
	Bo = 15.8 ± 0.1mm
DW-28	Ao = 10.9 ± 0.1mm
	Bo = 18.3 ± 0.1mm

2.9 Embossed Tape Dimension Ko

LG	Ko = 2.9 ± 0.1mm
LH	Ko = 4.9 ± 0.1mm
LS	Ko = 4.1 ± 0.1mm
DW-16/20/24/28	Ko = 3.0 ± 0.1mm

2.10 Pitch of Component Compartments P1

LG	P1 = 20.0 ± 0.1mm
LH	P1 = 16.0 ± 0.1mm
LS	P1 = 16.0 ± 0.1mm
DW-16/20/24/28	P1 = 12.0 ± 0.1mm

2.11 Outside Dimension of Pocket B1

LG	B1 = 16.5 ± 0.2mm
LH	B1 = 13.9 ± 0.2mm
LS	B1 = 12.2 ± 0.2mm
DW-16	B1 = 11.4 ± 0.2mm
DW-20	B1 = 13.9 ± 0.2mm
DW-24	B1 = 16.5 ± 0.2mm
DW-28	B1 = 18.9 ± 0.2mm

2.12 Pocket Centre Holes D1

LG/LH/LS/DW D1 = 1.55 +1.0mm/-0.05mm

CML Packaging for Despatch .....

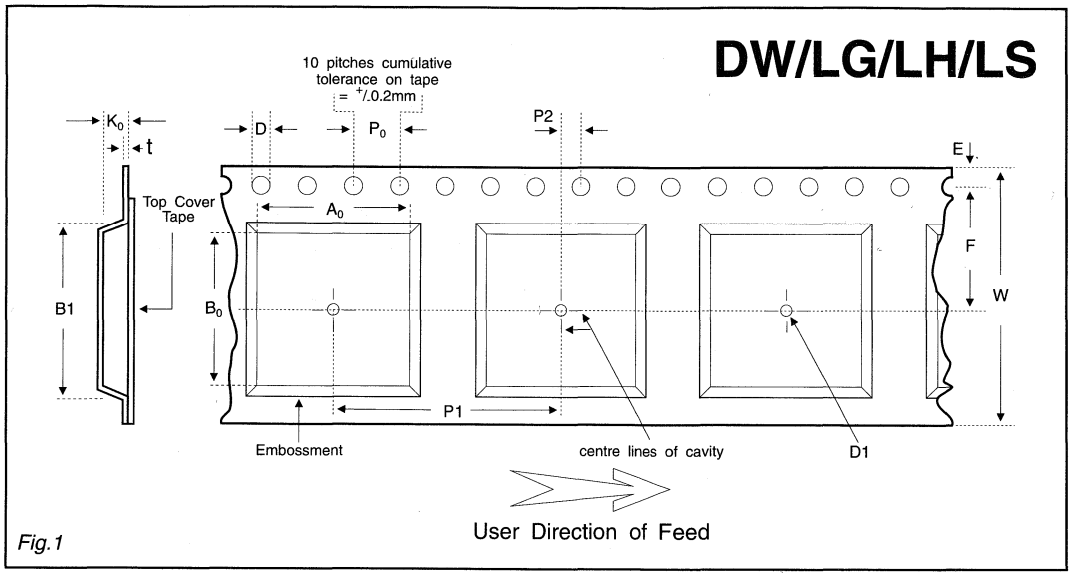


Fig.1

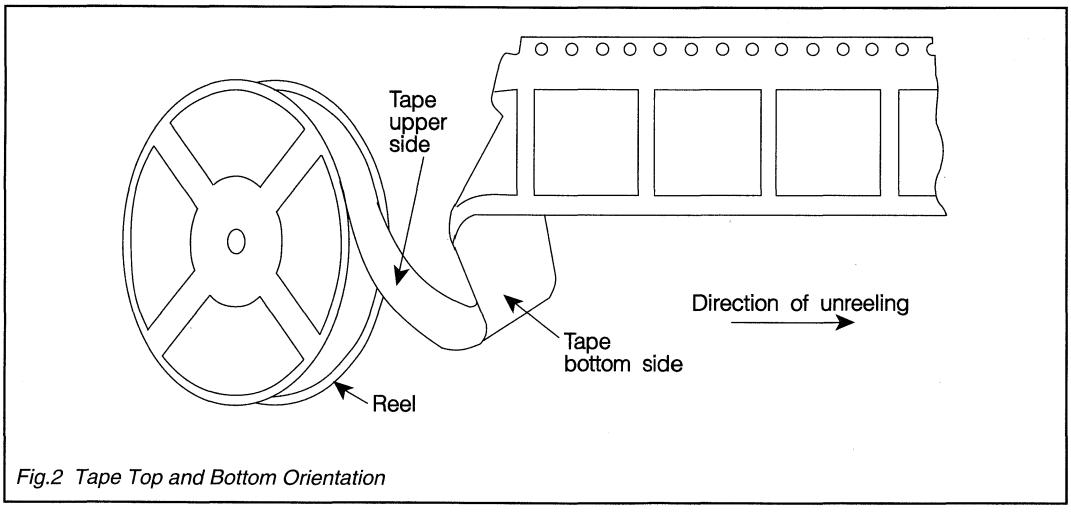


Fig.2 Tape Top and Bottom Orientation

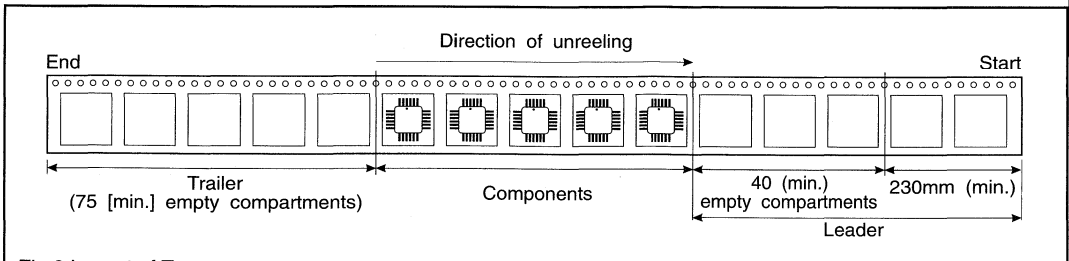


Fig.3 Layout of Tape

3. Materials

3.1 Carrier tape to be made of a conductive grade of polystyrene.

3.2 Conductive polycarbonate is also an approved carrier tape material and may be used under certain circumstances.

3.3 Cover tape is an anti-static grade of polypropylene/polyester or a PET/PE film.

4. Polarity and Orientation of Components in Tape

4.1 All components will be placed such that Pin 1 is adjacent to the sprocket holes (See Figures 6a, 6b and 6c).

4.2 The mounting side of the component shall be oriented to the bottom side of the tape (See Figure 2).

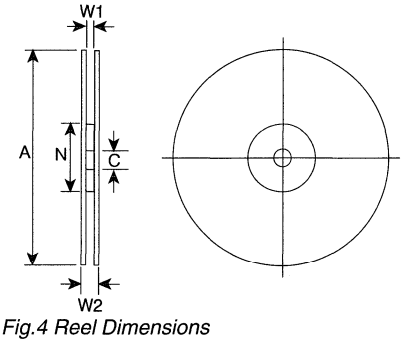


Fig.4 Reel Dimensions

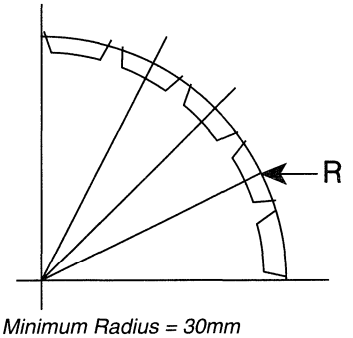


Fig.5 Minimum Radius = 30mm

5. Fixing of Components in Tape

5.1 Cover tapes shall not cover the sprocket holes.

5.2 Tapes in adjacent layers shall not stick together in the packing.

5.3 The adhesive of the cover tape shall not adversely effect the mechanical and electrical characteristics and marking of the components.

5.4 Components shall not stick to the carrier tape or the cover tape.

5.5 The tapes shall be suitable to withstand storage of the taped components without danger or migration of the terminations or the giving off of vapours which would impair soldering or deteriorate the component properties or termination by chemical action.

5.6 When the tape is bent with a minimum radius (See Figure 5) of 30mm, the tape shall not be damaged and the components shall remain in their position and orientation in the tape.

5.7 The peel strength of the cover tape shall be 50 ±25 grams measured at 175° - 180° with respect to the carrier tape along its longitudinal axis. The peel speed shall be 240mm/min.

5.8 After baking at 60°C for 48 hours or storage in ideal conditions for three months, the peel strength shall remain within the specified limits.

Fig.6a

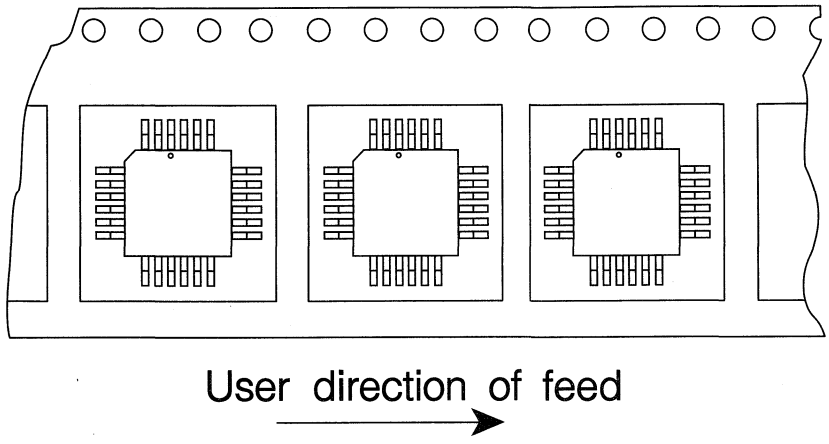


Fig.6b

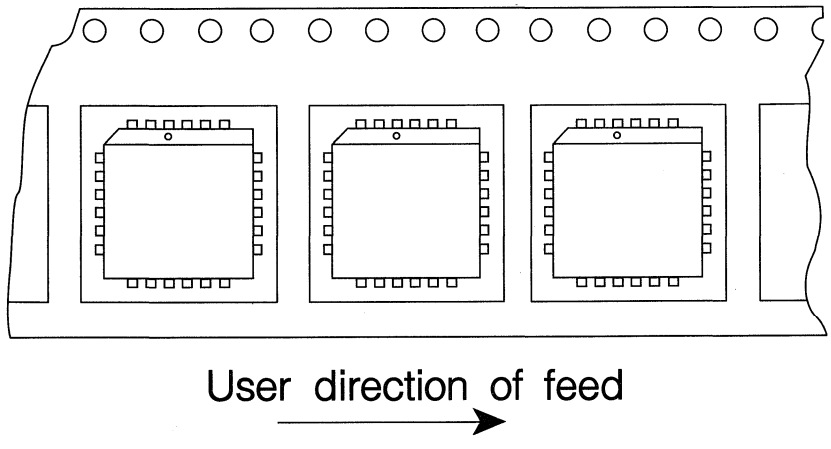


Fig.6c

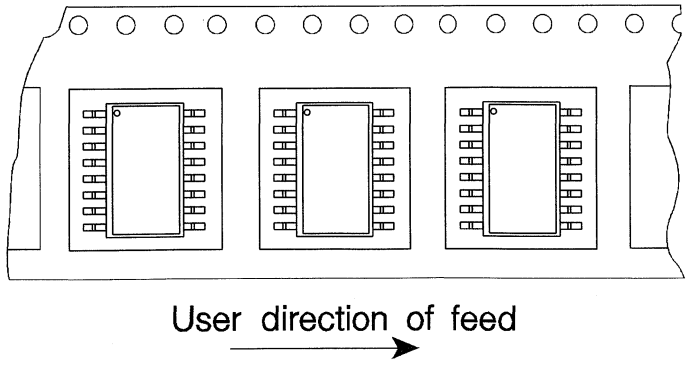


Fig.6 Component Orientation

CML Packaging for Despatch .....

6. Packaging

6.1 Tape will be wound on anti-static plastic reels (See Figure 4)

Dimensions

6.1.1

A	C	N	W1	W2
Reel Dia.	Centre Hole	Hub Outer Dia.	Inside Cheek Width	Outside Cheek Width
330mm	12.7mm	62.5mm	24.5mm	28.8mm

6.2 There will be a leader of a minimum of 230mm followed by 40 empty compartments at the start of the carrier tape (See Figure 3).

6.3 There will be no missing components between the first and last part of working tape in any reel.

6.4 At the end of the tape there will be a trailer of a minimum of 75 empty compartments (See Figure 3).

6.5 The tape shall release from the reel hub as the last portion of the carrier tape unwinds from the reel.

6.6 Components on a reel.

LG = 500
LH = 500
LS = 500
DW = 1,000

6.7 The tape will be prevented from unreeling by winding a paper tape around the reel and fixing with adhesive tape.

6.8 All reels will display:

1. Device Type
2. Quantity on reel
3. Date code
4. A static hazard warning label
5. CML Serial Number

6.9 Reel packed into anti-static bubble bag then in a cardboard box, with appropriate labelling as in paragraph 6.8.

6.10 Ideal storage conditions are 15°C to 20°C with a relative humidity of 60% - 70%.

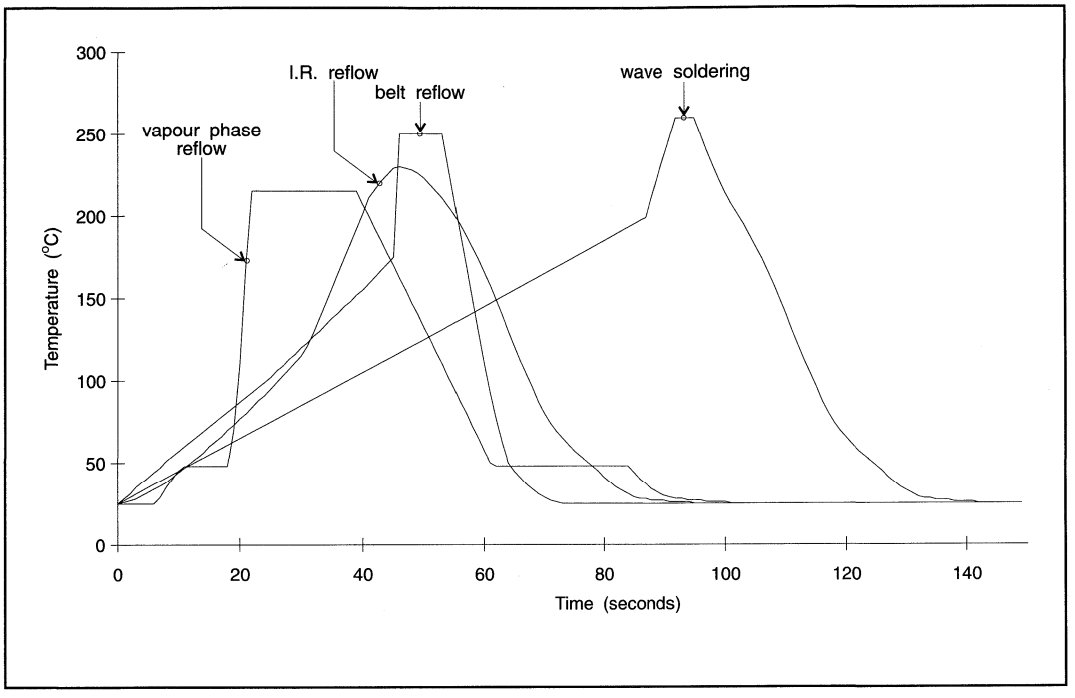
6.11 Shelf-life when stored in ideal conditions will be in excess of six (6) months.

Handling Precautions

CML microcircuits are CMOS LSI devices which include input protection. However precautions should be taken, at all times, to prevent static discharges which may cause device damage.

- It is recommended that the user initially stores and transports the microcircuit in the original supplied packaging.
- At all times observe anti-static precautions including the correct use of a conductive wrist-band and cord.
- Keep benches, personnel and test equipment at the same electrical potential.
- Ensure that the microcircuit is stored and operated well away from any potential source of static discharge.
- Do not insert or remove a microcircuit from an application whilst any power remains applied.
- Whenever possible ensure that the microcircuit is inserted after all other components have been mounted.
- Do not apply signals to a microcircuit until the power supply is suitably established.

CML Microcircuit Soldering Profile



Integrated Circuits Data Book

Section 11

Applications

A collection of recently published CML Application Notes

Generation of Non-Standard CTCSS Tones

CML manufactures several integrated circuits which encode and decode CTCSS tones at the EIA RS-220 standard frequencies. In many instances, however, using tones of slightly different frequencies may be desirable. Because these CML ICs use switched capacitor technology, tone frequencies may be shifted simply by changing the crystal or clock input. The following three tables list alternative tones which can be encoded and decoded by the FX365C and the FX375, and encoded by the FX315.

Each table lists the tone frequencies for three crystal values for each chip. The FX315 and FX365C use a nominal crystal value of 1.0 MHz; the table lists tone frequencies for 1.008 MHz and 1.024 MHz crystals as well as for 1.0 MHz. The FX375 uses a 4.0 MHz nominal crystal value; its table lists frequencies for 4.0 MHz, 4.032 MHz, and 4.096 MHz crystals. The column labeled as "Divisor" for each table lists the quotient of the clock frequency divided by the tone frequency. This column can be used to calculate the clock frequency required to generate other tone frequencies. Each table also lists the (D5-D0) program code input associated with each divisor and tone frequency group. Each code is listed in both binary and hexadecimal formats. As an example, to encode a 70.0 Hz tone with the program code input D_5-D_0 = 011111 (1F Hex), the required clock would be calculated in the following manner:

D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	1	1

Divisor = 13908
Tone frequency = 70.0 Hz
Required clock frequency = Divisor * Tone Frequency
= 13908 * 70.0 Hz
= 973560 Hz

When using these ICs in this manner, you must remember the following:

1) When the clock is changed, the audio pass band limits will change proportionately. These changes will be fairly small, however. For example, in the FX365A using a 1.024 MHz crystal, the lower limit will change to (1.024/1.0) * 300 = 307 Hz, and the upper limit will change to (1.024/1.0) * 3000 = 3072 Hz.

2) In the FX375, the frequency inversion carrier frequency will also change proportionately from its nominal value of 3333 Hz. For example, with a 4.096 MHz clock, the carrier frequency will change to (4.096/4.0) * 3333 Hz = 3413 Hz. For proper communication, the transmitter and receiver must use the same inversion carrier frequency.

Device: FX365C

Divisor	Xtal Freq 1.0 MHz	Xtal Freq 1.008 MHz	Xtal Freq 1.024 MHz	Program Codes Binary D_5	D_4	D_3	D_2	D_1	D_0	Hex
14914	67.05	67.59	68.66	1	1	1	1	1	1	3F
14426	69.32	69.87	70.98	1	1	1	0	0	1	39
13908	71.90	72.48	73.63	0	1	1	1	1	1	1F
13450	74.35	74.94	76.13	1	1	1	1	1	0	3E
12994	76.96	77.58	78.81	0	0	1	1	1	1	0F
12536	79.77	80.41	81.68	1	1	1	1	0	1	3D
12108	82.59	83.25	84.57	0	1	1	1	1	0	1E
11712	85.38	86.06	87.43	1	1	1	1	0	0	3C
11285	88.61	89.32	90.74	0	0	1	1	1	0	0E
10919	91.58	92.31	93.78	1	1	1	0	1	1	3B
10553	94.76	95.52	97.03	0	1	1	1	0	1	1D
10279	97.29	98.07	99.62	1	1	1	0	1	0	3A
10004	99.96	100.76	102.36	0	0	1	1	0	1	0D
9668	103.43	104.26	105.91	0	1	1	1	0	0	1C
9333	107.15	108.01	109.72	0	0	1	1	0	0	0C
9028	110.77	111.66	113.43	0	1	1	0	1	1	1B
8723	114.64	115.56	117.39	0	0	1	0	1	1	0B
8418	118.80	119.75	121.65	0	1	1	0	1	0	1A
8143	122.80	123.78	125.75	0	0	1	0	1	0	0A
7869	127.08	128.10	130.13	0	1	1	0	0	1	19
7595	131.67	132.72	134.83	0	0	1	0	0	1	09
7320	136.61	137.70	139.89	0	1	1	0	0	0	18
7076	141.32	142.45	144.71	0	0	1	0	0	0	08
6832	146.37	147.54	149.88	0	1	0	1	1	1	17
6619	151.09	152.30	154.72	0	0	0	1	1	1	07
6374	156.88	158.14	160.65	0	1	0	1	1	0	16
6161	162.31	163.61	166.21	0	0	0	1	1	0	06
5947	168.14	169.49	172.18	0	1	0	1	0	1	15
5764	173.48	174.87	177.64	0	0	0	1	0	1	05
5551	180.15	181.59	184.47	0	1	0	1	0	0	14
5368	186.29	187.78	190.76	0	0	0	1	0	0	04
5185	192.86	194.40	197.49	0	1	0	0	1	1	13
4910	203.65	205.28	208.54	0	0	0	0	1	1	03
4758	210.17	211.85	215.21	0	1	0	0	1	0	12
4575	218.58	220.33	223.83	0	0	0	0	1	0	02
4422	226.12	227.93	231.55	0	1	0	0	0	1	11
4270	234.19	236.06	239.81	0	0	0	0	0	1	01
4148	241.08	243.01	246.87	0	1	0	0	0	0	10
3996	250.28	252.28	256.29	0	0	0	0	0	0	00

Device: FX375

Divisor	Xtal Freq 4.0 MHz	Xtal Freq 4.032 MHz	Xtal Freq 4.096 MHz	Program Codes Binary D_5	D_4	D_3	D_2	D_1	D_0	Hex
59657	67.05	67.59	68.66	1	1	1	1	1	1	3F
55633	71.90	72.48	73.63	0	1	1	1	1	1	1F
53800	74.35	74.94	76.13	1	1	1	1	1	0	3E
51975	76.96	77.58	78.81	0	0	1	1	1	1	0F
50144	79.77	80.41	81.68	1	1	1	1	0	1	3D
48432	82.59	83.25	84.57	0	1	1	1	1	0	1E
46849	85.38	86.06	87.43	1	1	1	1	0	0	3C
45142	88.61	89.32	90.74	0	0	1	1	1	0	0E
43678	91.58	92.31	93.78	1	1	1	0	1	1	3B
42212	94.76	95.52	97.03	0	1	1	1	0	1	1D
41114	97.29	98.07	99.62	1	1	1	0	1	0	3A
40016	99.96	100.76	102.36	0	0	1	1	0	1	0D
38673	103.43	104.26	105.91	0	1	1	1	0	0	1C
37331	107.15	108.01	109.72	0	0	1	1	0	0	0C
36111	110.77	111.66	113.43	0	1	1	0	1	1	1B
34892	114.64	115.56	117.39	0	0	1	0	1	1	0B
33670	118.80	119.75	121.65	0	1	1	0	1	0	1A
32573	122.80	123.78	125.75	0	0	1	0	1	0	0A
31476	127.08	128.10	130.13	0	1	1	0	0	1	19
30379	131.67	132.72	134.83	0	0	1	0	0	1	09
29280	136.61	137.70	139.89	0	1	1	0	0	0	18
28305	141.32	142.45	144.71	0	0	1	0	0	0	08
27328	146.37	147.54	149.88	0	1	0	1	1	1	17
26474	151.09	152.30	154.72	0	0	0	1	1	1	07
25497	156.88	158.14	160.65	0	1	0	1	1	0	16
24644	162.31	163.61	166.21	0	0	0	1	1	0	06
23790	168.14	169.49	172.18	0	1	0	1	0	1	15
23057	173.48	174.87	177.64	0	0	0	1	0	1	05
22204	180.15	181.59	184.47	0	1	0	1	0	0	14
21472	186.29	187.78	190.76	0	0	0	1	0	0	04
20740	192.86	194.40	197.49	0	1	0	0	1	1	13
19642	203.65	205.28	208.54	0	0	0	0	1	1	03
19032	210.17	211.85	215.21	0	1	0	0	1	0	12
18300	218.58	220.33	223.83	0	0	0	0	1	0	02
17690	226.12	227.93	231.55	0	1	0	0	0	1	11
17080	234.19	236.06	239.81	0	0	0	0	0	1	01
16592	241.08	243.01	246.87	0	1	0	0	0	0	10
15982	250.28	252.28	256.29	0	0	0	0	0	0	00

Device: FX315A

Divisor	Xtal Freq 1.0 MHz	Xtal Freq 1.008 MHz	Xtal Freq 1.024 MHz	Program Codes Binary D_5	D_4	D_3	D_2	D_1	D_0	Hex
14912	67.06	67.60	68.67	1	1	1	1	1	1	3F
14415	69.37	69.93	71.04	1	1	1	0	0	1	39
13920	71.84	72.41	73.56	0	1	1	1	1	1	1F
13454	74.33	74.92	76.11	1	1	1	1	1	0	3E
12989	76.99	77.61	78.84	0	0	1	1	1	1	0F
12555	79.65	80.29	81.56	1	1	1	1	0	1	3D
12121	82.50	83.16	84.48	0	1	1	1	1	0	1E
11718	85.34	86.02	87.39	1	1	1	1	0	0	3C
11284	88.62	89.33	90.75	0	0	1	1	1	0	0E
10943	91.38	92.11	93.57	1	1	1	0	1	1	3B
10540	94.88	95.64	97.16	0	1	1	1	0	1	1D
10261	97.46	98.24	99.80	1	1	1	0	1	0	3A
10013	99.87	100.67	102.27	0	0	1	1	0	1	0D
9672	103.39	104.22	105.87	0	1	1	1	0	0	1C
9331	107.17	108.03	109.74	0	0	1	1	0	0	0C
9021	110.85	111.74	113.51	0	1	1	0	1	1	1B
8711	114.80	115.72	117.56	0	0	1	0	1	1	0B
8432	118.60	119.55	121.45	0	1	1	0	1	0	1A
8122	123.12	124.10	126.07	0	0	1	0	1	0	0A
7843	127.50	128.52	130.56	0	1	1	0	0	1	19
7595	131.67	132.72	134.83	0	0	1	0	0	1	09
7316	136.69	137.78	139.97	0	1	1	0	0	0	18
7068	141.48	142.61	144.88	0	0	1	0	0	0	08
6851	145.96	147.13	149.46	0	1	0	1	1	1	17
6603	151.45	152.66	155.08	0	0	0	1	1	1	07
6386	156.59	157.84	160.35	0	1	0	1	1	0	16
6169	162.10	163.40	165.99	0	0	0	1	1	0	06
5952	168.01	169.35	172.04	0	1	0	1	0	1	15
5766	173.43	174.82	177.59	0	0	0	1	0	1	05
5549	180.21	181.65	184.54	0	1	0	1	0	0	14
5363	186.46	187.95	190.94	0	0	0	1	0	0	04
5177	193.16	194.71	197.80	0	1	0	0	1	1	13
4929	202.88	204.50	207.75	0	0	0	0	1	1	03
4836	206.78	208.44	211.75	1	1	1	0	0	0	38
4743	210.84	212.53	215.90	0	1	0	0	1	0	12
4588	217.96	219.70	223.19	0	0	0	0	1	0	02
4433	225.58	227.38	230.99	0	1	0	0	0	1	11
4278	233.75	235.62	239.36	0	0	0	0	0	1	01
4123	242.54	244.48	248.36	0	1	0	0	0	0	10
3999	250.06	252.06	256.06	0	0	0	0	0	0	00

The EIA RS-220 specification divides the standard frequencies into three groups. They are tabulated below with the program codes used in CML ICs:

Group A	
Freq	**Code**
67.0	3F
77.0	0F
88.5	0E
100.0	0D
107.2	0C
114.8	0B
123.0	0A
131.8	09
141.3	08
151.4	07
162.2	06
173.8	05
186.2	04
203.5	03
218.1	02
233.6	01
250.3	00

Group B	
Freq	**Code**
71.9	1F
82.5	1E
94.8	1D
103.5	1C
110.9	1B
118.8	1A
127.3	19
136.5	18
146.2	17
156.7	16
167.9	15
179.9	14
192.8	13
210.7	12
225.7	11
241.8	10

Group C	
Freq	**Code**
74.4	3E
79.7	3D
85.4	3C
91.5	3B
97.4	3A
69.3	39
206.5	38

Note that with the exception of the 67.0 Hz tone in Group A, the programming codes are in reverse sequential order in relation to the tone frequencies for each group. Again, with the exception of 67.0 Hz, also note that the first hexadecimal digit for Group A is 0, the first digit for Group B is 1, and the first digit for group C is 3.

For more general information about these ICs, see the relevant Data Sheets.

CML does not test its CTCSS ICs (FX315, FX365C, FX375) at crystal or clock frequencies other than the nominal frequency specified in the Data Sheets, and as such, makes no guarantee of the performance of the device when used with a non-specified crystal or clock frequency.

CML does not assume responsibility for the use of its ICs in the manner described in this application note in any circuit or product.

Squelch Tail Elimination in CTCSS Systems

The Problem *(with reference to Figure 1)*

When in receive mode and the received carrier drops, the CTCSS decoder takes a finite time to de-respond. If an Rx Tone Decode Output is used to control the Rx audio path this sudden RF carrier loss results in FM noise generated by the receiver being passed through the audio stages to the loudspeaker as the audio gate remains open for the majority of the CTCSS Decoder de-response period.

The resultant effect is an annoying short-duration noise burst being heard at the receiver every time the received carrier drops; this is commonly known as the CTCSS "Squelch Tail".

Methods of Removing The "Squelch Tail"

Carrier Sense "AND" CTCSS

If the design of the receiving equipment makes available an RF carrier-detect output, it is effectively possible to remove the Squelch Tail by logically "ANDing" the RF carrier-detect output with the CTCSS Rx Tone Decode Output and using the result of this logic process to control the Rx audio gate.

Tx Control/CTCSS Encode Control *(with reference to Figure 2)*

In the Tx side of the system, when the PTT is released the CTCSS tone generator is switched off but transmission of the RF carrier is continued for a short period of time. This allows the CTCSS decoder in the receiver to de-respond and remove the Rx audio prior to FM noise being generated at the Rx discriminator.

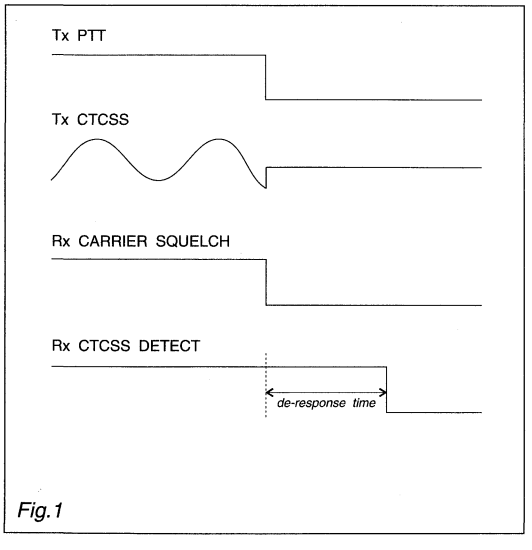


Fig.1

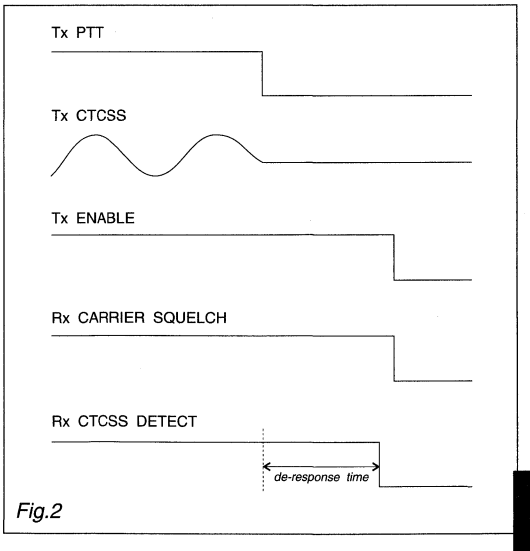


Fig.2

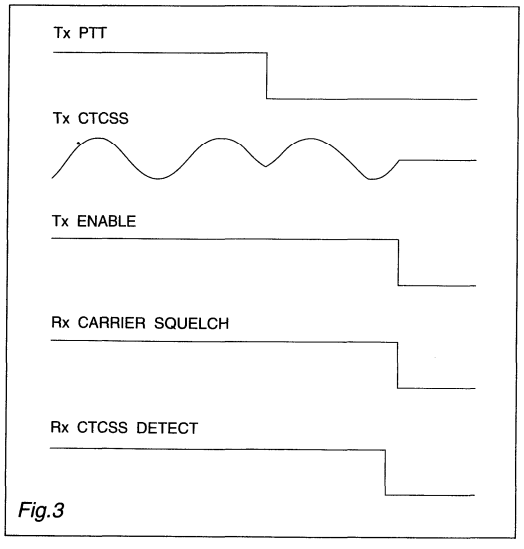


Fig.3

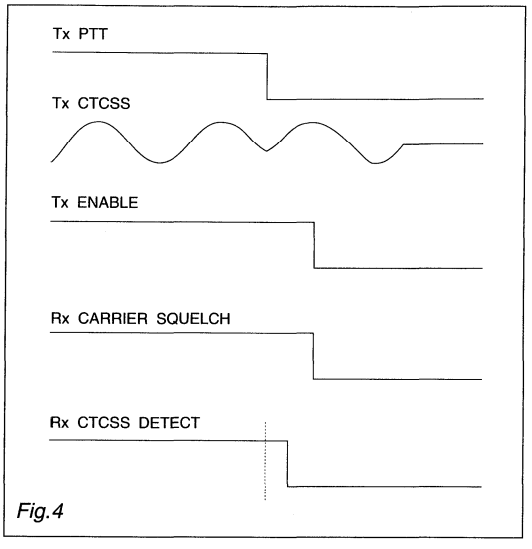


Fig.4

Tx Tone Phase Reversal *(with reference to Figure 3)*

It is possible to reduce the de-response time and eliminate the squelch tail by reversing the phase of the transmitted CTCSS tone for a short period of time at the end of the transmission. In effect this forces the CTCSS decoder to de-respond quickly by feeding the signal in antiphase for a short duration.

It should be noted that the length of time the antiphase tone is applied is dependent upon a number of variables, in particular:

- The frequency of the CTCSS tone in use and the time taken for the CTCSS tone to decay and ramp-up again in reverse phase; these are typically:

67.05Hz	≈	70ms
103.43Hz	≈	50ms
162.31Hz	≈	35ms
250.28Hz	≈	25ms

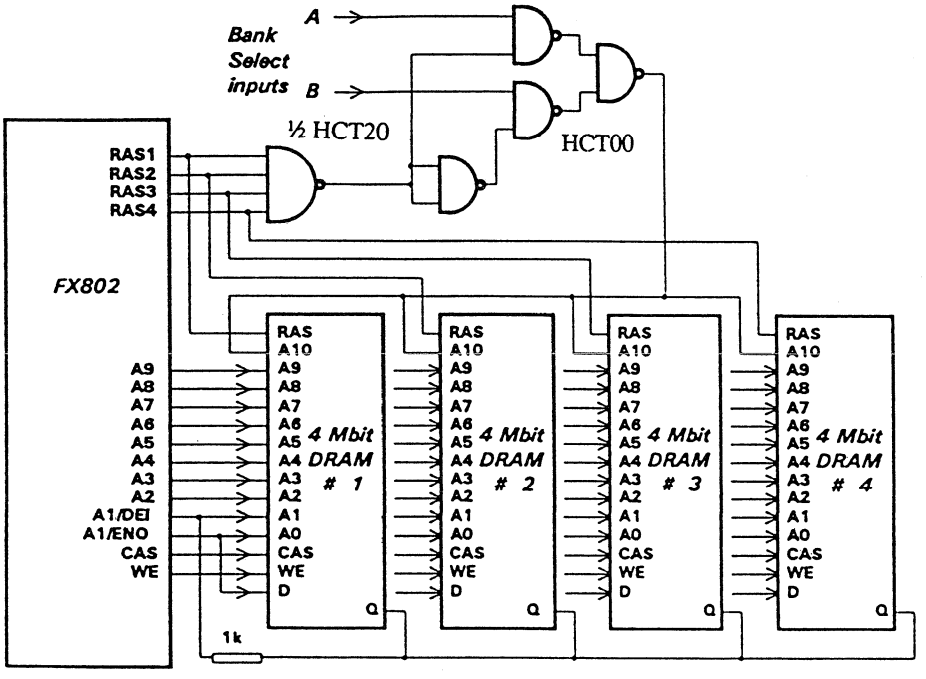
Designers should be aware that when the reversed phase tone is applied for too long the CTCSS decoder will initially de-respond and close the audio gate and then shortly after re-respond to the 'new' anti-phase tone and again open the receiver's audio gate.

Tx Tone Phase Reversal Detection *(with reference to Figure 4)*

The Tx tone phase reversal facility is employed together with a phase-detector in the receiver. The receiver works as normal using the CTCSS tone to control the opening of the audio gate. However, whenever the phase-detector detects a CTCSS tone phase reversal it immediately closes the audio gate eliminating the squelch tail in the minimum time possible.

The use of 4MBit DRAM with the FX802 DVSR Codec

Figure 1 FX802 connection to 4 x 4 Mbit. DRAMS for applications requiring up to 16 Mbits of memory. Each DRAM is divided in to 4 banks, selected by static 'Bank Select' lines A + B.



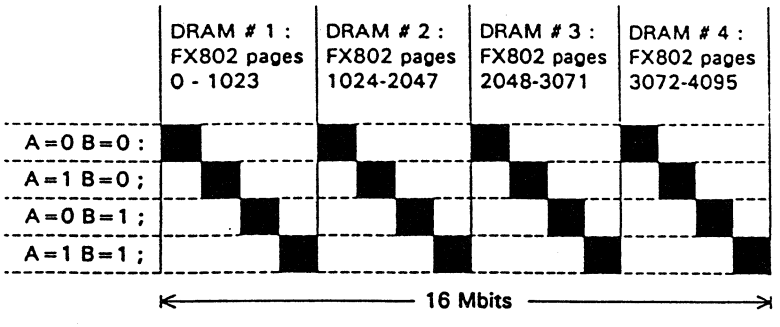


Figure 2 FX802 Connection to a standard 4 Mbit DRAM. The 4 Mbit DRAM is divided into 4 off 1 Mbit banks, selected by static 'Bank Select' lines A and B.

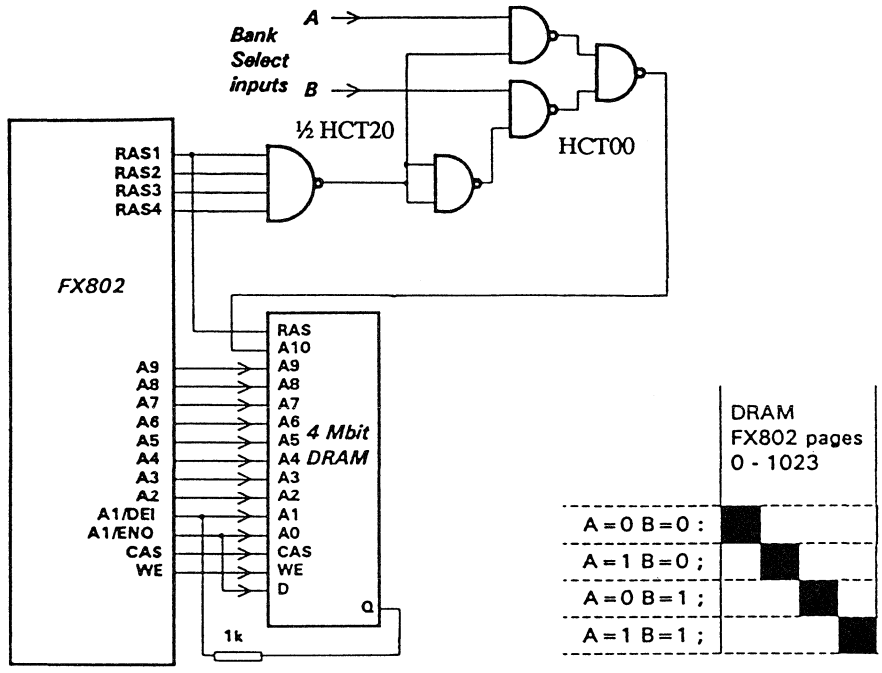
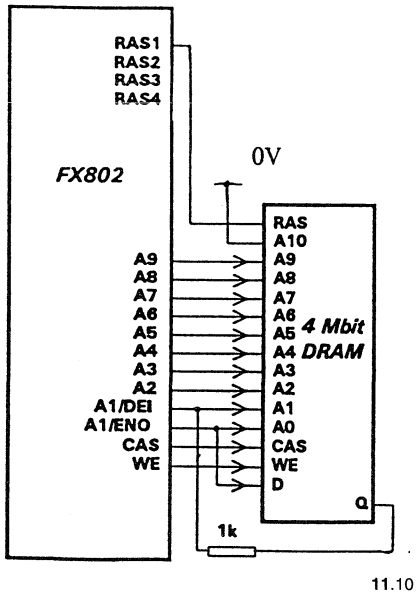


Figure 3 FX802 Connection to a standard 4 Mbit DRAM where an application requires less than 1 Mbit of memory.



CM1481 Base Notes

This document describes how a base station might be programmed in order to use the over-air features of the CM1481 selcall module. This document should be read in conjunction with the Data Sheet supplied with the Module.
Before a base station is to be used in this manner it must be able to achieve the following:

1. Transmit selcall tone sequences up to 16 tones long.
2. Receive and process selcall tone sequences up to 11 tones long.
3. Prompt the operator for an input.
4. To be programmable (add extra functionality. eg. a Pseudo Random Number Generator).
5. Have a real-time timer (to operate a 15 second time out).

The transaction security relies on two Pseudo Random Number Generators (PRNG details in Data Sheet) running in parallel; the number of iterations to run the PRNG through is stored in the EEPROM on the module and prompted for at the base. Therefore the base operator MUST have a record of which modules (ie mobiles) have which iteration numbers. If the base operator types in the incorrect number of iterations then the over-air operation will fail at the security checking.

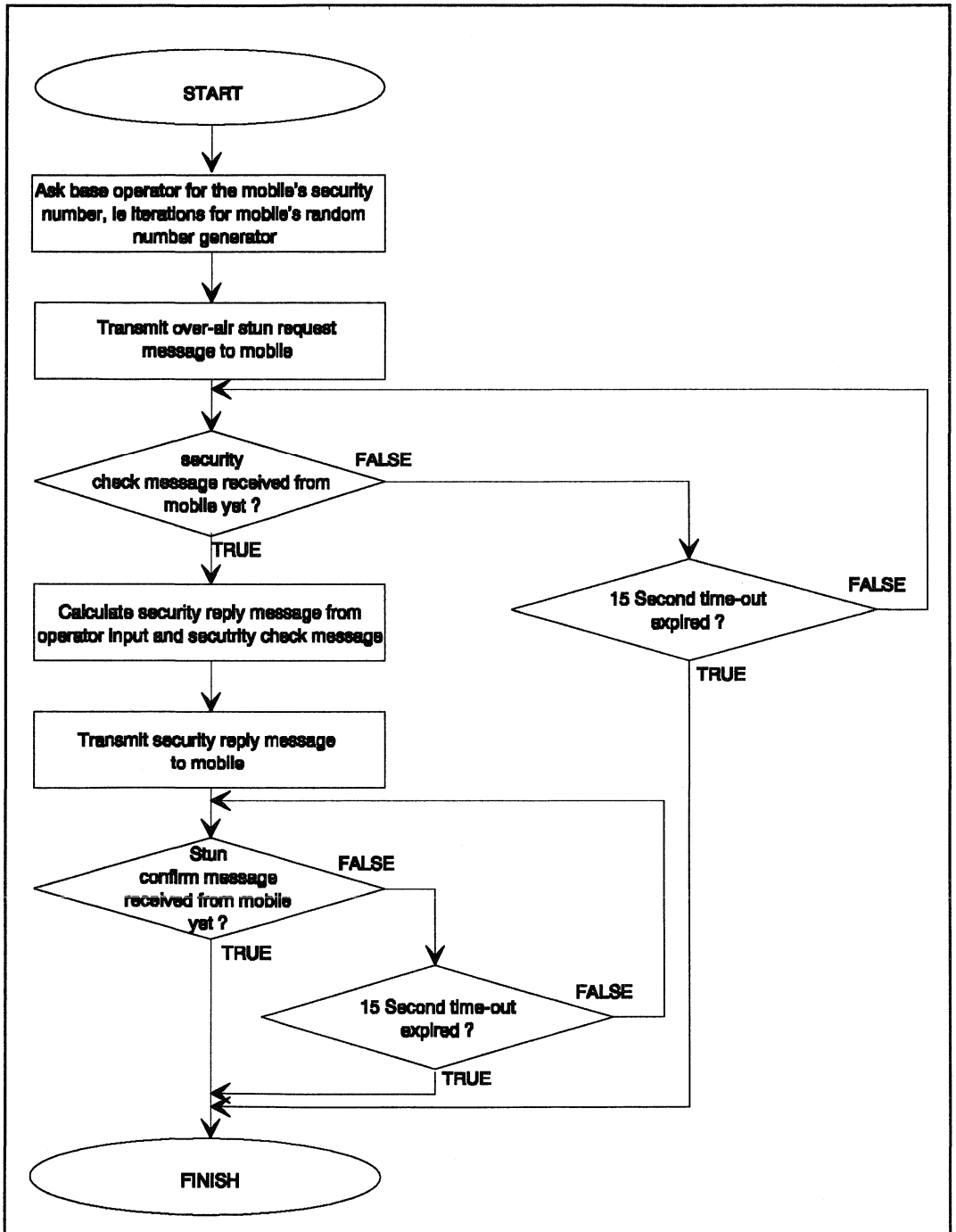
The whole operation MUST be completed inside 15 seconds, if this does not happen the module will time-out and return to its previous state (ie the state it was in before the over-air operation was tried), therefore the base station must run a timer to check that the over-air operation has not taken more than 15 seconds (to carry on would be pointless if the module at the other end has returned to its previous state).

If the base station is to perform an over-air re-configuration, as well as prompting for the number of iterations the base must also prompt for the parameter to be re-configured and its new value. All the base operator input must be decided and formatted before the over-air operation is started in order not to exceed the 15 second time limit.

If the base station transmits an incorrect security reply it still has until the 15 second time-out expires to transmit the correct reply. After the 15 seconds time-out the base will need to re-initiate the operation.

If the operation fails due to no confirm message being received it may be that the mobile is no longer receiving or has its over-air features disabled (configured as such).

If the Tx address of a mobile is being re-configured, if the operation is successful then the confirm message will be headed by the new Tx address.



The steps that a base station might perform in order to stun a mobile unit over-air

Fitting the CM1481 Selcall Module To A 'KEY KME Series' PMR

Figure 1 shows the interconnection between the facility socket inside the Key KME PMR and the connector on the CM1481 Selcall Module.
This document is to be read in conjunction with the current CM1481 Operating And Programming Manual (Publication D/1481/) and the Key KME PMR Technical Manual.

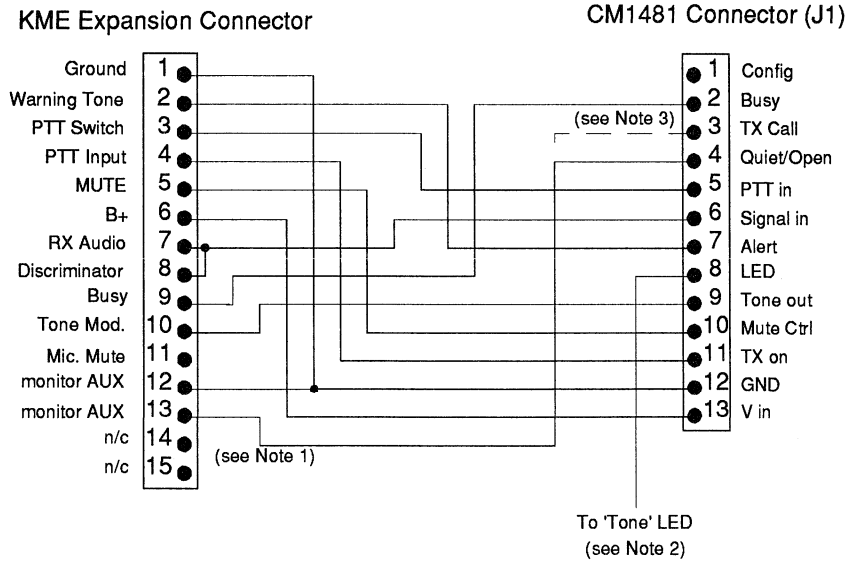


Fig. 1 Interconnection Between CM1481 Selcall Module And Key KME Series PMR

Note

1. The Key KME PMR has a latching switch on the front panel labelled 'AUX'. This uncommitted switch is utilised to operate the CM1481. The requirement for switches that are connected to pins 3 (Tx Call) or pin 4 (Quiet/Open) on the CM1481 connector is that they should be non-latching types, it is recommended the 'AUX' switch be replaced by a non-latching type.
2. The Key KME PMR has an LED on the front panel labelled 'Tone'. This can be connected to the CM1481 in one of two ways:

1. The CM1481 LED output pin can be directly connected to the 'Tone' LED. This may require soldering a wire onto the front panel PCB of the Key KME PMR (see Key KME PMR Technical Manual). The 'Tone' LED is supplied with 13.8V (from the radio) and is illuminated by grounding the other pin, however the LED output from the CM1481 only varies between 0V and 5V (i.e. logic low and logic high), this means that the effect of this connection is that the CM148 instead of switching the 'Tone' LED ON or OFF, merely changes its brightness.
   When the CM1481 LED output is at 0V (i.e. logic low), the voltage drop across the 'Tone' LED is about 13.8V, therefore the 'Tone' LED appears illuminated.
   When the LED output from the CM1481 is 5V (i.e. logic high) the voltage drop across the LED is reduced to around 8.8V, therefore the 'Tone' LED remains illuminated but its brightness is reduced.
   It is recommended that the LED output from the CM1481 is configured to be active low (CM1481 configuration, see manual for details), then the 'Tone' LED will have the function:

'Tone' LED State	**Meaning**
Dim illumination	CM1481 Selcall Unit Present in the radio
Alternating dim/bright	CM1481 Selcall Unit has decoded its Rx address - the radio is being called -
Not illuminated	N/A

2. This method of connection allows correct on/off operation of the 'Tone' LED.
   The CM1481 LED output can be used to switch the 'Tone' LED on or off by an extra switching transistor. Fig. 2 shows how an extra transistor can be used to allow the logic LED output from the CM1481 to switch the 'Tone' LED on or off.

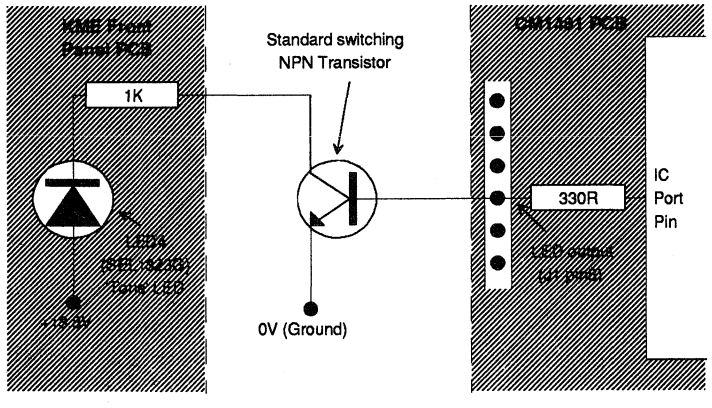


Fig. 2 Additional Changes Between The CM1481 LED output and the Front Panel 'Tone' LED

If the LED connection is performed in this way then it is recommended that the CM1481 LED output should be configured as active high (done by configuring the CM1481, see manual for details), then the 'Tone' LED will have the function:

'Tone' LED State	Meaning
Not Illuminated.	CM1481 has not decoded its Rx address - the radio has not been called -
Flashing.	CM1481 has decoded its Rx address - the radio is being called -

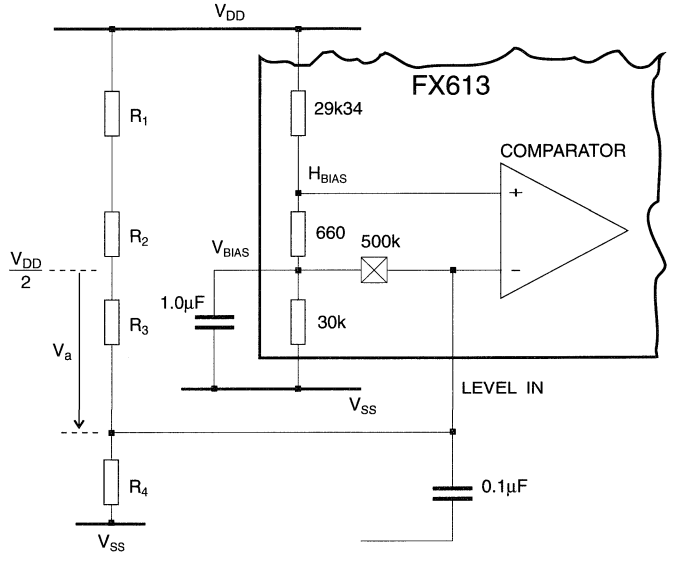
3. In order for the CM1481 to operate fully with one switch, it is necessary to configure the CM1481 operation as 'single button'.
4. The link (i.e. zero ohms shunt) on the alert output stage of the CM1481 must be removed. Alerts are fed to an audio amplifier stage and therefore a high impedance output is required (see CM1481 manual Figure 4 PCB Layout for location of the link).

FX613 Sensitivity Threshold Adjustment

The sensitivity threshold is the difference between the 'must' and 'must not' decode levels. Currently, as defined in the FX613 Data Sheet this is set to 20.8 dB.

In many applications a smaller sensitivity threshold range is required, for example 12.0dB or 6.0dB. This Application Note describes how this can be achieved by the use of a simple external resistor chain.

Fig.1



Note:

1. R_1, R_2 and R_3 could be replaced with a single resistor. In the example given this would be a resistor of value 35.0kΩ.

2. The overall sensitivity threshold range can be reduced by simply attenuating the signal input.

FX613 Sensitivity Threshold Adjustment .....

The Data Sheet Specification

V_{DD}	Must Decode Level			Must Not Decode Level			Sensitivity Threshold
(V)	(dBu)	(mVp-p)	(mVp)	(dBu)	(mVp-p)	(mVp)	(dB)
3.3	-25.2	120	60	-46	11	5.5	20.8
5.0	-21.6	181.8	90.0	-42.4	16.7	8.35	20.8

Example, to reduce the Sensitivity Threshold to 6.0dB
By adjusting the dc level (-ve I/P of the comparator) of LEVEL IN pin with external resistors, see Figure 1; Va is referenced to V_{BIAS} ($V_{DD}/2$).

At 5.0V:
Sensitivity Threshold = (90.9mVp + Va)/ (8.35mVp + Va) = 2 = 6.0dB
Va = 74.2mVp

For 6.0 dB Sensitivity Threshold:

Must Decode level	=	165.1mVp	=	330.2mVp-p	=	-16.44 dBu
Must Not Decode level	=	82.55mVp	=	165.1mVp-p	=	-22.46 dBu

External Resistors

Referrence to Figure 1. The resistor selection criteria:

1. $R_1 + R_2 + R_3 + R_4 <= 70k\Omega$
2. $R_1 + R_2 = R_3 + R_4$

For the above example of 6.0dB, sensitivity threshold =

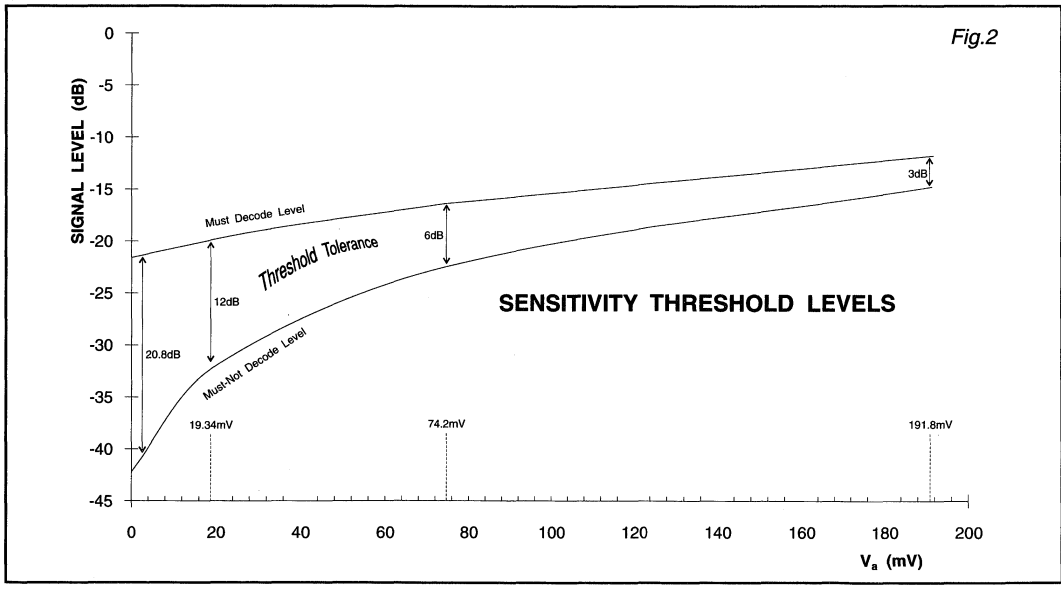
Va = $R_3/(R_3 + R_4)$ x 2.5Vp = 74.2mVp

R3 = $(R_3 + R_4)$ x 74.2mVp/2.5Vp

which gives

R4 = 33 x R3

If R_3 = 1kΩ then R_4 = 33kΩ and $R_1 + R_2$ = 34kΩ, or $R_1 + R_2 + R_3$ = 35kΩ.



FX631 Low-Power SPM Detector

External Component Value Calculation -A Worked Example

German 16kHz FTZ Specification:

Must Not Decode level = -27dB
Must Decode Level = -21dB

Using the graph supplied in the FX631 Data Sheet and following steps 1, 2 and 3, the required 'gain-range' of -3.25 to -6.5 dB is obtained. Note.This graph is for a V_{DD} of 3.3V.

For 5.0V V_{DD} operation the graph provided in Figure 4 of this Application Note should be used.
This will provide a 'gain-range' of -0.25dB to -2.75dB.

Using the 'gain-range' for 5.0V V_{DD}, the mid-point gives a gain requirement of -1.5 dB.

Assuming a Differential Input:

$R_4 = R_1$
$C_4 = C_3$
$R_3 = R_2$

The amplifier gain (G) is set by: $G = \frac{R_1}{(R_2 + X^{C3})}$ = -1.5 dB or 0.8414

For a system frequency of 16kHz and an input capacitor value of 330pF.

$$X^{C3} = \frac{1}{2\Pi \times 16000 \times 330 \times 10^{-12}} = 30.143k\Omega$$

The FX631 data sheet suggests $R_1 = 100k\Omega$

Using $G = \frac{R_1}{(R_2 + X^{C3})}$ by transposition and calculation; $R_2 = 88.0k\Omega$

This can be made from 20.0kΩ and 68.0kΩ resistors in series; diodes are only required if line protection is not included elsewhere in the telecoms circuit (see FX631 Data Sheet).

See Figure 1 for worked values.

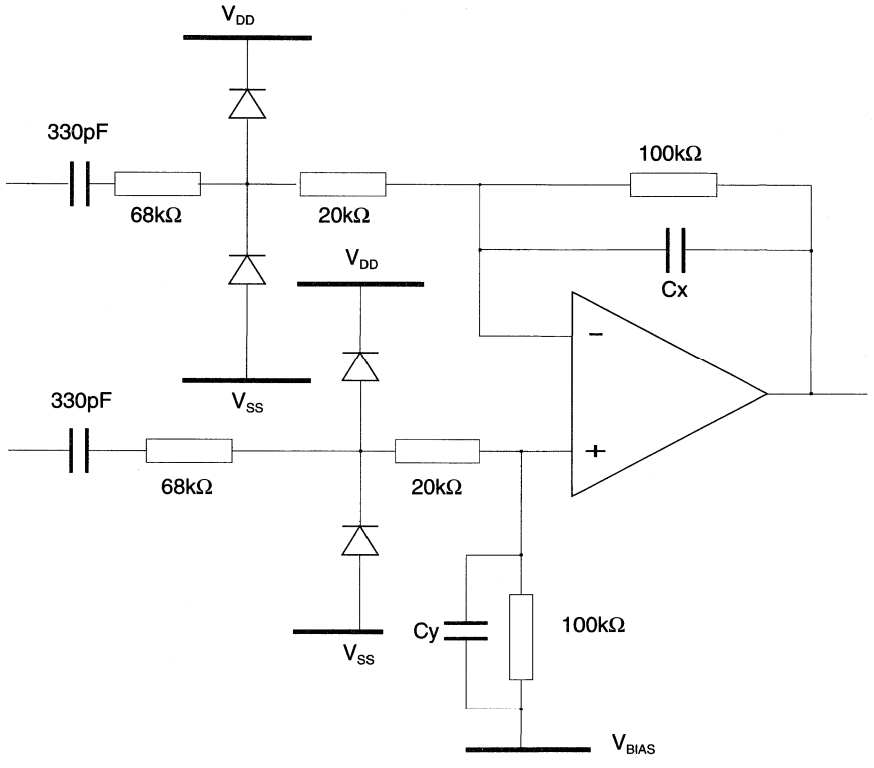


Fig.1 Worked Values

Cx and Cy are required if aliasing is a problem. See Data Sheet.

Diodes are only required if line protection is not included elsewhere in the circuit (see Data Sheet).

External Components

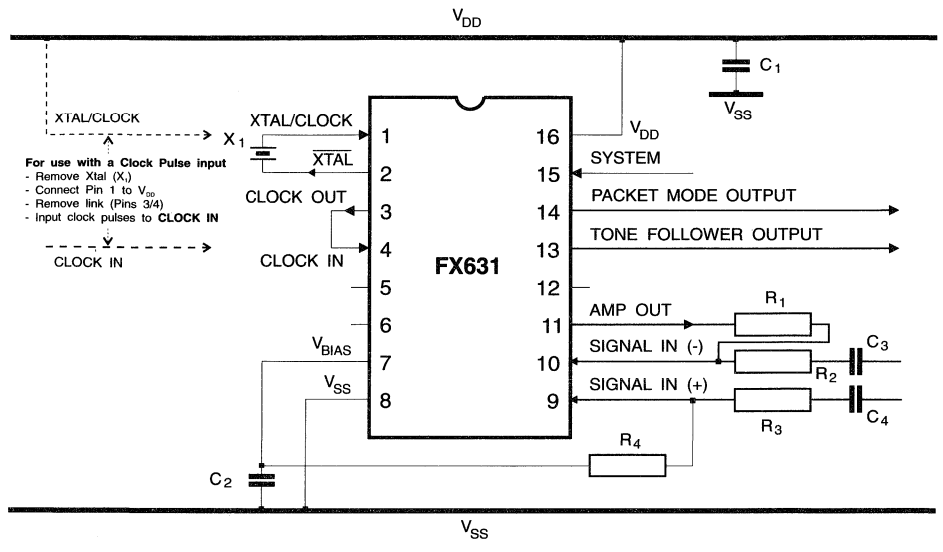


Fig.2 Recommended External Components - Differential Input Mode

Component	Value
R_1	$R_{FEEDBACK}$
R_2	$R_{IN(-)}$
R_3	$R_{IN(+)}$
R_4	R_{BIAS}
C_1	1.0µF ±20%
C_2	1.0µF ±20%
C_3	$C_{IN(-)}$
C_4	$C_{IN(+)}$
X_1	3.579545MHz

External Components

1. The values of the Input Amp gain components illustrated are calculated using the Input Gain Calculation Graph (Figure 4).
   Whilst calculating input gain components, for correct operation, it is recommended that the values of resistors R_1 and R_4 are always greater than, or equal to, 100kΩ.

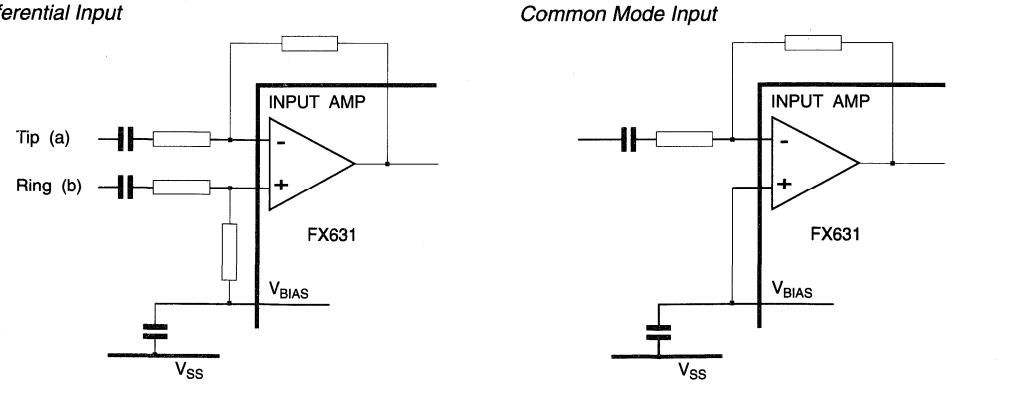


Fig.3 Example Input Configurations

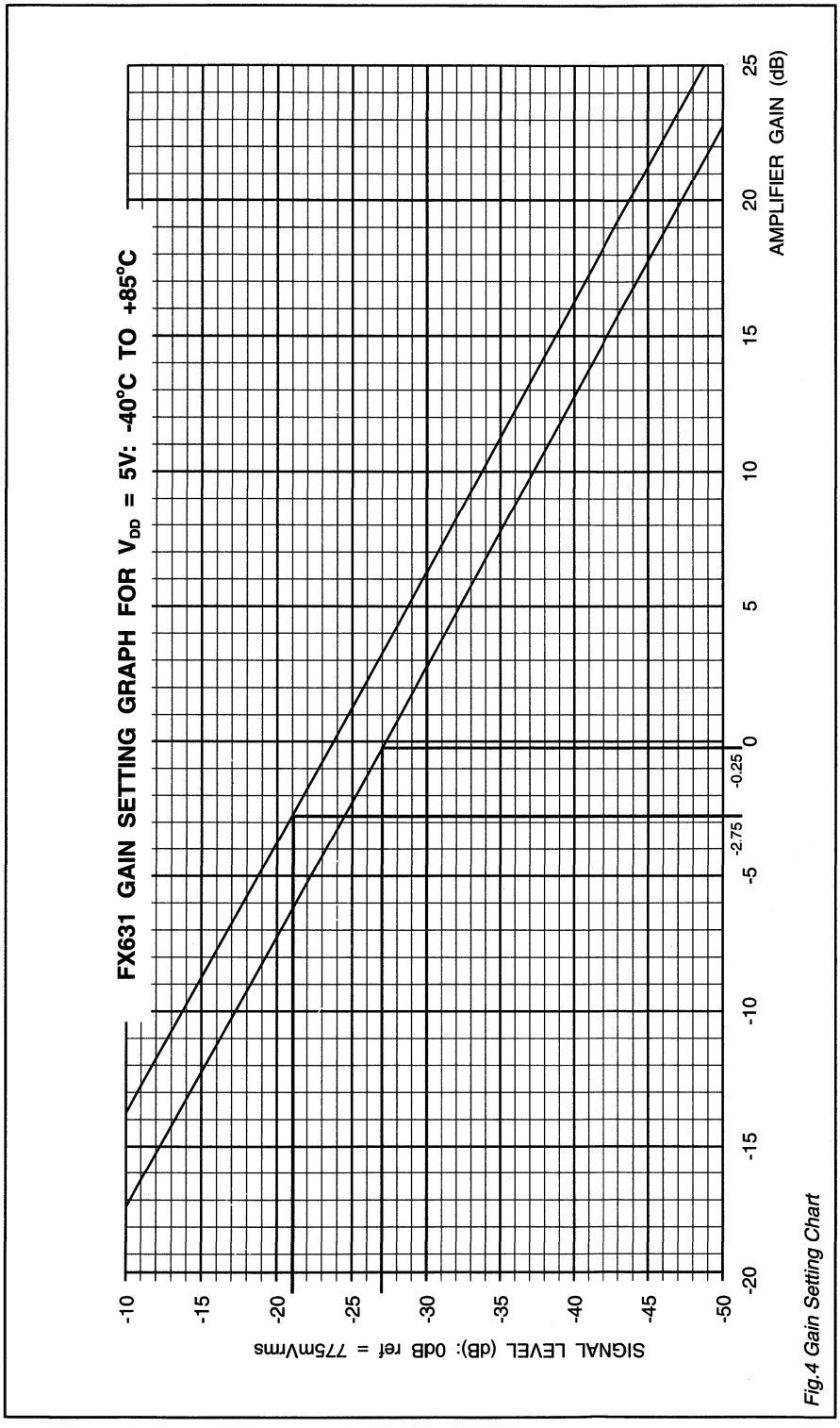


Fig.4 Gain Setting Chart

Téléphone à carte SPM Detector

- A dual (12kHz and 18kHz) tone detector circuit -

This Application Note describes how two FX631 Low-Voltage (Subscriber Pulse Metering) SPM Detector microcircuits can be used, with additional external filter components, to detect both the 12kHz SPM and the 18kHz security tones employed in the French payphone/cardphone system. This Application Note must be read in conjunction with the current FX631 Data Sheet.

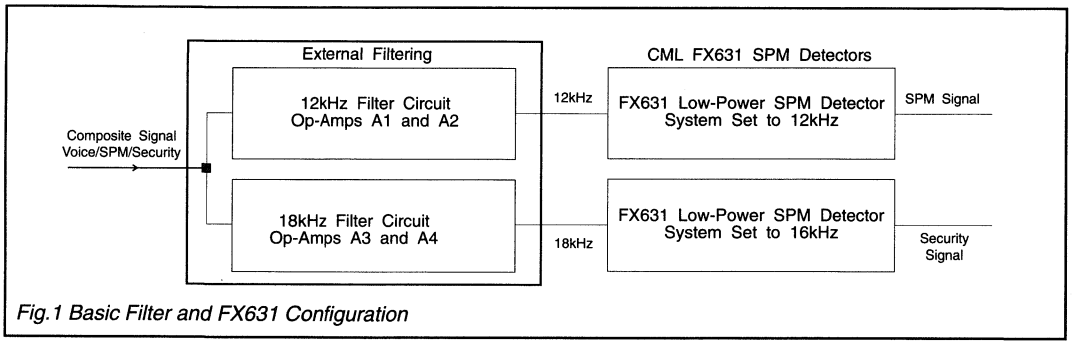


Fig.1 Basic Filter and FX631 Configuration

The Circuit

The telephone signal will consist of voice, 12kHz SPM pulses and an 18kHz security system signal.

The current FX631 design allows it to completely reject voice frequencies but, the close proximity of the 12kHz and 18kHz frequencies require some form of separation pre-filtering.

Figures 1 and 2 describe, basically and in detail, the circuitry requirements to separate the 12kHz and 18kHz signals and to provide them to the processing medium.

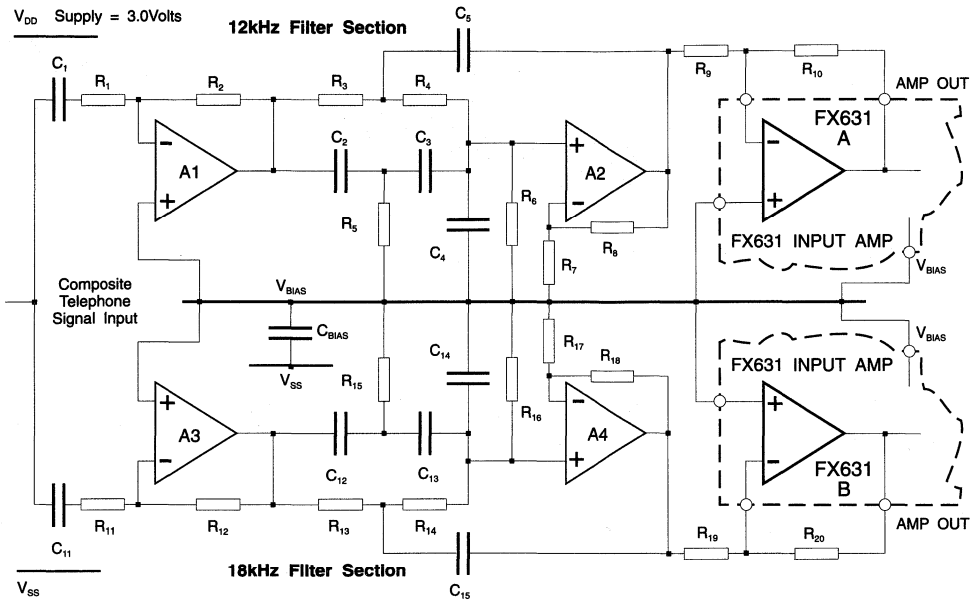
Amplifiers A1, A2, A3 and A4 are formed using a TLC274 quad Op-Amp; A1 and A3 form attenuators to set the devices to the required sensitivity.

12kHz Filter section

Amplifier A2, with components, (Figure 2) forms a 12kHz/18kHz pole/zero pair feeding FX631A whose input stage is set to unity gain. FX631A is set to operate to a 12kHz SPM system with the Xtal/clock input at 3.579545MHz. This configuration separates the 12kHz SPM signal.

18kHz Filter Section

Amplifier A4, with components, forms an 18kHz/12kHz pole/zero pair feeding FX631B whose input stage is set to unity gain. FX631B is set to operate to a 16kHz SPM system and upgraded to operate to 18kHz by increasing the Xtal/clock input to 4.032MHz. This configuration separates the 18kHz security frequencies.



The 12kHz (top) section

Component	Value		
A1	TLC274 -1	R_8	13.0kΩ
A2	TLC274 -2	R_9	100kΩ
R_1	1.0MΩ	R_{10}	100kΩ
R_2	56.0kΩ	C_1	27.0pF
R_3	24.0kΩ	C_2	270pF
R_4	47.0kΩ	C_3	120pF
R_5	36.0kΩ	C_4	180pF
R_6	160kΩ	C_5	820pF
R_7	10.0kΩ	FX631 X_1	3.579545MHz

Tolerances: all components ±1.0%

The 18kHz (bottom) section

Component	Value		
A3	TLC274 -3	R_{18}	43.0kΩ
A4	TLC274 -4	R_{19}	100kΩ
R_{11}	1.0MΩ	R_{20}	100kΩ
R_{12}	56.0kΩ	C_{11}	27.0pF
R_{13}	24.0kΩ	C_{12}	820pF
R_{14}	47.0kΩ	C_{13}	390pF
R_{15}	6.8kΩ	C_{14}	120pF
R_{16}	30.0kΩ	C_{15}	560pF
R_{17}	10.0kΩ	FX631 X_1	4.032MHz

Tolerances: Resistors ±1.0%
Capacitors C_{11}= ±10%, C_{12} to C_{15}= ±5%

FX631 external components should be selected in accordance with the Data Sheet instructions; R_9/R_{10} and R_{19}/R_{20} (Figure 2 above) are the FX631 input components. The V_{BIAS} lines of both FX631 devices may be connected to the circuit bias line and then decoupled to V_{SS} (capacitor C_{BIAS}).

Fig.2 Recommended Circuitry

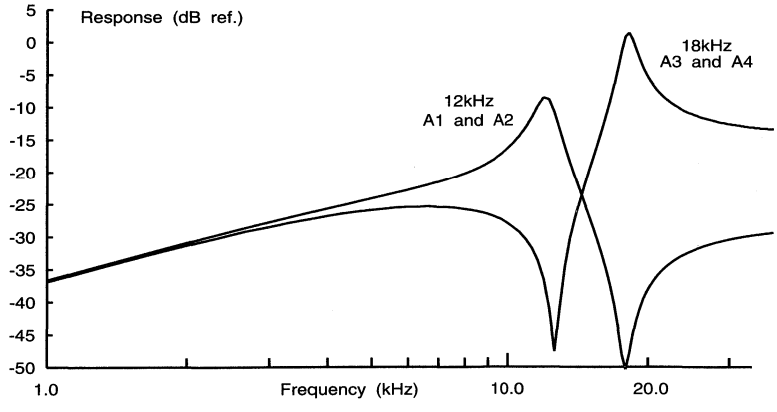


Fig.3 Responses of the External Filter Stages

Telephone Fraud Prevention using *'Echo-Back'*

Many telephone companies are voicing concern over the increase in payphone fraud and the corresponding loss of revenue. It is possible for unauthorised telephones to "connect-in" to a payphone or private subscriber line to obtain free and illegal use of the system.

The *'Echo-Back'* method, using the FX631 Subscriber Private Metering (SPM) Detector, is suggested by CML as being: simple to implement, of low-cost and secure in operation.

This method is described below.

The addition of a 12kHz or 16kHz pulse generator to the remote 'phone, and an FX631 SPM Detector to the exchange, will prevent this type of fraud by arranging that the remote installation 'reports back' to the exchange in a predetermined way using 12kHz or 16kHz *'Echo-Back'* signalling.

In a standard metering installation, under normal conditions, the exchange sends the relevant (12kHz or 16kHz) metering (SPM) pulses to the remote 'phone for call-charge monitoring purposes.

With the *'Echo-Back'* system (see Figure 1) the 'remote' 'phone is configured to transmit a 12kHz or 16kHz signal (back) to the exchange in a coded fashion. This signal is decoded by an additional card in the exchange; any unit that does not respond with the authentic reply will be barred by the exchange system terminating the call.

The FX631 SPM Detector is low-power microcircuit, which may be line-powered, requiring less than 1.0mA at 3.0V.

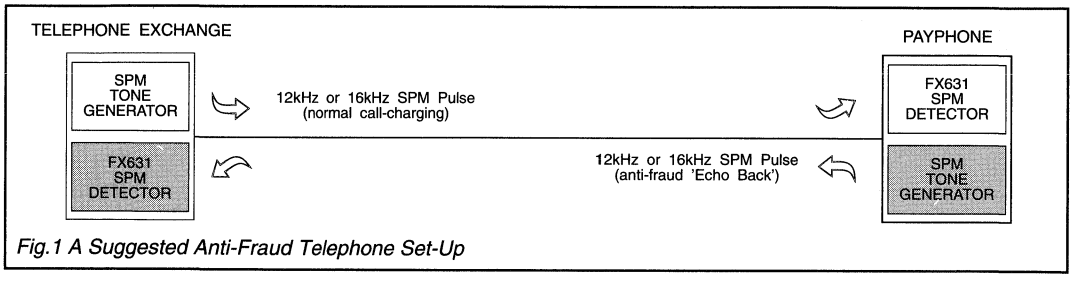


Fig.1 A Suggested Anti-Fraud Telephone Set-Up

Subscriber Pulse Metering in PCMCIA, Data and Fax Modems

Telelephone Line Activity

All Fax machines, PC and laptop Fax and data cards have a facility to report the "duration" of a Fax transmission in seconds and minutes.
The system relies on simple timing but gives no information as to the **actual cost** of each data transmission.

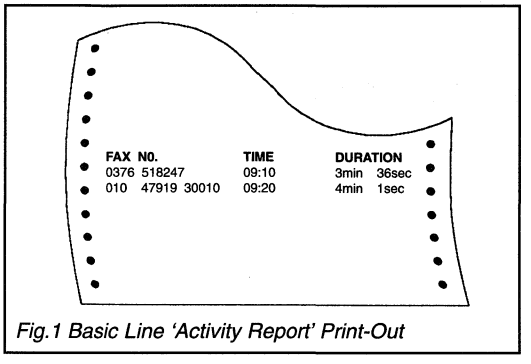


Fig.1 Basic Line 'Activity Report' Print-Out

A Call-Charge Report

By including an SPM detector (FX631) in the relevant equipment, a report can now be generated which actually reports the **real cost** of the 'call' in local currency.

This allows the machine to cost the differences between local and international calls and the use of peak- and cheap-rate dialling periods.

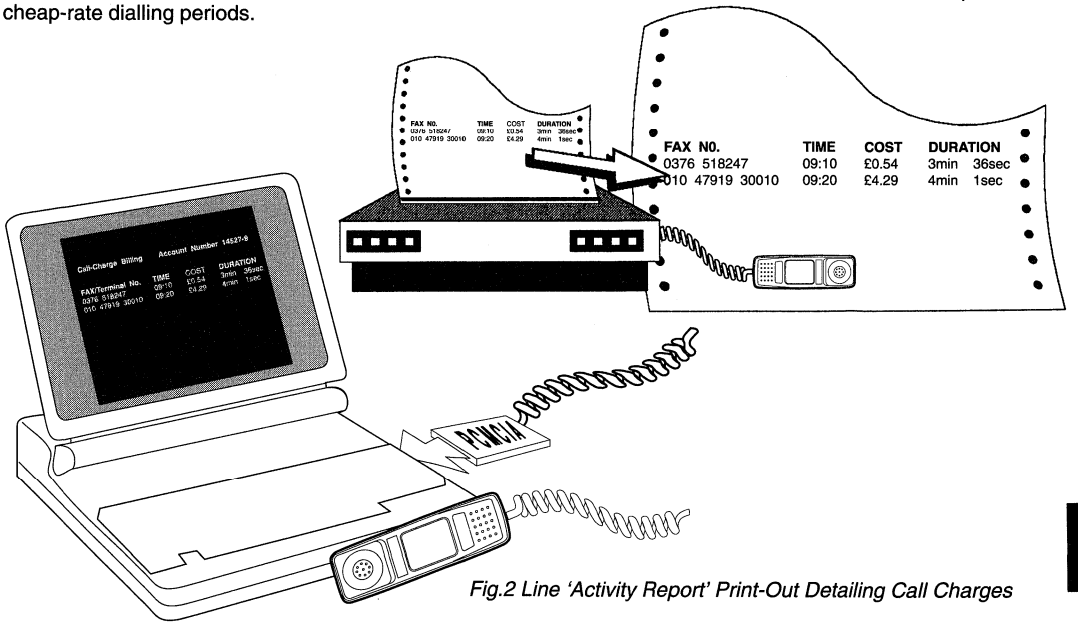


Fig.2 Line 'Activity Report' Print-Out Detailing Call Charges

The Principals of Data and Fax Call-Charging

The FX631 SPM Detector monitors and detects 12kHz or 16kHz (SPM) call-charge pulses placed on the telephone line by the local telephone exchange. Each SPM pulse represents "one unit" of charge.

The number of pulses sent per second determines how expensive a particular telephone or Fax call is! In this respect, long-distance calls would have more pulses per second than a local call.

By using the detected output of the FX631 the host PC, Laptop or PDA can convert this received SPM information into actual cost. The conversion is achieved by multiplying the number of received SPM pulses for a given data transmission by the country's relevant "unit charge" [cost per pulse]. This unit-charge is a fixed rate in each country.

Transmission Cost = Number of received SPM pulses x Relevant unit charge for the country concerned

The "unit charge" would be programmed locally at installation of the modem or, multiple countries' charge rates would be held in memory. Increases in call charges could be taken care of automatically by the local telecomms authority increasing the ***rate*** of SPM pulses and ***not*** their unit value

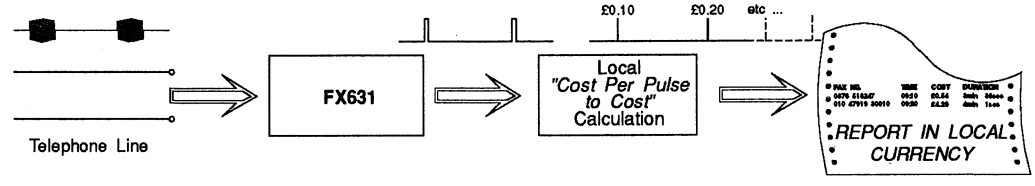


Fig.3 SPM/Call-Charge Flow Diagram

FX009 and FX019 Digitally Controlled Amplifier Arrays

The FX009 and FX019 offer 8 and 4 digitally controlled gain/attenuation amplifiers, respectively.

FX009	FX019	
7 Amplifiers	3 Amplifiers	+3dB to -3dB adjustment range in 0.43dB steps
1 Amplifier	1 Amplifier	+15dB to -15dB adjustment range in 2dB steps

In certain applications it may be necessary to trim over a wider dynamic range or use smaller step sizes. This can be achieved by grouping the amplifier stages together either in series or parallel.

The 2 following examples show typical application of:

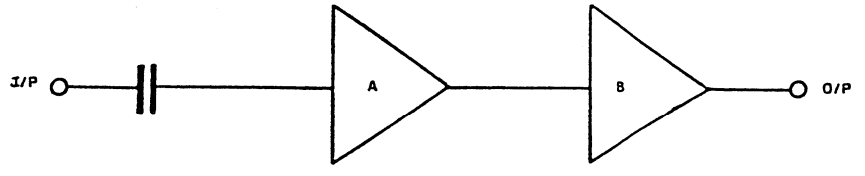
1. Series connection of 2 amplifiers to achieve trimming over a 30dB dynamic range in 0.43dB steps.

2. Parallel connection of 2 amplifiers to achieve approximately 0.21dB steps over a 6dB dynamic range.

Example 1

0.43dB steps over a 30dB dynamic range

This is achieved by connecting the volume amplifier stage in series with 1 of the other amplifier stages as shown in the diagram below.

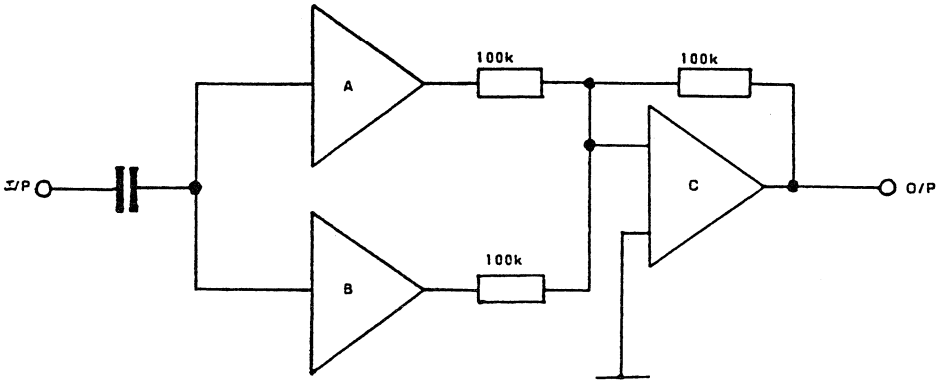


A - FX009 AMPLIFIER NO. 8 (FX019 AMPLIFIER NO. 4) (VOLUME)
B - ANY OF THE FX009 AMPLIFIERS 1 THROUGH 7 (FX019 AMPLIFIERS 1 THROUGH 3)

Example 2

0.21dB steps over a 6dB dynamic range

A very fine step size of approximately 0.21dB can be obtained over a 6dB dynamic range by the connection of 2 amplifiers in parallel.



A & B - ANY FX009 AMPLIFIERS 1 THROUGH 7 (FX019 AMPLIFIERS 1 THROUGH 3)
C - STANDARD CMOS AMPLIFIER

The table shows all the possible combinations of gain on each of the 2 amplifiers, many of which are duplicated. The highlighted section shows 1 of the possible combinations to achieve an output dynamic of 6dB with approximately 0.21dB steps.

Amplifier B setting

	3.00	2.57	2.14	1.71	1.29	0.66	0.43	0.00	-0.43	-0.86	-1.29	-1.71	-2.14	2.57	-3.00
3.00	3.00	2.79	2.58	2.38	2.19	1.99	1.81	1.83	1.45	1.28	1.12	0.96	0.80	0.65	0.51
2.57	2.79	2.57	2.36	2.15	1.95	1.76	1.57	1.38	1.20	1.03	0.86	0.69	0.53	0.38	0.22
2.14	2.58	2.36	2.14	1.93	1.72	1.52	1.33	1.14	0.95	0.77	0.60	0.43	0.26	0.10	-0.05
1.71	2.38	2.15	1.93	1.71	1.50	1.30	1.10	0.90	0.71	0.52	0.34	0.17	.00	-0.17	-0.33
1.29	2.19	1.95	1.72	1.50	1.29	1.07	0.87	0.67	0.47	0.28	0.09	-0.09	-0.26	-0.43	-0.60
0.88	1.99	1.76	1.52	1.30	1.07	0.86	0.65	0.44	0.24	0.04	-0.15	-0.33	-0.51	-0.69	-0.86
0.43	1.81	1.57	1.33	1.10	0.87	0.65	0.43	0.22	0.01	-0.19	-0.39	-0.58	-0.76	-0.94	-1.12
0.00	1.83	1.38	1.14	0.90	0.67	0.44	0.22	0.00	-0.21	-0.42	-0.62	-0.81	-1.01	-1.19	-1.37
-0.43	1.45	1.20	0.95	0.71	0.47	0.24	0.01	-0.21	-0.43	-0.64	-0.85	-1.05	-1.24	-1.43	-1.62
-0.86	1.28	1.03	0.77	0.52	0.28	0.04	-0.19	-0.42	-0.84	-0.86	-1.07	-1.28	-1.48	-1.67	-1.86
-1.29	1.12	0.86	0.60	0.34	0.09	-0.15	-0.39	-0.62	-0.85	-1.07	-1.29	-1.50	-1.70	-1.90	-2.10
-1.71	0.96	0.69	0.43	0.17	-0.09	-0.33	-0.58	-0.81	-1.05	-1.28	-1.50	-1.71	-1.93	-2.13	-2.33
-2.14	0.80	0.53	0.26	.00	-0.26	-0.51	-0.76	-1.01	-1.24	-1.48	-1.70	-1.93	-2.14	-2.35	-2.56
-2.57	0.65	0.38	0.10	-0.17	-0.43	-0.69	-0.94	-1.19	-1.43	-1.67	-1.90	-2.13	-2.35	-2.57	-2.78
-3.00	0.51	0.22	-0.05	-0.33	-0.60	-0.86	-1.12	-1.37	-1.62	-1.88	-2.10	-2.33	-2.56	-2.78	-3.00

Getting the Best Performance from Wireless Data Modems

CML Wireless Data Modems

Consumer Microcircuit's complete product line of wireless data modem ICs offers full product migration from speeds of 1,200b/s to 40,000b/s.

The first modem (the FX409) appeared in 1984. An updated version of which, the FX439, now addresses the same bit-serial Fast Frequency Shift Keying (FFSK) market. Uses of MSK or FFSK are varied: from the automatic location of vehicles to the transmission of data by orbiting satellite. Radio data gives fast accurate information transfer with instantaneous responses. Complex and expensive wire-line networks are liberated by the freedom of radio data.

Byte-wide, protocol-specific devices serve trunked mobile systems worldwide (UK MPT1327 -FX429 and in France PAA1382 -FX529). These are excellent, field proven protocols useful for wide range of radio system data applications.

A selective calling protocol is supported by FFSK-1200 and has been approved by the European Telecommunications Standards Institiute (ETSI).

The FX809 combines many of the best features of the serial and byte-wide devices. Receive and Transmit data is exchanged in byte-length serial bursts allowing both free-format and protocol specific operation.

The control and data interface of the FX809 is provided using C-BUS (CML's proprietry standard for the transmission of commands and data between a µController and DBS800 PMR and Cellular radio microcircuits), and addressable registers.

All CML's 1,200b/s modems use 1200/1800 mark and space frequencies: One cycle of 1200Hz represents a logic '0'. Each bit-period is a constant 1/1200 of a second. One-to-zero bit transitions occur at the sinewaves' zero crossing points. This gives a phase coherent frequency-shift which gives rise to FFSK or MSK. The occupied bit-rate-bandwidth is 900 to 2,100 Hz.

Our most recent product releases are: the FX469, a 1200/2400/4800b/s FFSK device and the FX589 a GMSK modem which will operate from 4,000b/s to 40,000b/s .

Device	Description	Two-Way Radio	Cellular Radio	Wireless Data Modems
FX429/529	1,200b/s FFSK Modem with Parallel BUS Control	●		●
FX439	1,200b/s FFSK Modem with Serial Control	●	●	●
FX469	1,200/2,400/4800b/s FFSK Modem with Serial Control	●	●	●
FX589	40kb/s GMSK Modem with Serial Control	●		●
FX809	1200b/s FFSK Modem with "C-BUS" Control	●		●

Table 1 CML Modem Microcircuits

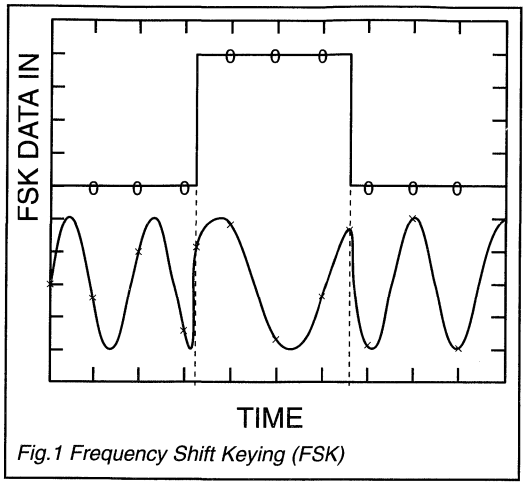


Fig.1 Frequency Shift Keying (FSK)

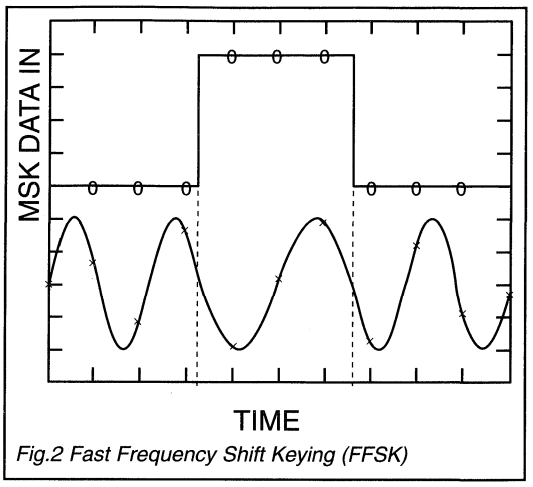


Fig.2 Fast Frequency Shift Keying (FFSK)

Principles of FSK/GMSK

Frequency Shift Keying (FSK) functions by assigning one carrier frequency (f1) to the '0' binary state and a second carrier frequency (f2) to the '1' binary state. Abrupt changes in carrier phase can occur as transitions take place between the two frequency states, as shown in Figure 1.

Defining the modulation index, m, as

$$m = \Delta f \times T$$

where, $\Delta f = f2 - f1$

T = binary state duration (inverse of bit rate, 1/bps)

$$m = \frac{f\Delta}{R}$$

R = Binary Signalling rate

CPFSK is defined as continuous phase FSK. Fast Frequency Shift Keying is defined as a special case of CPSFK where m = 0.5, and results in a minimum difference in signalling frequencies equal to the bit-rate divided by 2. Continuous phase in FFSK is also maintained by constraining the frequency changes to the carrier zero crossing, as shown in Figure 2. The carrier can be directly keyed RF carrier and or an audio sub-carrier. In the case of CML's FFSK modems an audio sub-carrier is used.

An alternative method of data modulation which can be used in radio modems is direct modulation of the RF carrier rather than the use of an audio sub-carrier. The definition of FFSK/MSK given above can be applied to direct Radio Frequency modulation or audio sub-carrier modulation.

Although phase continuity has been achieved there remains a frequency discontinuity at each symbol transition, and to remove this requires pre-shaping of the baseband bit stream with an appropriate filter. Use of a pre-modulation low pass filter with Gaussian characteristics in conjunction with MSK achieves this.

If an RF carrier of 100 MHz were used to signal at 20kb/s our definition of MSK would infer a frequency shift of 10kHz. If the data stream were applied to a suitable Gaussian filter this would give true GMSK. However in practical systems the data speed is much less than the RF carrier frequency. This leads to the result that if the RF carrier is modulated with a data stream which has been passed through a gaussian filter the resulting modulation has the same characteristics as GMSK. This is sometimes called Modified GMSK as in the Mobitex systems specification but is also widely referred to as just GMSK.

CPFSK modulation has been adopted for the Bell 202 modem standard. FFSK was selected for RF data communication for low signal-to-noise environment or situations that require less bandwidth than the FSK approach. GMSK has been adopted as the modulation standard for the European Digital Cellular network GSM, Mobitex/RAM at 8kb/s, Cellular Digital Packet Data at 19.2kb/s and Digital Short Range Radio (DSRR).

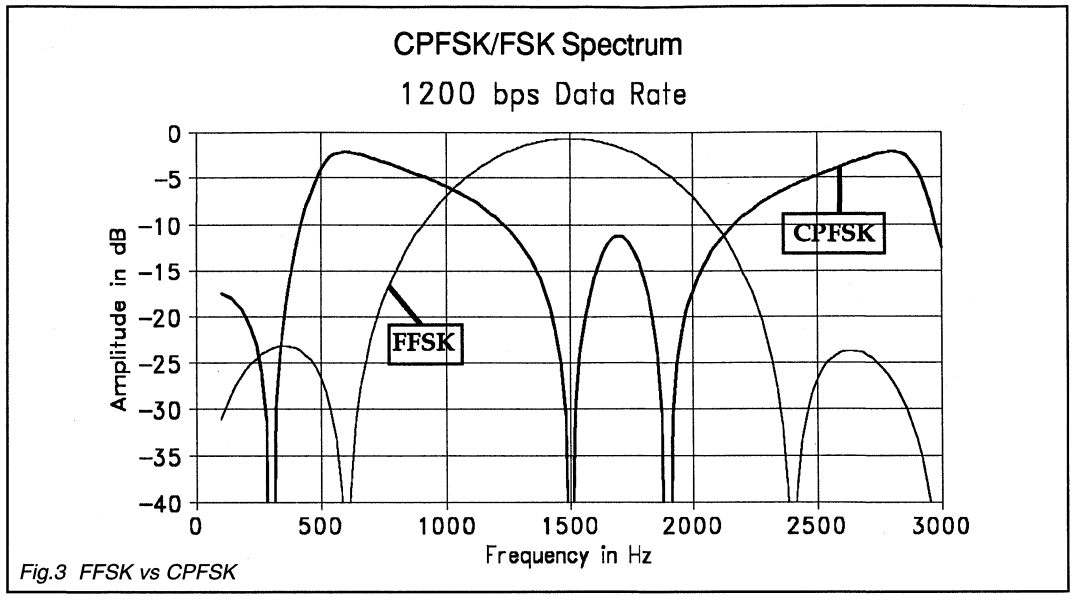


Fig.3 FFSK vs CPFSK

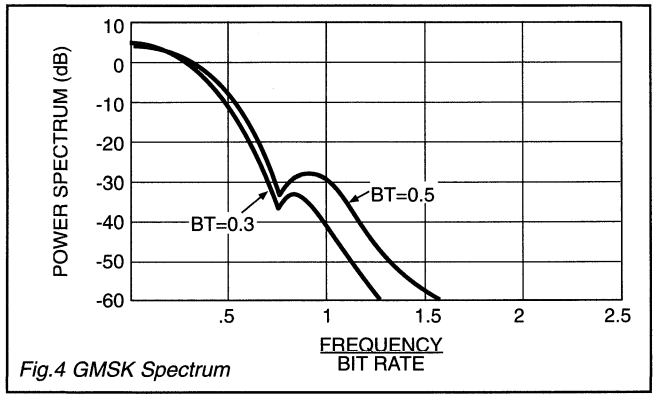


Fig.4 GMSK Spectrum

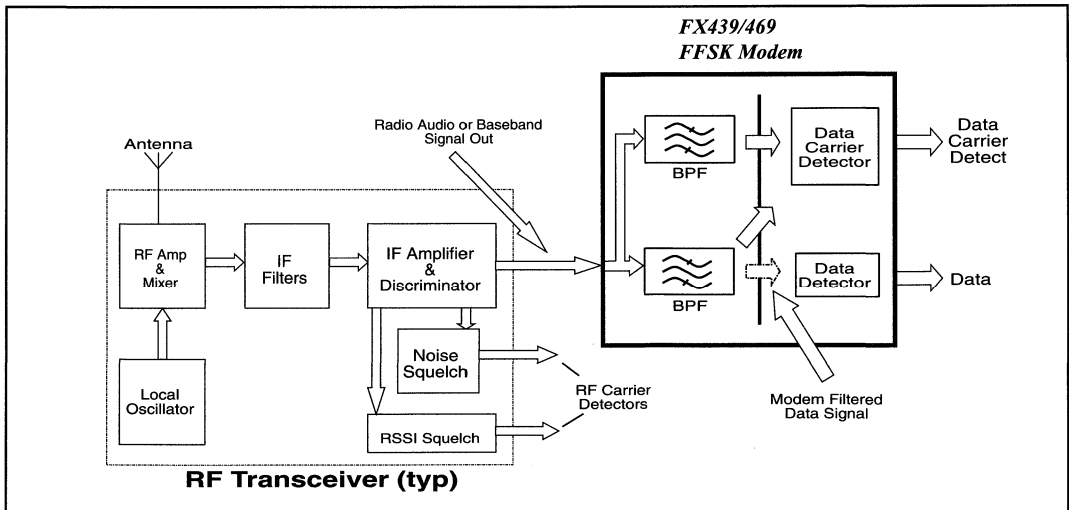


Fig.5 FFSK Modem Together With a Typical FM Receiver

The Effect of Modem Bandwidth on Bit Error Rate (BER)

The basic measure for rating one modem against another is its BER performance. BER is the ratio of error bits to the total transmitted bits for a given level of signal-to-noise (SNR). BER performance is dependent on the noise bandwidth at the modem's internal data detector circuit. The narrower the modem's bandwidth, the better BER for same SNR at the modem's inputs. An FFSK modem has a 1200Hz noise bandwidth where a Bell 202 type has approximately 2500Hz. The improved performance using a typical FM receiver is shown in Figure 5, with the FFSK modem outperforming the Bell 202 by several dB.

In a given radio link, BER performance varies with signal-to-noise, and fringe area service decreases SNR. Noise increases errors (see Figure 6). FFSK-1200 performs several dB better than voice, on the premise that voice follows. In trunking and Selcall systems, the data is used to set up a voice link, so there is no point in grossly over-reaching the radio's voice range. A SINAD of 12 dB is the accepted limit of voice intelligibility, and 8 to 10 dB SINAD is the goal of FFSK-1200 service.

Poor performance under good signal conditions points to elements in the detection process that are not correctly aligned. Modems made from discrete components typically need periodic re-alignment. Data carriers drift or the PLL goes off centre.

IC Modems lock onto quartz crystals, use digital frequency dividers and switched capacitor filters that don't drift, and don't need alignment because there's nothing to align.

Once the modem is in your radio system, you will test it. Modem testing is optimized for test time (cost) and statistical significance of the test results. For example, the FX439 1200 bps modem, rated at 10-3 BER at -117 dBm RF signal level, will require 12000 bits to detect up to 12 errors and will take 10 seconds to test. That is a reasonable amount of test time. However, if this modem is tested for BER of 10-4 at another RF signal level, this will require 120,000 bits for the same statistical test significance and the test time will zoom to over 100 seconds!

What happens to BER as RF levels are varied? Comparative testing performed with an FX439 and a typical Bell 202 IC modem installed in a typical UHF receiver appear in Figure 6. With a signal of -117dBm (0.3mV) the FX439 delivers a BER of about 1 x 10^{-4} compared to the Bell 202 units about 1 x 10^{-3}. FFSKs inherent narrower bandwidth allows filtering to remove more noise than the Bell FSK modem. This results in fewer bit errors.

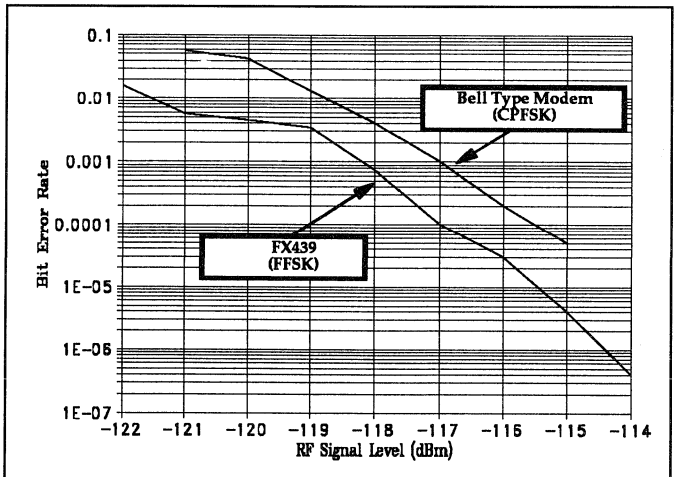


Fig.6 Bit Error Performance

Synchronous vs Asynchronous Data

Data transmission systems are designed to operate with either synchronous or asynchronous serial data formats. In a synchronous system, each bit is clocked in synchronism with the system master clock. The synchronizing signal may be embedded in the data signal or provided on a separate clock line. In addition, synchronous transmission requires the use of frame sync preamble to allow the receiver to determine the beginning and end of blocks of data.

This is achieved in FFSK synchronous modems by encoding a preamble of 1-0-1-0 transitions (16 bits by convention), allowing receiving stations time to lock onto the edges of the received data. This is done in CML modems with a digital PLL that controls a frequency divider incremented in 1/28th bit steps. A misaligned worst-case signal may take as many as 14 bit times to lock. Lacking edges on which to lock, the DPLL free runs at 1200 bps.

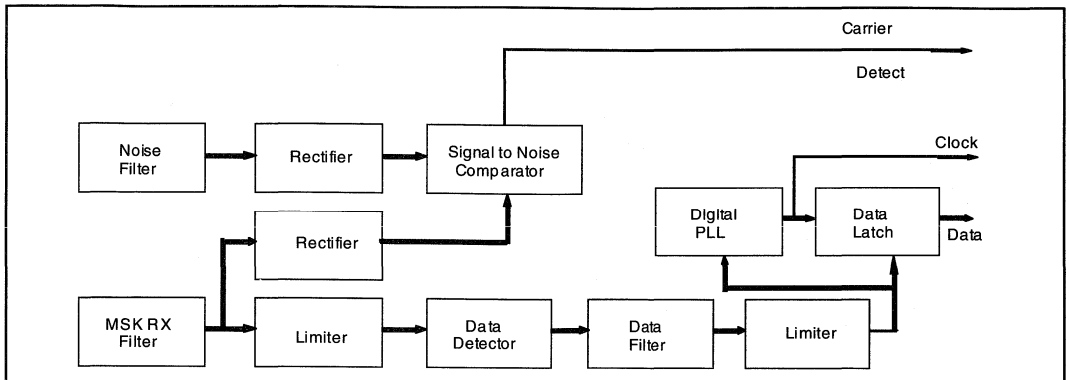


Fig.7 FSK Receiver Block Diagram

In asynchronous systems, each character (or word) consists of a "start bit" that starts the receiver clock and concludes with a "stop bit" that terminates the clocking. Typically, slower wireline modems use asynchronous modulation while fast ones are synchronous. All benefit from a great deal of handshaking, and smart ones default to slower speeds when the going gets tough.

FM Mobile radio is characterized by noise and fading, over a few short hops. Wirelines have noise, but little fading and fewer hops. These introduce group delay and isochronous distortion or jitter -- a source of difficulty for synchronization and high Bit Error Rates (BER).

Forward Error Correction (FEC) functions best with synchronous data streams. If any single bit is corrupted, all other bits stay in position and FEC can act to correct the bit error. In asynchronous data streams, any "start" corrupted bit will result in offsetting all subsequent data bits, rendering the FEC useless.

Detecting Data Carriers Wireline vs Wireless

Data carrier detection methods vary depending on the transmission media characteristics. Wireline modem data carrier detectors look for broadband energy. Detectors can differentiate between white noise and signal. But wireless data carrier detection, as in the FX439, looks for a level differential between the energy in the data passband and the energy at the FFSK first null point (2400HZ). That's because the output of unsquelched RF discriminator is characterized by high levels of broadband white noise which wireline broadband detectors will not be able to differentiate from signal. The circuitry in the FX439 is a pair of envelope detectors looking for a signature characteristic of FFSK data.

One of the application problems of any carrier detection technique is trading off response time for false alarms. The value of the detector integration capacitor shown on the data sheet is 0.1uF.

Naturally, it plays an important role in determining detector response time, but also affects the false alarm rate. Increasing the capacitor value, decreases the false alarm rate but increases the time to detect the carrier. The level of the noise which drives the detectors also controls the false alarm rate. Care must be taken not to saturate the filters in the FX439 or provide too low of a level. In the particular receiver used for our tests, RMS levels of unsquelched noise were twice that of data (data @ 3kHz deviation). The result of substituting other values of integration capacitors is shown in Figure 8.

The FX439's data carrier detect threshold is approximately 125 mVrms. For best operation noise should be kept in the 250 to 400 mVrms range. Some RF receivers may require a pad or attenuator to provide this optimum detection level. Another option might be to adjust the Q of the radio receiver's quadrature detector coil to establish the desired recovered audio level that way.

A by-product of increasing the size of the capacitor on the carrier detector pin is chatter or multiple edges in the carrier detector output. As the detected data signal appears at the carrier detect time constant pin, there is a much slower rise time due to the increased size of the time constant capacitor. As this signal has some of the detected audio components present, it causes multiple edges on the leading edge of the carrier detect output as the signal passes through the threshold point of the comparator.

Modems working in concert with microprocessors may be able to overcome this with software by multiple samples over time of the carrier detect signal. An alternative is to add an inverter to the output of the carrier detector and apply positive feedback at the carrier detector time constant pin to accomplish a Schmidt trigger effect. This is shown in Figure 9. Capacitive feedback was selected instead of resistive feedback because capacitor feedback is easier to control in this application.

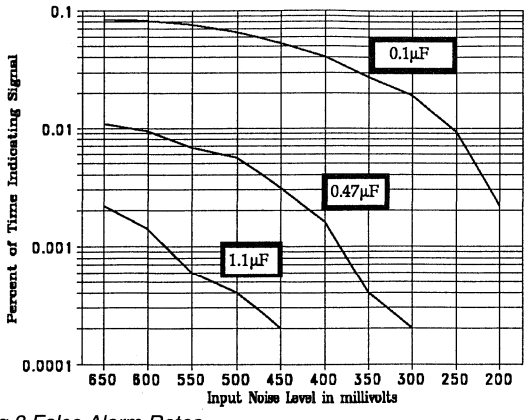


Fig.8 False Alarm Rates

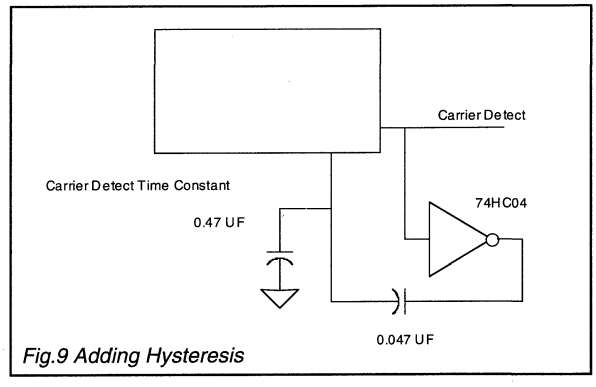


Fig.9 Adding Hysteresis

Using an FFSK/MSK Synchronous Modem with an Asynchronous Data I/O

This application note, used with current FX439/FX469 product information, outlines the construction of a low-cost asynchronous modem for transmission of RS-232 data in the from of FFSK/MSK, between terminals by a radio or line medium.

The modem circuitry shown in Figure 1 accepts asynchronous data while transmitting synchronous data using the FX439/FX469 series modem. The FX469 may be used to transmit data at either 1200 or 2400 bps, depending on the setting of switch 1 shown in Figure 1. The FX439 always transmits data at 1200 bps. Switch 1 must be set in position A to use the FX439. The chart below details the devices used in this application.

Performance Requirement	***Associated Circuitry***
RS-232 Driver/Receiver Level Translator	*Maxim MAX-232*
Async to Sync,	*Exar XR-2135*
Sync to Async Conversion	
Data Carrier Detection	*CML FX439/469*
Controlled RTS/CTS Delay	*74HC04 Delay Element*
Generation of MSK Signals	*CML FX439/469*

The signals required for an RS-232 handshake for asynchronous data are as follows. A complete definition of each is given at the end of this application note.

DTR	Data Terminal Ready
DSR	Data Set Ready
RTS	Request to Send
CTS	Clear to Send
TXD	Transmit Data
RXD	Receive Data

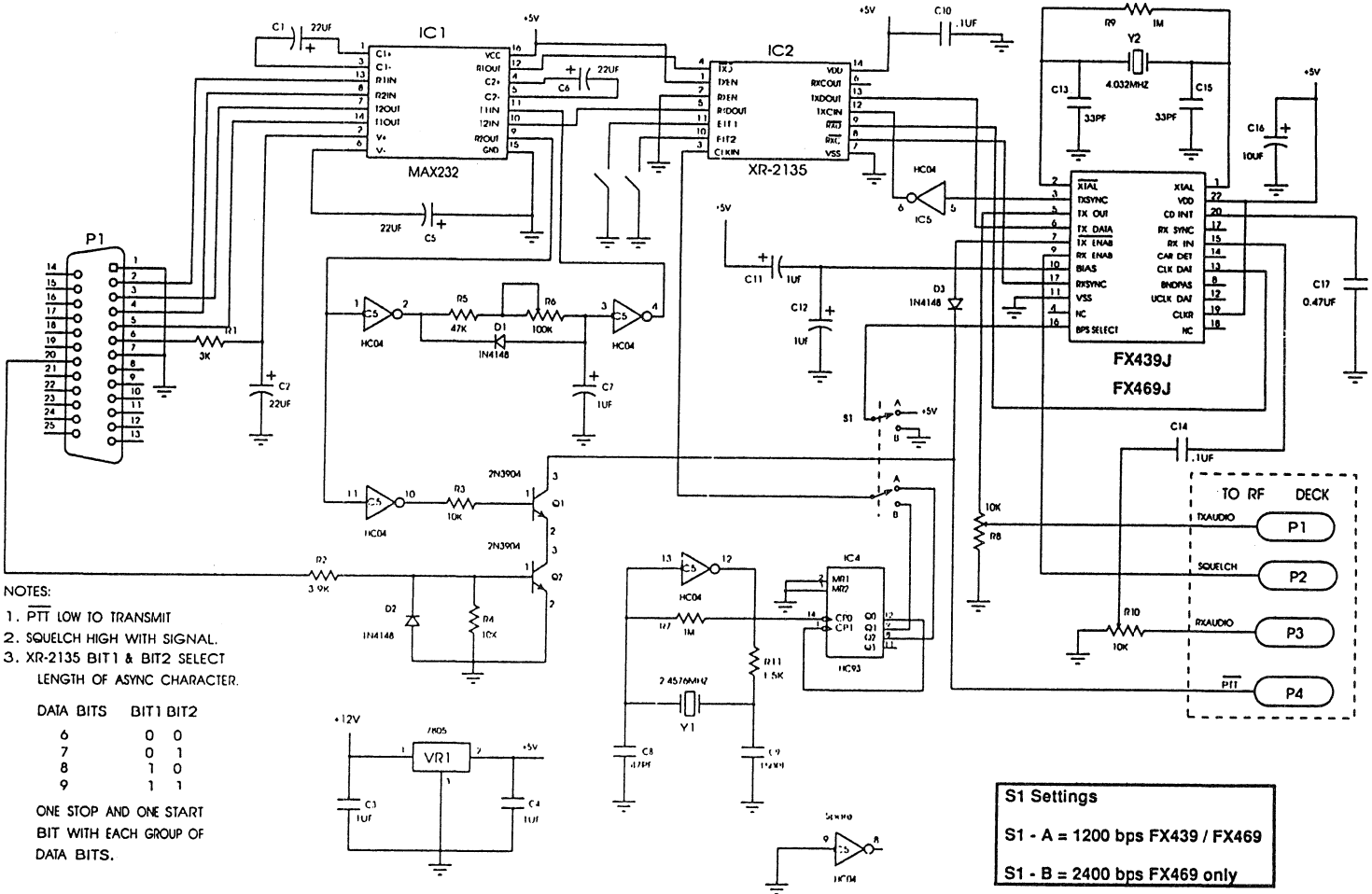
The Maxim MAX-232 converts the TTL/COMS input/output levels to $\pm$ 10V RS-232 input/output levels. On power-up, the data set ready (DSR) signal is set by the MAX-232's DC to DC converter. The incoming data terminal ready (DTR) signal enables the transmitter keying signal.

The request to send (RTS) and clear to send (CTS) signals are level shifted from the RS-232 interface to TTL/CMOS signal levels. When the modem receives an RTS, the RF transmitter and he MSK tone are keyed immediately and a 30 ms to 100 ms timer started. At the completion of the timing, a CTS signal is generated for the data terminal to allow serial data flow.

The transmit data (TXD) signal is level shifted to the TTL/CMOS levels, and applied to the Exar 2135 sync to async converter circuit.
The random timed asynchronous input from the data terminal is synchronised with the transmit clock pulses of the FX439/FX469.

If a timing error builds up due to the difference of the external asynchronous clock and the synchronous internal timing on the modem, the XR-2135 will skip a stop pulse to allow an adjustment to occur. The receiving end XR-2135 will generate a stop pulse and add it into the data flow so that no information is lost.

From the sync to async converter, synchronous information is then sent into the FX439/469, which converts the digital '1' into one cycle of 1200 Hz sinewave and a digital '0' into one and a half cycles of 1800 Hz sinewave for 1200 bps and 1200 and 2400 Hz for 2400 bps. This sinewave is then sent on the transmitter through a level adjustment. The signal is sufficiently band limited and level controlled to pass FCC type acceptance testing without any additional in-band filtering.



NOTES:

1. $\overline{\text{PTT}}$ LOW TO TRANSMIT
2. SQUELCH HIGH WITH SIGNAL.
3. XR-2135 BIT1 & BIT2 SELECT LENGTH OF ASYNC CHARACTER.

DATA BITS	BIT1	BIT2
6	0	0
7	0	1
8	1	0
9	1	1

ONE STOP AND ONE START BIT WITH EACH GROUP OF DATA BITS.

The incoming receiver signal is fed into the FX439/469 which is held in a power down mode until RF carrier is detected by the receiver squelch circuitry. This minimises power drain and also prohibits false information from being sent to the data terminal. If the receiver does not have a noise squelch signal, the chip's carrier detect must be used. It will detect within 12 ms the presence of the data modulation tone. This event is output on the carrier detect pin which should be used to disable the data output to minimise the 'clatter' at the beginning of the detection signal.

The tones are translated into logic levels and a digital phase lock loop is locked onto the incoming data steam within 16 bit reversals. The detected synchronous data and the recovered receive clock are sent into the XR-2135 for conversion back into asynchronous data . This information is then sent out to the data terminal through the Maxim MAX-232.

Operation in either a synchronous or asynchronous mode is achieved with a jumper. If additional RS-232 level shifting is needed for transmit and receive clocks and Tx and Rx enable, pins on the XR-2135 are brought low. Bringing these pins low bypasses the conversion process and allows synchronous data to pass directly through the device.

Proper clock frequency for the FX439 device is provided by a 4.032 MHz crystal. Clock frequency for the XR-2135 must be provided at 256 times the bit rate. This is accomplished by using a 2.4576 MHz crystal and dividing down by eight to 301.2 kHz (1200 bps) or by any four to 602.4 kHz (2400 bps). Power is derived from a single 7805 voltage regulator. DC current measured on the first model is 12.745 mA.

Software Considerations

As with many data systems, there are certain items that should be addressed within software for proper operation. These items are:

Bit Sync Pattern

Bit Sync Time

Noise Bits at End of Transmission

Since the FFSK/MSK modem is a synchronous device, a pattern must be transmitted at the beginning of each RF burst to allow the DPLL sufficient time and data transitions (a change from a one to zero or a change from a zero to a one) to synchronise. The device requires a least sixteen of these transitions for sync to occur. This may be accomplished by appending two bytes of $55 or $AA onto the message. Once this is accomplished, adding a beginning of text character and an end of text character would ensure a correct decode at the receiving end. This is especially true at the end of the transmission. Once the RF signal ends, high level noise will be emitted from the receiver. Even if the data carrier detect or the noise squelch signals are used to gate the data off, there will be a period of noise while these circuits are making their decision. It is random data which many times will cause a programmable logic controller or point of sales terminal to lock up. Having the message bracketed and only dealing with information between the start and stop characters is one method of prohibiting random data from entering the actual message.

Operation with CTCSS or DCS Sub-Carriers

Because the FX439/469 modems contain a bandpass filter on the input, CTCSS/DCS sub-carriers are filtered out without extra circuitry.

It is important that no energy from the tone section appears within the transmitted data signal passband of 900 Hz to 2100 Hz for 1200 bps or 600 to 3000 Hz for 2400 bps. It is equally important that the tone and data signals are not summed together and sent into the limiter section of the transmitter. The limiter represents a non linearity and would generate intermodulation products within data bandpass which when received generate errors in the decoding of the data. Tone is normally summed into an FM transmitter after the limiting.

Radios designed only for data do not require a speech limiter, allowing tone and data to be summed directly.

RS-232 Handshake

The RS-232 handshake for asynchronous data requires the following signals:

Data Terminal Ready is a signal from the terminal or computer that indicates to the modem that the unit is powered and active. An RF transmission should not be enabled if the Data Terminal is not active.

Data Set Ready is a signal from the modem that indicates to the terminal that the unit is powered and active. Many terminals or computers will not allow data to flow without this condition being true.

Request to Send emanates from the terminal or computer. The software or user has decided that transmission should begin and requests that the RF carrier be turned on.

Clear to Send is a signal that originates from the modem. It is sent in response to a RTS, the request to send signal from the terminal or computer after certain criteria have been met. It is not sent until sufficient time has expired after the transmitter keyed to allow adequate settling time for both the RF transmitter and receiver. It would not be sent if there is an RF carrier on the channel indicating another user. Finally, it would not be sent if a high VSWR were detected on the transmitter when it was keyed. (Not all transmitters are provided with a VSWR detector).

Transmit Data and Receive Data is the actual asynchronous data flow. Transmit data is data coming from the terminal and Receive data is data flowing into the terminal.

Another term often heard is DTE and DCE ends of RS-232 connectors would be. Most often a computer would be programmed to be a DTE or data terminal end of the information flow. When one computer wishes to talk to another computer, it's like two people transmitting on their radios at the same time. Nobody hears the other! If one were to use 'null' modem cable, the wires are interchanged such that one of the data terminals is now wired like a data communication device. The same is true of two modem devices. A modem device is a DCE (data communication device) which cannot be plugged into another DCE. However, if a few additional signals are available, one DCE could be used to daisy chain into another DCE as shown in Figure 2. As can be seen the data carrier detect lines are used to key the companion modem unit. The originating end must be programmed with sufficient delay to allow the RTS/CTS delay of the modems to occur prior to the beginning of any information transfer.

Error Detection and Correction of MPT1327 Formatted Messages

using CML devices

1. Background

MPT1327 messages are transmitted as 64-bit 'codewords', where each codeword contains 48 information bits followed by 16 check bits:

1	48	49	64
Information Field		Check Bits	

(Bit number 1 is transmitted first.)

These check bits allow the receive terminal to *detect* all odd numbers of errors, any 2 or 4 errors, and any error-burst up to length 16 in a codeword, and also to *correct* errors in the received codeword, although it should be noted that the higher the degree of error correction applied, the more likely is false decoding.

This document gives algorithms for ;

Generation of the check bits of a transmitted codeword.
Received codeword *error detection.*
Limited *error correction* of a received codeword.

These algorithms may be used with any bit or byte oriented modem, such as the **FX419**, **FX429**, **FX439** or **FX809**, although the **FX429** and **FX809** devices can perform *check bit generation* and *error detection* automatically and the **FX429** also provides a 16-bit 'Syndrome' output which may be used to aid *error correction.*

2. Generation of Transmit Codeword Check Bits

2.1 Theory:

The first 15 check bits are derived from a (63,48) cyclic code by using codeword bits 1 to 48 as the coefficients X^{62} to X^{15} (in that order) of a 63 bit polynomial, which is then divided modulo-2 by the generating polynomial;

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + X^0 \qquad (11101000\ 00010101 \text{ binary})$$

On completion of the division, the 15 coefficients X^{14} to X^0 of the remainder are used as the first 15 check bits (codeword bits 49 to 63), with the X^0 coefficient (bit 63 of the complete codeword) inverted.
Finally, bit 64 of the codeword is added to provide an even parity check of the whole 64-bit codeword.

2.2 Example of Transmit Codeword Generation

Information field; 6 data bytes:

```
      89       AB       CD       EF       12       34     Hex
10001001 10101011 11001101 11101111 00010010 00110100  Binary
```

Polynomial division

```
     x62 ..................................................................... x0
10001001 10101011 11001101 11101111 00010010 00110100 00000000 0000000
11101000 00010101
 1100001 10111110 1
 1110100 00001010 1
   10101 10110100 010
   11101 00000010 101
    1000 10110110 1110
    1110 10000001 0101
     110 00110111 10111
     111 01000000 10101
       1 01110111 0001010
       1 11010000 0010101
         10100111 00111111
         11101000 00010101
          1001111 00101010 1
          1110100 00001010 1
           111011 00100000 01
           111010 00000101 01
                1 00100101 0010111
                1 11010000 0010101
                  11110101 00000101
                  11101000 00010101
                     11101 00010000 000
                     11101 00000010 101
                           10010 10110010 001
                           11101 00000010 101
                            1111 10110000 1001
                            1110 10000001 0101
                               1 00110001 1100010
                               1 11010000 0010101
                                 11100001 11101110
                                 11101000 00010101
                                      1001 11111011 0000
                                      1110 10000001 0101
                                       111 01111010 01010
                                       111 01000000 10101
                                            111010 11111000 00
                                            111010 00000101 01
                                                   11111101 0100000
```

Remainder with last bit inverted;

```
                                                   11111101 0100001
```

Complete codeword, including parity bit;

```
Bit; 1                                                              64
     10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000010
        89       AB       CD       EF       12       34       FD       42
```

2.3 'C' Language Algorithm:

```
/*****************************************************************************/
/*    Function gen_ckbits() returns the first 15 check bits of a transmit  */
/*    codeword (codeword bits 49 to 63). Bit 15 of the returned value will */
/*    be codeword bit 49, bit 1 of the returned value will be codeword bit */
/*    63, and the lsb (bit 0) should be ignored.                           */
/*    The last bit (64) of the codeword must be derived separately, to     */
/*    give even parity of the whole 64-bit codeword.                       */

gen_ckbits()
    {
    int n,bit;
    unsigned int ckbits = 0;                    /* Clear check bits         */
    for(n=1;n <= 48;n++)                        /* 48 information bits......*/
        {                                       /*                          */
        bit = getbit_tx(n);                     /* Get each bit in turn ... */
        if( 1 & (bit ^ (ckbits >> 15)))         /*     XOR tx bit with MSB  */
                                                /*     of checkbits and if  */
                                                /*     the result == 1      */
            ckbits ^= 0x6815;                   /*     then XOR checkbits   */
                                                /*     with 6815 Hex        */
        ckbits <<= 1;                           /* ... Shift check bit word */
                                                /*        one bit left,     */
        }
    return(ckbits ^ 0x0002);                    /* Return checkbits with    */
                                                /* codeword bit 63 inverted */
    }

/*    Function getbit_tx(n) should return bit 'n' (1 to 48) of the transmit*/
/*    codeword information field.                                          */

getbit_tx(n)
    {
    return(/* 1 or 0 */);
    }
```

3. Receive Codeword Checking & Error Correction

3.1 Theory

The parity of the received 64-bit codeword is checked, then bit 63 of the codeword is inverted.
The first 63 bits of the resulting codeword are then used as the coefficients X77 to X15 of a 77 bit polynomial, which is then divided modulo-2 by the 'generating polynomial'. If the remainder is zero, and the parity check is met, then no errors have been detected;

The 15-bit remainder of this division is used as the least significant 15 bits of the 16-bit 'Syndrome' word generated by the FX429 (and by the algorithm of section 3.4), while the msb of the Syndrome word is set to '1' if the parity of the received codeword is incorrect. The resulting Syndrome word value can give an indication of which bit(s) of the codeword have been received incorrectly; see section 4.

3.2 Example of Receive Codeword Checking; No Errors

Received codeword; 6 bytes;

```
         89       AB       CD       EF       12       34       FD       42
      10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000010
  Bit;1                                                                    64
```

Step 1; even parity checked OK

Step 2, invert bit 63 then divide first 63 bits (shifted left 15 places) by generating polynomial;

```
X77 ..................................................................... X0
10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000000 00000000 000000
11101000 00010101
 1100001 10111110 1
 1110100 00001010 1
   10101 10110100 010
   11101 00000010 101
    1000 10110110 1110
    1110 10000001 0101
     110 00110111 10111
     111 01000000 10101
       1 01110111 0001010
       1 11010000 0010101
         10100111 00111111
         11101000 00010101
          1001111 00101010 1
          1110100 00001010 1
           111011 00100000 01
           111010 00000101 01
                1 00100101 0010111
                1 11010000 0010101
                  11110101 00000101
                  11101000 00010101
                     11101 00010000 000
                     11101 00000010 101
                           10010 10110010 001
                           11101 00000010 101
                            1111 10110000 1001
                            1110 10000001 0101
                               1 00110001 1100010
                               1 11010000 0010101
                                 11100001 11101110
                                 11101000 00010101
                                     1001 11111011 1111
                                     1110 10000001 0101
                                      111 01111010 10101
                                      111 01000000 10101
                                           111010 00000101 01
                                           111010 00000101 01
                                           000000 00000000 00000000 00000000 000000
```

Remainder = zero
FX429 'Syndrome' word;

```
                    00000000 00000000
```

No errors detected

3.3 Example of Receive Codeword Checking; 2 Errors

Received codeword; 6 bytes; bits 9 & 10 in error

```
         89        6B        CD        EF        12        34        FD        42
      10001001 01101011 11001101 11101111 00010010 00110100 11111101 01000010
       errors; xx
  Bit;1                                                                      64
```

Step 1; even parity checked OK

Step 2, invert bit 63 then divide first 63 bits (shifted left 15 places) by generating polynomial;

```
x77 ..................................................................... x0
10001001 01101011 11001101 11101111 00010010 00110100 11111101 01000000 00000000 000000
11101000 00010101
 1100001 01111110 1
 1110100 00001010 1
   10101 01110100 010
   11101 00000010 101
    1000 01110110 1110
    1110 10000001 0101
     110 11110111 10111
     111 01000000 10101
       1 10110111 0001010
       1 11010000 0010101
          1100111 00111111 1
          1110100 00001010 1
            10011 00110101 011
            11101 00000010 101
             1110 00110111 1100
             1110 10000001 0101
                  10110110 10011111
                  11101000 00010101
                   1011110 10001010 0
                   1110100 00001010 1
                    101010 10000000 10
                    111010 00000101 01
                     10000 10000101 110
                     11101 00000010 101
                      1101 10000111 0111
                      1110 10000001 0101
                        11 00000110 001000
                        11 10100000 010101
                           10100110 01110110
                           11101000 00010101
                            1001110 01100011 0
                            1110100 00001010 1
                             111010 01101001 10
                             111010 00000101 01
                                    1101100 11110100 1
                                    1110100 00001010 1
                                      11000 11111110 011
                                      11101 00000010 101
                                        101 11111100 11011
                                        111 01000000 10101
                                         10 10111100 011101
                                         11 10100000 010101
                                          1 00011100 0010000
                                          1 11010000 0010101
                                            11001100 00001011
                                            11101000 00010101
                                              100100 00011110 01
                                              111010 00000101 01
                                               11110 00011011 000
                                               11101 00000010 101
                                                  11 00011001 101000
                                                  11 10100000 010101
                                                     10111001 11110100
                                                     11101000 00010101
```

```
                                                    1010001 11100001 0
                                                    1110100 00001010 1
                                                     100101 11101011 10
                                                     111010 00000101 01
                                                      11111 11101110 110
                                                      11101 00000010 101
                                                         10 11101100 011000
                                                         11 10100000 010101
                                                          1 01001100 0011010
                                                          1 11010000 0010101
                                                            10011100 00011110
                                                            11101000 00010101
                                                             1110100 00001011 0
                                                             1110100 00001010 1
```

Remainder; non zero

```
                                                                        1 100000
```

FX429 'Syndrome' word; 00000000 01100000

Therefore, from the table in sectio 4, codeword bits 9 & 10 of the received codeword are incorrect.

3.4 'C' Language Algotithm

The following algorithm produces a 16-bit 'Syndrome'similar to that generated by the FX429, which will have a value of zero only if no errors have been detected in the received codeword.

```
/*************************************************************************/
/*    Function calc_syndrome() returns the 16-bit 'Syndrome' of a received */
/*    MPT1327 64-bit codeword.                                             */

calc_syndrome()
    {
    int n,bit;
    int parity=0;                          /* Clear parity register    */
    int syndrome=0;                        /* Clear 16-bit syndrome    */
    for(n = 1;n <= 64;n++)                 /* 64-bit codeword...       */
        {                                  /*                          */
        bit = getbit_rx(n);                /* Get each bit in turn;..  */
        parity ^= bit;                     /* .. update parity         */
        if(n == 63) bit ^= 1;              /* .. then invert bit 63    */
        if(n < 64)                         /* .. for bits 1 to 63;.... */
           {                               /*    .. shift parity word  */
           syndrome <<= 1;                 /*          one bit left.   */
           if( 1 & (bit ^ (syndrome >> 15))) /*    .. XOR rx bit with    */
                                           /*       MSB of parity word,*/
                                           /*       and if result == 1 */
               syndrome ^= 0x6815;         /*       then XOR syndrome  */
                                           /*       with 6815 Hex.     */
           }                               /*                          */
        }
    syndrome &= 0x7FFF;                    /* Finally, replace MSB of  */
    if(parity)                             /*  syndrome word with the  */
        syndrome |= 0x8000;                /*  calculated parity bit   */
    return(syndrome);
    }

/*   Function getbit_rx(n) should return the bit 'n' of the received      */
/*   codeword; Bit '1' is the first bit to be received, bit '64' the last.*/

getbit_rx(n)
    {
    return(/* 1 or 0 */);
    }
```

4. Error Correction

Single-bit and bit-pair errors in a received codeword may be corrected by comparing the 'Syndrome' word (generated by the FX429 or the algorithm of section 3.4) against the entries in the following table, and if a match is found inverting the corresponding bits.

Syndrome (Hex)	Error bits	Syndrome (Hex)	Error bits	Syndrome (Hex)	Error bits	Syndrome (Hex)	Error bits
0003	14, 15	468D	40, 41	8001	15	B456	25
0006	13, 14	4841	61, 62	8002	14	B484	19
000C	12, 13	4989	33, 34	8004	13	B83F	62
0018	11, 12	4B7B	45, 46	8008	12	B887	34
0030	10, 11	4BD7	22, 23	8010	11	B929	46
0060	9, 10	4E0F	16, 17	8020	10	B94D	23
00C0	8, 9	502A	62, 63	8040	9	BA05	17
0180	7, 8	50CE	34, 35	8080	8	C000	1
0300	6, 7	51B7	46, 47	8100	7	C02E	36
0600	5, 6	51E1	23, 24	8200	6	C31C	50
0C00	4, 5	530D	17, 18	8400	5	C60A	39
15D3	43, 44	574C	41, 42	8800	4	C748	57
1763	20, 21	5A62	48, 49	88E9	60	C885	28
1800	3, 4	5CD1	47, 48	8A09	32	CA3E	54
18CD	28, 29	5CFA	24, 25	8CB1	44	D048	29
193B	59, 60	5D8C	18, 19	8D21	21	E401	38
1E1B	31, 32	6000	1, 2	9000	3	E588	41
21CD	56, 57	6039	36, 37	90C7	52	E685	56
220B	38, 39	6292	50, 51	91D2	59	E815	63
2867	35, 36	6334	26, 27	9412	31	E849	35
2BA6	42, 43	64EC	57, 58	9962	43	E89E	47
2D31	49, 50	650F	39, 40	9A2B	26	E8AC	24
2E7D	25, 26	6815	63, 64	9A42	20	E908	18
2EC6	19, 20	6CAE	52, 53	A000	2	EE2D	49
3000	2, 3	6F21	54, 55	A017	37	F07E	61
3149	51, 52	740B	15, 16	A18E	51	F10E	33
319A	27, 28	786C	29, 30	A305	40	F252	45
3276	58, 59	7897	60, 61	A3A4	58	F29A	22
3657	53, 54	7B07	32, 33	A51F	55	F40A	16
3C36	30, 31	7EE3	44, 45	A824	30	F91F	27
439A	55, 56	7FBB	21, 22	B2C4	42	FC69	53
4416	37, 38	8000	64	B44F	48		

Example

Transmitted codeword

```
Bit; 1                                                                  64
     10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000010
      errors; xx
```

Received codeword

```
     10001001 01101011 11001101 11101111 00010010 00110100 11111101 01000010
```

For this received codeword, the 'Syndrome' will be 0060H, which appears in the table, indicating that the 9th & 10th bits received are incorrect, and should be inverted.

Interfacing Requirements of the FX589 GMSK Modem

This document is intended to provide further advice on the utilisation of the FX589 in a radio/data communication system. It should be used in conjunction with a current data sheet.

Bitrate, BT and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on -

- Channel spacing
- Allowable adjacent channel interference
- Tx filter bandwidth (BT)
- Peak carrier deviation (Modulation Index)
- Tx and Rx carrier frequency accuracies
- Modulator and Demodulator linearity
- Rx IF filter frequency and phase characteristics
- Use of error correction techniques
- Acceptable error-rate

As a guide, a raw data-rate of 8000bps at 12.5kHz channel spacing is achievable using a BT of 0.3 +/- 2kHz maximum deviation and no more than 1500Hz discrepancy between Tx and Rx carrier frequencies.
Forward error correction could then be used with interleaving to reduce the effect of burst errors.

Reducing the data-rate to 4800bps would allow the BT to be increased to 0.5, improving the error-rate performance.

FM Modulator, Demodulator and IF

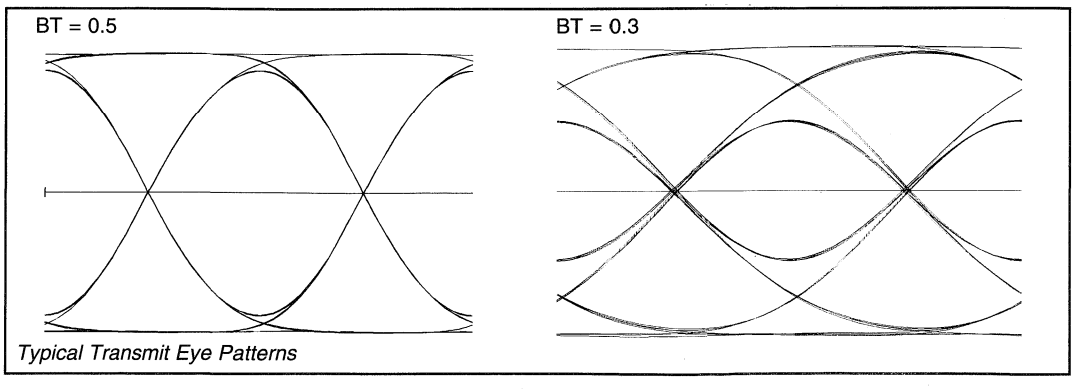
For optimum performance, the eye pattern of the received signal applied to the FX589 for random transmitted data should be as close as possible to the examples shown overleaf.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening.
To achieve this, attention must be paid to -

- Linearity and frequency/phase response of the Tx frequency modulator. Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few Hz, two-point modulation being necessary for synthesised radios.
- Bandwidth and phase response of the Rx IF filters.
- Accuracy of the Tx and Rx carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the Rx demodulator should be d.c. coupled to the FX589 'Rx Signal In' pin (with a d.c. bias added to centre the signal around $V_{DD}/2$ [V_{BIAS}]), however a.c. coupling can be used provided that -

- The 3 dB cut-off frequency is 20Hz or below (i.e. a 0.1uF capacitor in series with 100kW).
- The data does not contain long sequences of consecutive ones or zeroes.
- Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of a rf carrier) for the voltage into the FX589 to settle before the 'RxDCacq' line is strobed.



Typical Transmit Eye Patterns

Data Formats

The receive section of the FX589 works best with data which has a reasonably 'random' structure --the data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences of consecutive 'ones' or 'zeroes'. Also, long sequences (>100 bits) of '10101010 ...' patterns should be avoided.

For this reason, it is recommended that data is scrambled in some manner before transmission, for example by 'exclusive-ORing' it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceeded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble should be at least 16 bits long, and should preferably consist of alternating pairs of '1's and '0's i.e. '110011001100 .....'; the pattern '10101010 ....' should not be used.

'Acquisition' and 'Hold' Modes

The 'RxDCacq' and 'PLLacq' inputs must be pulsed 'High' for about 16 bits at the start of reception to ensure that the d.c. measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, then the above inputs should be taken 'Low' again.

In most applications, there will be a d.c. step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on.

The FX589 can tolerate d.c. offsets in the received signal of at least +/- 0.5V with respect to V_{BIAS}, however to ensure that the d.c. offset compensation circuit operates correctly and with minimum delay, the 'Low' to 'High' transition of the 'RxDCacq' and 'PLLacq' inputs should occur after the mean input voltage to the FX589 has settled to within about 0.1V of its final value. (Note that this can place restrictions on the value of any series signal coupling capacitor.)

As well as using the 'Rx Hold' input to freeze the Level Measuring and Clock Extraction circuits during a signal 'fade', it may also be used in systems which employ a continuously transmitting control channel to freeze the receive circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronisation.

To achieve this, the FX589 'Xtal' clock needs to be accurate enough that the derived 'RxClock' output does not drift by more that about 0.1 bit time from the actual received data-rate during the time that the 'RxHold' input is 'Low'.

The 'RxDCacq' input, however, may need to be pulsed 'High' to re-establish the level measurements if the 'RxHold' input is 'Low' for more that a few hundred bit-times.

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude.

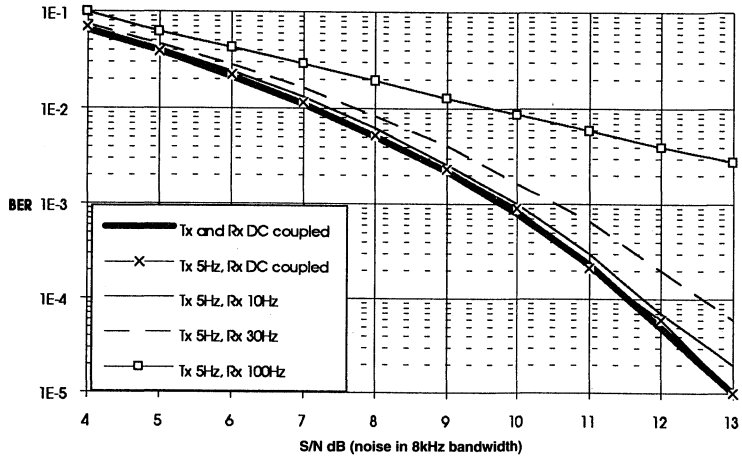
Note however, that these pins are driven from very high-impedance circuits, so that the d.c. load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

AC Coupling of Rx and Tx Signals

In practical applications, it will usually be possible to arrange for any ac coupling between the FX589 Tx output and the frequency modulator to cut-off at a very low frequency such as 5.0Hz, but ac coupling between the receive discriminator and the input of the FX589 may need to have a shorter time constant to avoid problems from voltage steps at the output of the discriminator when changing channels or when the distant transmitter turns on.

For these reasons, as well as to maintain reasonable BER, the optimum -3dB cut-off frequencies would seem to be around 5Hz in the Tx path, 20Hz in receive.

The following chart shows the typical static Bit-Error-Rate performance of the FX589 operating under nominal conditions (8kb/s, V_{DD}= 5.0V, Tamb = 25°C, Tx BT=0.3) for various degrees of A.C. coupling at the Rx Input and the Tx Output.



FX909 Signal Acquisition Principles

This Application Information publication provides guidance on the correct way of using the automatic level and timing extraction sequences of the FX909 as triggered by the AQLEV and AQBC bits of the Command Register.

The techniques detailed should work in most radio systems but slightly different operation could lead to worthwhile improvements for specific cases. Experimentation will be necessary to evaluate the performance of the procedures in comparison with system requirements.

Bit Clock Extraction and Receive Level Measurement Principles

The clock extraction circuits operate by storing on-chip a current best estimate of the bit timing of the received signal. These clock extraction circuits track the timing of the input signal by monitoring the data zero-crossings. They will eventually lose track of the timing if these do not occur for extended periods.

As data is received the device continually updates the current best estimate, unless the 'Hold' setting is selected in which case the estimate is frozen. The input signal can change the internal estimate at a speed related to the bandwidth set (PLLBW).

During acquisition the PLLBW is initially set to 'Wide' and the input signal can then rapidly alter the internal estimate. As the clock extraction circuits home-in on the received data timing the bandwidth is automatically switched to 'Medium' for 30 bits to reduce the amount of jitter and hence improve the BER performance; the setting is then changed to the residual value (as set by the Control Register, PLLBW bits).
The 'Hold' setting is intended to enable clock retention during short fades.

The upper and lower voltages of the input signal, after internal filtering, are stored on external capacitors connected to the DOC1 and DOC2 pins. These are used to generate levels inside the device to enable the detection of zero-crossings and to extract the received binary data. As data is received, the values stored on these capacitors are updated to track amplitude variations and drift, unless 'Hold' is selected in which case the voltages will decay slowly towards V_{BIAS}.

During acquisition the two capacitors are rapidly charged toward the input voltage over 1-bit period (Clamp), the capacitor voltages then follow the input signal using Lossy Peak Detect to quickly establish the upper and lower levels. As the signal is acquired the mode automatically changes to the residual setting (as set by the Control Register, LEVRES bits). The 'Hold' setting is intended to enable level retention during short fades.
Note that to operate correctly in the 'Peak Averaging' mode it is required that bit timing has already been established.

The level extraction circuits require the voltages present during pairs of '1's' and '0's', i.e. the upper and lower values. If '00' and '11' sequences do not occur for periods greater than approximately 100 bits the levels stored will not accurately reflect those of the input wave.

Acquisition Operation

The acquisition sequences available to the user of the FX909 are intended for 2 types of system:

1 'Mobitex' type systems with some form of carrier or signal detect facility.
2 Systems with no carrier or signal detect indication.

In both cases it is assumed that the incoming signal to be detected consists of a bit sync pattern (..11001100..) followed by a system synchronisation pattern and that the device is set to raise an interrupt when this occurs (an SFS or SFH task has been set). The following techniques should lead to reliable detection and acquisition of the start of isolated data for most radio systems. (See note on ac coupling).

'Mobitex-Type' - Carrier Detect Indication Available

The device must lock-on to the incoming signal within the 16 bits of bit sync; to achieve this it is necessary to activate both AQBC and AQLEV acquisition sequences at or before the start of the bit sync, typically during a period of unmodulated carrier which precedes messages. In this case the AQBC and AQLEV automatic sequences can be used with the residual settings for the PLLBW = 'Medium' or 'Narrow' and LEVRES = 'Peak Averaging'. The BER will improve toward its steady value over a period of approximately 30 bits from the start of the bit-sync.

It is important that when the AQLEV acquisition sequence is started the voltage level of the input wave is within, or at worst just outside, the extremes of a '11110000' data pattern.

No 'Carrier Detect' Available

Where no carrier or signal detect circuitry is available the device has to lock onto the incoming signal with little or no cue from the controlling device, this will of course mean that acquisition will take longer and that decoding errors are more likely.

The FX909 must track the incoming signal continuously for a data signal and the best settings to achieve this will be PLLBW = 'Wide' and LEVRES = 'Lossy Peak Detect'. To initiate this the AQBC and AQLEV bits would need to be set with the residual PLLBW = 'Medium' or 'Narrow' and LEVRES = 'Lossy Peak Detect' or 'Peak Averaging'.

When the synchronisation pattern is successfully detected the PLLBW and LEVRES functions will automatically sequence to the residual setting.

Where the device is required to detect a signal in this way it is recommended that the bit sync sequence of repetitive '..0011..' bits is extended from 16 (Mobitex spec.) to ⊕64 or that the pre-message unmodulated carrier period is extended. Also it may be found advantageous to lengthen the frame sync sequence to reduce the possibility of frame sync. falsing.

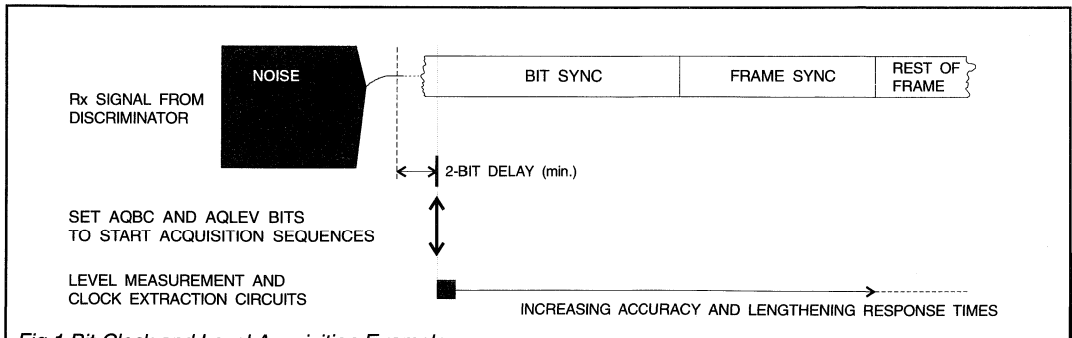


Fig.1 Bit-Clock and Level Acquisition Example

Acquisition Notes

Frame Sync Falsing

When noise or an unmodulated carrier is fed into the device the output of the internal bit decode circuits will effectively be random data. This will have the effect of triggering the frame-sync detect circuit whenever this random data matches the frame-sync bytes programmed. There is little possibility of this happening if a Search for Frame Head or Search for Frame Sync task is set at the beginning of the bit-sync.

However if the device is set to detect a message a long time before it appears, and no carrier detect is available, the possibility of falsing is increased. This problem is aggravated in the case of the Mobitex system which specifies that the frame sync must be detected with up to any one bit in error; this raises the probability of falsing, due to random data, from 1 in 2^16 bits to 17 in 2^16 bits.

The user can significantly reduce the chances of falsing by providing extra frame sync bits after those programmed in the FX909. For example, when receiving a signal with 4 bytes of frame sync the receiving device is programmed with the first two bytes (LFSB), when these are detected using the SFS task, two RSB tasks are issued.

Decoding of the signal only continues if these next 2 bytes match the last two bytes of the 4 byte frame sync otherwise the search would be restarted.

Short Unmodulated Carrier and Bit Sync Sequences

The most critical case to be met is to use the FX909 in a system where no carrier detect or signal presence indicator is available, the frame-sync is short and the unmodulated carrier is present for a short period.

The device is required to lock-on to the incoming signal within 16 bits whilst also dealing with the potentially large dc and level changes that can occur just before the message is received.

Operating to such a system may result in some proportion of received messages being missed due to frame sync falsing and missing the frame sync bytes due to decoding errors. It is therefore recommended that the FX909 is used in systems with a short unmodulated carrier and bit sync sequences, only if a carrier detect or similar indication is available.

AC Coupling

The effect of ac coupling is to reduce the static BER performance for a given S/N ratio as it causes low frequencies to be attenuated and cause dc changes to appear as a decaying voltage superimposed upon the signal. A carrier, giving a dc shift, coming on near the start of a message will have the effect of confusing the level detection circuitry and hence cause errors in extracting data. It would be better to delay the message appearing until any dc shift had decayed thus improving the likelihood of correct acquisition. In either case the automatic acquisition sequences can be used.

Automatic Acquisition Sequences

Sequences of operation for automatic acquisition. For situations when a bit sync pattern is not being searched for (SFS or SFH is not set) the FX909 uses a fixed number of bits delay in switching between the modes:

AQLEV

SFH or SFS is set:	1 bit of clamp Lossy peak detect until frame sync is detected Residual setting
SFH or SFS is not set:	1 bit of clamp 30 bits of lossy peak detect Residual setting

AQBC

SFH or SFS is set:	'Wide setting' until frame sync detected 30 bits of 'Medium setting' Residual setting
SFH or SFS is not set:	16 bits of 'Wide setting' 30 bits of 'Medium setting' Residual setting

An Audio Delay Circuit Based on the FX609 CVSD Codec

The diagram shown on the following page is an audio delay circuit based on the FX609 CVSD Codec, employing, additionally, a Fujitsu MB81C71 64k x 1-bit RAM, two 4520 counter ICs, and a 4069 inverter microcircuit.
It provides a starting point for a designer who wishes to implement an audio delay circuit.
CML makes no guarantee of its performance and assumes no responsibility for its use in any product.

Circuit Operation

In the following operational description, a bar over a signal name is used to indicate an active-low signal. For example $\overline{W}$ is an active-low write enable signal.

On the FX609J Clock Mode 1, (pin 22) is tied to V_{DD} and Clock Mode 2, (pin 21) is tied to ground to set the encode and decode clocks for a sampling rate of 32kb/s. The Encoder Force Idle, Powersave, and Decoder Force Idle inputs, (pins 6, 15 and 16) respectively, are tied to V_{DD} to set them inactive. The data Enable input, pin 7, is tied to V_{DD} to make the encoded data available at the Encoder Output, pin 5. Pin 19, the Algorithm Select input, is tied to ground to select a four-bit companding algorithm. The other inputs are the same as recommended for "External Component Connections" shown in the FX609 Data Sheet.

The audio signal to be delayed is input to the FX609 Encoder Input, where it is converted to a serial stream of digital data. The serial data is output on Encoder Output; and connected to the D input, of the MB81C71 memory chip. The decoder Data Clock output of the FX609 is connected to pin 1 of the 4069 inverter. The output of the inverter, pin 2, is connected to pin 10 of the MB81C71, the $\overline{W}$ input, and to pin 3 of the 4069, the input to second inverter. Pin 4, the inverter output, is connected to the enable input of the first 4520 counter.

The enable input is taken from the second inverter to ensure that the 4520 counters increment after the $\overline{W}$ signal into the 81C71 transitions from low to high. The clock inputs of each of the 4520s, pins 1 and 9, are tied to ground so that only the enable inputs control when the counters increment. The reset inputs, pins 7 and 15, are also tied to ground so that they never reset the counters. The individual four-bit counters in the 4520s are cascaded to produce a 16-bit counter. The counter outputs, Q15 - Q0, are connected to the address inputs, A15 - A0, of the MB81C71.

There are switches between Q15 and A15 and between Q14 and A14. The switches allow the number of bits of the counter, and therefore the length of the delay, to be adjusted. When the Decoder Data Clock falls from high to low, the counter, and therefore the address, increments. Since the $\overline{W}$ input to the memory, pin 17, is the complement of the clock, it rises from low to high, latching the encoded data bit at the D input. The E input to the MB81C71, pin 12, is tied to ground so that the memory is always selected. When $\overline{W}$ is high and the address is stable, a valid data bit appears at the Q output, pin 17, of the MB81C71. The address of the data bit appearing that was just written, so the counter must cycle through its entire range before a data bit that has been written into the memory can be read. Therefore a data bit output from the FX609 at the Encoder Output pin is delayed by the number for clock periods of the range of the counter. The delay is given by

$$\textit{Delay} = (T \text{ sec/cycle}) * (2^N \text{ cycles})$$

where

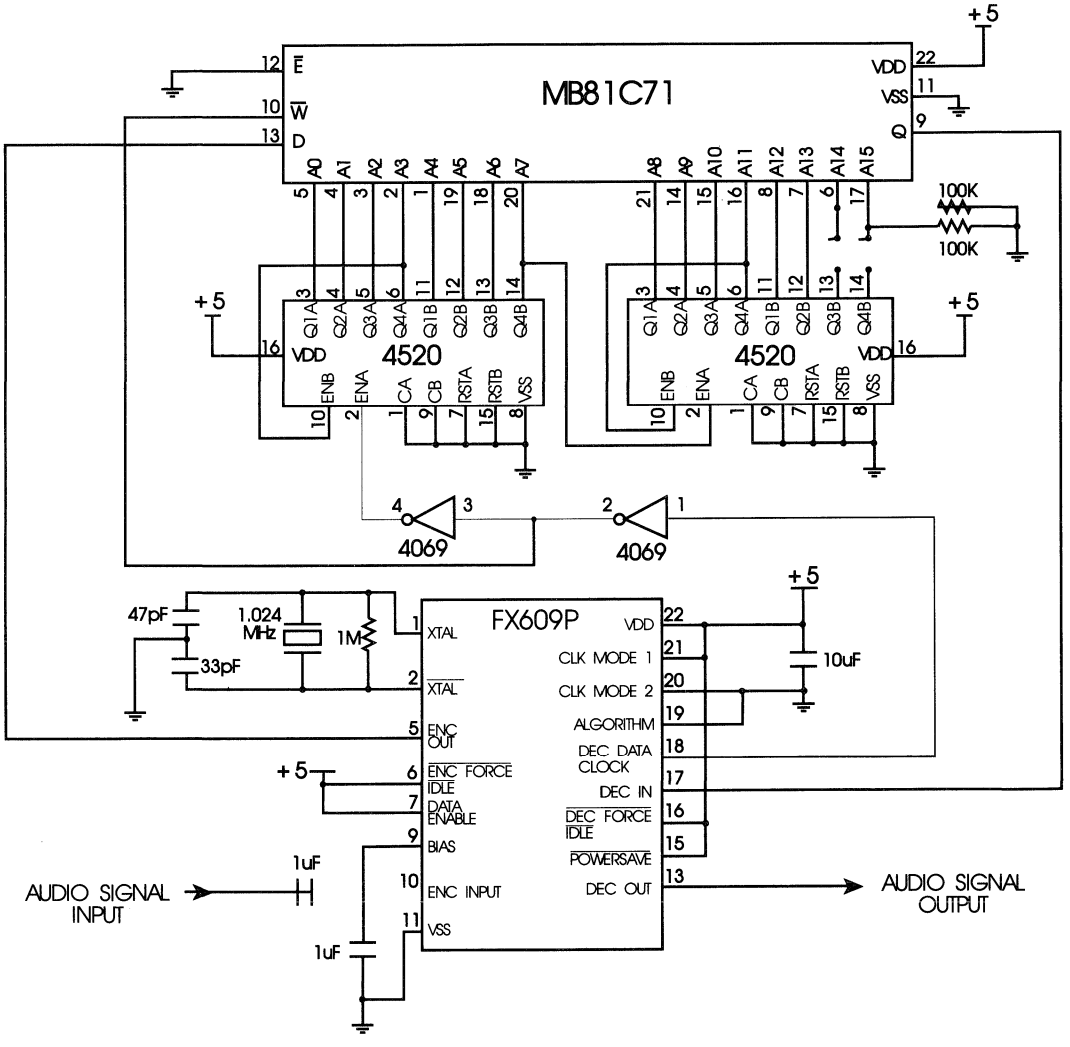
T = Period of the Decoder Data Clock

N = Number of bits used in the counter

If all 16 bits of the counter are used, and the Decoder clock frequency is 32kHz, then the delay would be

$$\textit{Delay} = (1/32000) \text{ sec/cycle} * (216) \text{ cycles}$$
$$= 2.048 \text{ seconds}$$

In this example, all locations of the memory are used. If a shorter delay is desired, the counter outputs and address inputs can be opened. If only 14 bits of the counter are used, then the delay is reduced by a factor of four, to 0.512 seconds. The range of delays could be increased even more by adding more switches and by making the sampling clock frequency adjustable. The Q output, pin 9 of the MB81C7 is connected to the FX609 Decoder Input. The decoder clocks in the serial digital data stream from the memory and converts it to an analogue signal which is output at the Decoder Output. The Decoder Output is the delayed audio signal.


MB81C71
+5
100K
100K
4520
4520
4069
4069
FX609P
47pF
33pF
1.024 MHz
1M
10uF
1uF
1uF
AUDIO SIGNAL INPUT
AUDIO SIGNAL OUTPUT
XTAL
ENC OUT
ENC FORCE IDLE
DATA ENABLE
BIAS
ENC INPUT
VSS
VDD
CLK MODE 1
CLK MODE 2
ALGORITHM
DEC DATA CLOCK
DEC IN
DEC FORCE IDLE
POWERSAVE
DEC OUT

Publication D/XT/2 December 1991

Xtal Oscillator Circuits

This Application Note discusses a general Xtal oscillator circuit applicable to most individual CML microcircuits.

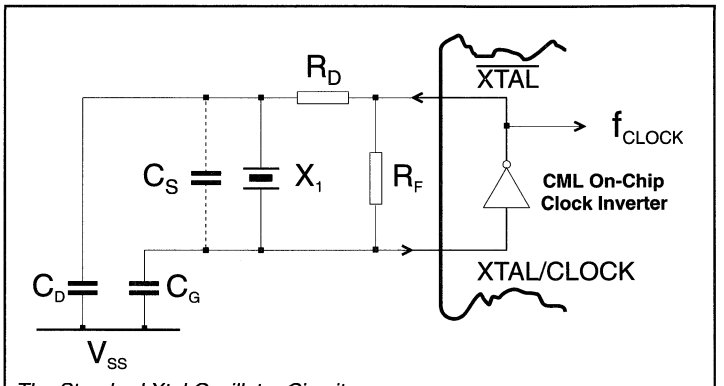
The figure below shows the standard Xtal oscillator circuit from which most recommended Data Sheet circuits are derived.

The standard on-chip CML CMOS oscillator circuit will function correctly with the majority of Xtals, however the use of this circuit with a few Xtal types may cause the following problems:

1. Excessive drive level to the Xtal.
2. Excessive over-voltage, outside the device maximum ratings, at the oscillator input pin. This over-voltage may show itself as degraded microcircuit performance.

Note: Operation of any CML microcircuit without a Xtal or clock input may cause device damage.

To minimise damage in the event of Xtal/drive failure, it is recommended that the power rail (V_{DD}) is fitted with a current limiting device (resistor or fast-reaction fuse).



The Standard Xtal Oscillator Circuit

Standard Xtal Oscillator Components

R_F Feedback Resistor

To set the bias point of the internal amplifier. Low values of R_F will reduce loop-gain and disturb the phase of the feedback network. Typical value = 1.0MΩ ± 20% in a range of 1.0MΩ to 20MΩ.

R_D Drive Resistor

Used to limit the Xtal drive level by forming a voltage-divider between R_D and C_D. R_D also stabilizes the oscillator against changes in the output impedance of the inverter. To verify that the maximum operating supply voltage does not overdrive the Xtal, observe the output frequency as a function at the buffered output. Under proper operating conditions the frequency should increase slightly (a few ppm) as the supply voltage increases. If the Xtal is being overdriven, an increase in supply will normally cause a decrease in frequency or instability. If the latter is the case (i.e. Xtal being overdriven), increase the value of R_D *(refer to the Xtal manufacturers' recommendations).*

X_1 Xtal

A parallel resonant Xtal to the value recommended in the relevant Data Sheet.

C_D Drain Capacitor

To provide phase shift and reduce Xtal drive. Large values of C_D tend to stabilize the oscillator against variations in power supply voltage but also reduce the tuning capability of the oscillator and overtone activity. *A typical value is 33.0pF ± 20% (Xtal manufacturer may recommend 5 – 40pF).*

C_G Gate Capacitor

To provide phase shift and input voltage for the amplifier. In some oscillator circuits C_G is used to adjust the oscillator to frequency although this generally may not be required. Large values of C_G reduce loop-gain and increase stability. C_G may be used to reduce over-voltage at the inverter input. However, the reduction in loop-gain may cause oscillator start-up problems. *C_G value will be typically 5 – 65pF ± 20%, (refer to Xtal manufacturers recommendations).*

C_S Stray Capacitance

Due to the low motional capacitance of small Xtals and the high inverter input impedance, the designer should be concerned with circuit board layout. For best oscillator performance C_S should be less than 1.0pF.

Integrated Circuits Data Book

Section 12

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Consumer Microcircuits Limited
1 Wheaton Road, Witham, Essex, CM8 3TD, U.K.
Tel: (+ 44) 1376 513833 Telex: 99382 CMICRO G Fax: (+ 44) 1376 518247
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Lamezanstr. 10
A-1232 Vienna
Austria
Tel: (0222) 610620
Fax: (0222) 61062151

Australia
VSI Electronics (Australia) Pty. Limited
Unit C, 6-8 Lyon Park Road, (PO Box 888)
North Ryde, NSW 2113,
Australia.
Tel: (02) 878 1555
Fax: (02) 878 1166

Belgium & Luxembourg
Heynen N.V
Industriepark Houthalen-Zuid,
De Koelen 6, 3530 HOUTHALEN,
Belgium.
Tel: (011) 52 57 57 Telex: 39047
Fax: (011) 52 57 77

Canada
Paltronics Limited,
1121 Invicta Drive, Unit 2,
Oakville, Ontario,
Canada L6H 2R2
Tel: (905) 844 2233
Fax: (905) 844 0129

Croatia & Slovenia
Eurodis Electronics GmbH
Lamezanstr. 10
A-1232 Vienna
Austria
Tel: [43] (1) 610620
Fax: [43] (1) 61062151

Czech & Slovak Republics
Eurodis Electronics GmbH
Lamezanstr. 10
A-1232 Vienna
Austria
Tel: [43] (1) 610620
Fax: [43] (1) 61062151

China
Asian Automation Associates Ltd.
1/F Hong Kong Productivity Council Building
78 Tat Chee Avenue,
Kowloon Tong, Kowloon,
Hong Kong.
Tel: [852] 7885311
Fax: [852] 7885314

Denmark
Ginsbury Electronic A/S
Bydammen, 1 G, DK-2750
Ballerup, Denmark.
Tel: 44664470
Fax: 44664406

Finland
Ginsbury Electronic Scandinavia OY.,
Laurinkatu 51B 12,
SF-08100, Lohja,
Finland.
Tel: 12314910
Fax: 12314912

France
Ginsbury Electronique SA
3 Rue Nationale, 92100 Boulogne
France.
Tel: (1) 49 109933 Telex: 633 246
Fax: (1) 49 109578

Germany
Ginsbury Electronic GmbH
PO Box 82 03 40, 81829 München,
Germany.
Tel: (089) 45170-0 Telex: 529818
Fax: (089) 45170-100

Greece
Peter Caritato & Associates S.A.
31 Ilia Iliou St., Athens 117 43
Greece.
Tel: (01) 9020115 Telex: 216723 CARI GR
Fax: (01) 9017024

Holland
Heynen B.V. PO Box 10,
NL-6590 AA Gennep, Holland.
Tel: 08851 96111
Fax: 08851 96200

Hong Kong
E. I. L. Company Limited,
Unit E, 5/F., On Hang Industrial Centre,
18 Yip Cheong Street,
Fanling, N.T., Hong Kong.
Tel: 669 7238
Fax: 669 1309

Hungary
Eurodis Electronics GmbH
Lamezanstr. 10
A-1232 Vienna
Austria
Tel: [43] (1) 610620
Fax: [43] (1) 61062151

India
Mekaster Telecom PVT Ltd.
908, Ansal Bhawan, 16, Kasturba Gandhi Marg
New Delhi-110 001 India
Tel: (011) 3312110 Telex: 31 66223 MPTL IN
Fax: (011) 3712155

Israel
Gallium Electronics Ltd.
5 Ussishkin St., PO Box 1379
Ramat-Hasharon 47100,
Israel
Tel: (03) 5402242
Fax: (03) 5402425

Italy
Esco Italiana S.p.A.,
Viale F.III Casiraghi, 355,
20099 Sesto S. Giovanni,
(MI), Milan, Italy.
Tel: (02) 2409241 Telex: 322383
Fax: (02) 2409255

Japan
Cornes & Company Limited,
2-5-12 Higashi-Kanda,
Chiyoda-ku,
Tokyo 101, Japan.
Tel: (03) 5821-1628
Fax: (03) 5821-1632
Cornes & Company Limited,
Cornes House,
13-40, Nishi-Honmachi, 1-Chome,
Nishi-ku, Osaka 550, Japan.
Tel: (06) 532-1013 Telex: 525-4496 COROSA.J
Fax: (06) 541-8850, 06 532-7749

Korea
S-Tec International Co. Ltd.,
Room 1301-1, Yoido Dept. Store Bldg,
36-2 Yeoido Dong, Yeongdeungpo-Ku,
Seoul, 150-010, Korea.
Tel: (02) 784 6800 Telex: K 23456 STECI
Fax: (02) 784 8600

New Zealand
VSI Electronics (NZ) Ltd.
274 Church Street, Penrose,
Auckland, New Zealand.
Postal Address: Private Bag 92821,
Penrose, Auckland, New Zealand.
Tel: (9) 636 7801
Fax: (9) 636 7803

Norway
Hans H Schive A/S,
Undelstadlia 27, PO Box 10,
N-1371 Asker, Norway.
Tel: (066) 900 900
Fax: (066) 90 44 84

Poland
Delta Elcom Limited,
Biuro w Polsce: DELTA TECH
02-134 Warszawa,
ul: 1-go Sierpnia 44/46
Tel./Fax: (022) 465370.
Int. Fax: (039) 121229.

Portugal
Digicontrole LDA,
AV. Eng. Arantes e Oliveira,
5-2° D, 1900 Lisboa (Lisbon) Portugal.
Tel: (01) 80 57 30 Telex: 62251
Fax: (01) 84 90373

Singapore and Malaysia
Uraco Impex Asia PTE Ltd.
47, Loyang Drive
Singapore 1750
Republic of Singapore
Tel: 5457811 (DID - 540834)
Fax: 5456120
Uraco Impex (M) SDN BHD
2-2 Lorong 6C/91
Taman Shamelin Perkasa Jalan Cheras
56100 Kuala Lumpur
Malaysia
Tel: (03) 9846055
Fax: (03) 9845998
Uraco Impex (M) SDN BHD
7E-2 Gottheb Road
10350 Penang
Malaysia
Tel: (04) 373920
Fax: (04) 376668

South Africa
Uniplan Pty. Limited
PO Box 7259, Johannesburg 2000
South Africa.
Tel: (011) 402 5800
Fax: (011) 402 6674

Spain
S.A. General De importaciones
Electronicas "Sagitron,"
C/Corazon de Maria 80-82,
28002 Madrid, Spain.
Tel: (01) 416 9261
Fax (01) 415 8652

Sweden
Ginsbury Electronic Scandinavia AB.,
PO Box 5068, Jäegerhorns Väg 19,
S-141 05 Huddinge, Sweden.
Tel: (08) 7405560
Fax: (08) 7404790

Switzerland
Egli, Fischer & Co. Limited,
Gotthardstrasse 6, Claridenhof,
8022 Zurich, Switzerland.
Tel: (01) 209 8111 Telex: 815535
Fax: (01) 201 2275

Taiwan
Prospect Technology Corporation
5F, No. 348, Sec. 7,
Cheng Teh Road, Taipei,
Taiwan. R.O.C.
Tel: (02) 820 5353
Fax (02) 820 5731

Turkey
Empa (elektronik mamülleri pazarlama a.s.)
34630 Besyol Londra Asfalti, Florya Is,
Merkezi, Sefakoy-Istanbul, Turkey.
Tel: (212) 599 30 50 Telex: 21137 Etna tr
Fax: (212) 598 53 53

United Kingdom, U.S.A. and other Territories
Refer to:
Consumer Microcircuits Limited
1 Wheaton Road, Witham,
Essex, CM8 3TD, U.K.
Tel: [+ 44] (1376) 513833
Fax: [+ 44] (1376) 518247

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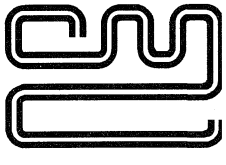

Consumer Microcircuits Limited

1 Wheaton Road Witham Essex CM8 3TD England

Telephone: [44] (376) 513833 • Telex: 99382 CMICRO G • Telefax: [44] (376) 518247

CML Semiconductor Products

PRODUCT DATA AMENDMENT

Integrated Circuits Data Book - Edition 3

- FX613 Data Correction -

Publication DA/DB3 1994

1.0 Introduction

1.1 An error during the production of Edition 3 of the CML Integrated Circuits Data Book (1994) has produced incorrect information on pages 6 . 4 and 6 . 6 (FX613) of that publication.
Pages 6. 4 and 6 . 6 do not refer in any form to the FX613 product; these pages are to be disregarded.
The 'pages' detailed on pages 2 and 3 of this Product Data Amendment are the correct 'pages' and should be used as a direct replacement for the incorrect pages.

2.0 Reference Document(s)

2.1 CML Integrated Circuits Book, Edition 3; Pages 6 . 4 and 6 . 6; FX613 Publication No. D/613/2 July 1994.

3.0 Additions and Alterations

3.1 Two options are available to correct this error:

3.1.1 Replace pages 6 . 4 and 6 . 6 in their entirety with the pages supplied in this document (by pasting over).

3.1.2 Ensure that this Product Data Amendment is kept with Edition 3 of the Integrated Circuits Data Book at all times.

4.0 Product Identification

4.1 This Product Data Amendment refers to Pages 6 . 4 and 6 . 6 of the CML Integrated Circuits Data Book, Edition 3.

Pin Number		Function
FX613DW	FX613P	
1	1	**Xtal/Clock**: The input to the on-chip clock oscillator inverter. A 3.579545MHz Xtal or externally derived telephone system clock (f_{XTAL}) should be connected here. Note - The operation of the FX613 without a suitable Xtal/Clock input may cause device damage.
2	2	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter. See Figure 2.
3	3	No internal connection.
4	4	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS}.
5	5	**Level In:** The input for level discrimination. This input is internally biased to V_{BIAS}, signals must be a.c. coupled. The audio signal must be fed to both this pin and the Signal In pin. Correct level detection determines the operation of this device (see Principles of Decoder Operation), however to disregard the amplitude of the input levels the FX613 may be permanently enabled by pulling this pin to V_{DD} and disabled by pulling to V_{SS}.
6	6	**Signal In:** The input for frequency discrimination and decoding. This input is internally biased to V_{BIAS}, signals must be a.c. coupled. The audio signal must be fed to both this pin and the Level In pin.
7		No internal connection.
8	7	**V_{SS}:** Negative supply rail. Signal ground.
9	8	No internal connection.
10		No internal connection.
11	9	**$\overline{\text{IRQ}}$:** This Interrupt Request output from the FX613 is 'wire-OR able' allowing the interrupt outputs of other peripherals to be combined and connected to the Interrupt input of a µProcessor. This input has a low-impedance pulldown to V_{SS} when active and a high-impedance when inactive. An interrupt is produced on completion of a HI or LO frequency measurement.
12	10	**Serial Clock:** The serial clock from the µProcessor. Data Out is clocked into the µProcessor on the rising edge of the Serial Clock. See Data-Read Timing diagram.
13	11	**$\overline{\text{Chip Select}}$:** A logic "0" at this input will select this device.
14	12	**Data Out:** The serial data output. Under the control of the Chip Select and Serial Clock inputs, data should be read from this output in 6-bit blocks MSB (Bit-5) first. If 8 serial clock pulses are applied, two additional logic "0s" will be output after Bit-0.
15	13	No internal connection.
16	14	**V_{DD}:** Positive supply rail. A single, stable supply is required. Levels and voltages within the FX613 are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor located close to the FX613 pins.

Application Information .....

Principles of Decoder Operation

Level Detection

As level and frequency discrimination operations take place in parallel the audio signal should, under normal circumstances, be input to both Signal In and Level In pins via coupling capacitors.

If the input signal level (Level In) is outside the preset 'Must/Must Not Decode' thresholds (Specification Page), the Universal Call Progress Decoder will be disabled.

If it is wished to disregard signal input *levels* at the Level In pin and attempt to decode under all conditions, the decoder may be permanently enabled by holding the Level In pin at V_{DD}.
The device can disabled by pulling Level In to V_{SS}.

NOTONE Recognition

The NOTONE condition can be recognized using µProcessor software timing as below.

a. Set the µP timer period to a period greater than the relevant frequency-band measurement period (13.16ms or 39.47ms).

b. Each 'Tone Measurement Complete' interrupt from the FX613 must reset the µP timer.

c. With NOTONE or white noise at the decoder input, the FX613 on-chip timer will be continually reset.

   ii No 'Tone Measurement Complete' interrupt will occur - the µP timer will run.

   ii The µP Timer time-out can be considered as a **NOTONE** indication.

Level In	Timer	IRQ	Data Out
In Limits	Running	Enabled	Enabled
Out of Limits	Reset	Disabled	Disabled (frozen to previous bit-5 level
V_{DD}	Running/Reset	Enabled/Disabled	Enabled (dependent upon Quality measurement)
V_{ss}	Reset	Disabled	Disabled (frozen to previous bit-5 level)

Frequency Band Discrimination

The input signal is amplified by a self-biased (zero-crossing) inverting amplifier and then 'filtered' to remove high-frequency noise and jitter.

High (HI) and Low (LO) counters are employed to determine the input frequency band (HI = 900Hz to 2150Hz, LO = 300Hz to 660Hz).

If the input frequency is in the LO Band, the device will operate as a LO Band decoder and will remain so until a HI frequency signal is detected. If the input frequency is in the HI Band, the device will operate as a HI Band decoder and will remain so until a LO frequency signal is detected.

Frequency band monitoring is continuous with the band selection taking place every 9.8ms. It will therefore take 9.8ms from Power-Up to set up the initial correct decode frequency band.

On-Chip Timer Operation

For frequency measurement, the FX613 counts the number of input cycles in a fixed time period. This fixed period, measured by the continuous on-chip timer, is set to 13.16ms for HI Band inputs and 39.47ms for LO Band inputs.

On-Chip Timer Operation .....

When the timer expires the following actions take place:

a. A HI or LO ("1" or "0") band indication bit is latched into Bit-5 of the Serial Output Port.

b. The Frequency Counter count of 5-bits is latched into the Serial Output Port (Bit-4 [MSB] to Bit-0). The Serial Output Port Contains 6-bits, if 8 Serial Clock edges are employed, two extra "0s", which should be ignored, will be output last.

c. An interrupt is generated (IRQ) to the µProcessor. The contents of the Serial Output Port should be read before the next interrupt is expected; if not data will be overwritten.

When the Chip Select input is set to "0" the interrupt is reset.

The On-Chip Timer and Frequency Counter will be reset in mid-count, and therefore unable to allow a valid measurement, under the following conditions:

a. A change of decode frequency band.

b. Decoder disabled; signal input level out of specification or Level Detect input set to V_{SS}.

c. Signal Quality Assessment considered 'Bad'.

d. Input signal frequency outside limits.

TELECOM ICs

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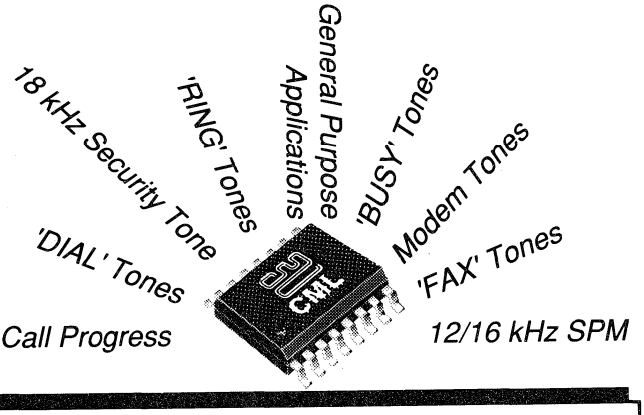

NEW For PABX & PAIR-GAIN Systems

FX641 Two-Channel 12/16kHz Detector

FX613 Universal Call-Progress Tone Decoder 300Hz to 1800Hz

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Consumer Microcircuits Limited
1 WHEATON ROAD · WITHAM · ESSEX · CM8 3TD · ENGLAND
Telephone: +44 376 513833 · Fax: +44 376 518247

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